



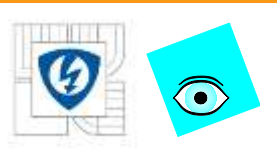
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

HW pro Rapid Control prototyping, HIL a finální nasazení

Ing. Roman Vala a Ing. Jiří Kepřt, Ph.D.

8. dubna 2011

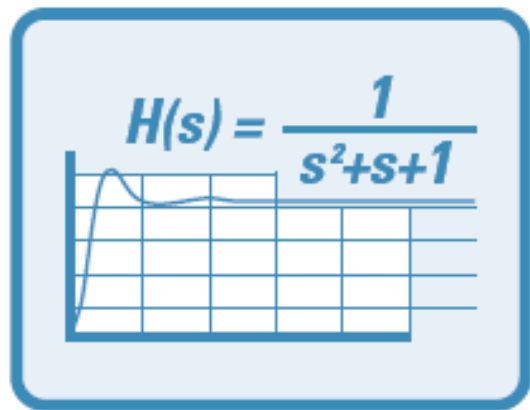
Tato prezentace je spolufinancována Evropským sociálním fondem a státním rozpočtem České republiky.



Agenda

- PXI / PXIe (PC – PCI / PCIeexpress)
- FPGA boards - Reconfigurable IO
- FlexRIO
- Compact RIO
- Single Board RIO

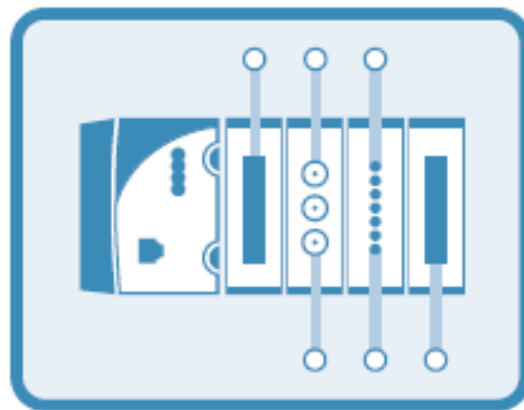
Graphical System Design



Design

Interactive Algorithm Design

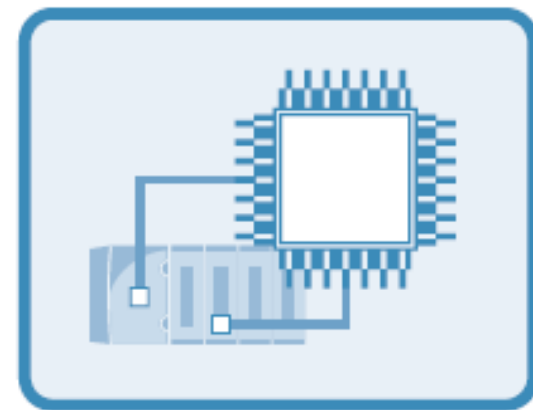
- Control design
- Dynamic system simulation
- Digital filter design
- Advanced mathematics



Prototype

Tight I/O Integration

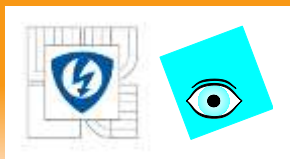
- I/O modules and drivers
- COTS FPGA hardware
- VHDL and C code integration
- Design validation tools



Deploy

Deployable Targets

- Rugged deployment platforms
- Distributed networking
- Human-machine interfaces
- Custom designs



Who Benefits from Graphical System Design

- **The “Domain Expert”**

- Non-embedded programming guru
- System-level engineer or scientist



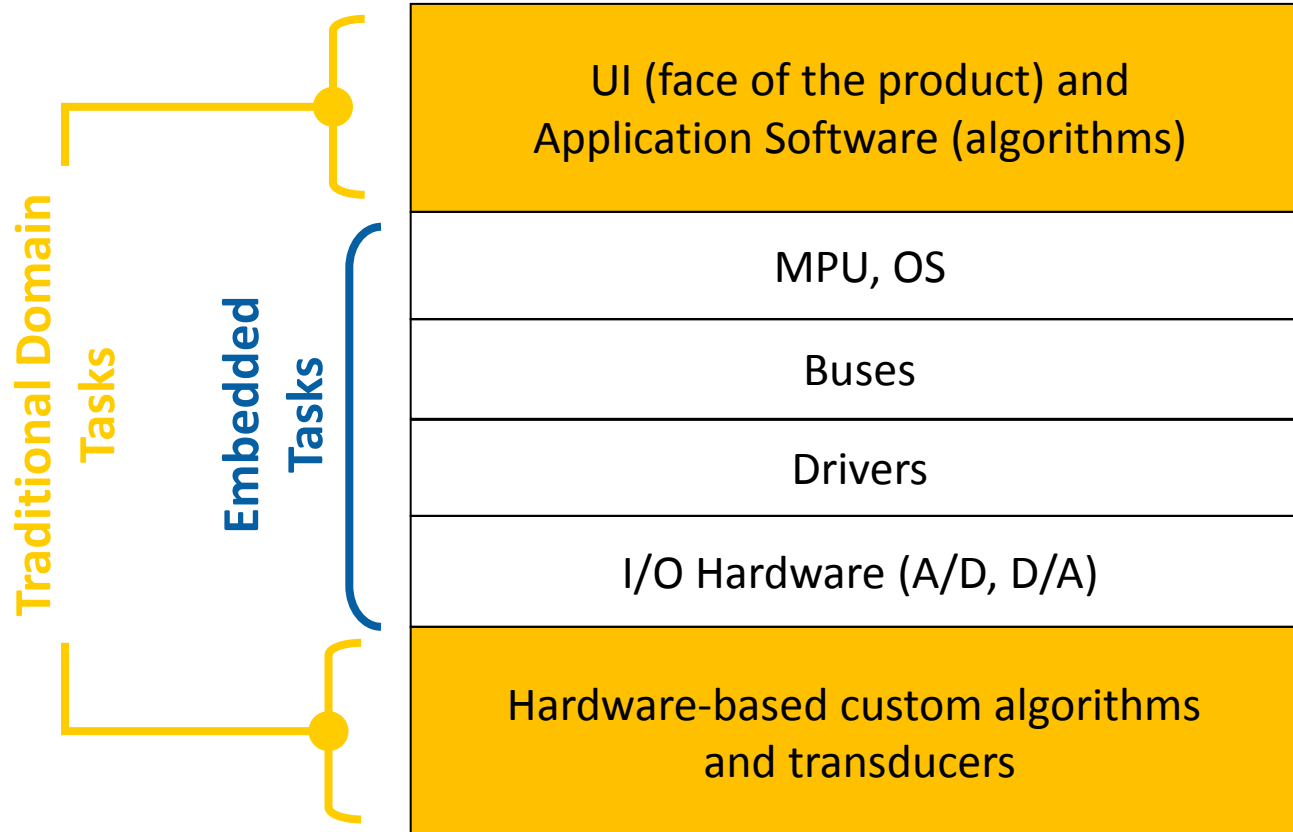
- **The “Embedded Expert”**

- Anyone needing easier, faster development process
- Anyone needing Commercial Off-The-Shelf (COTS) hardware to streamline development



Traditional Embedded System Design

Embedded Engineer Carries The Load

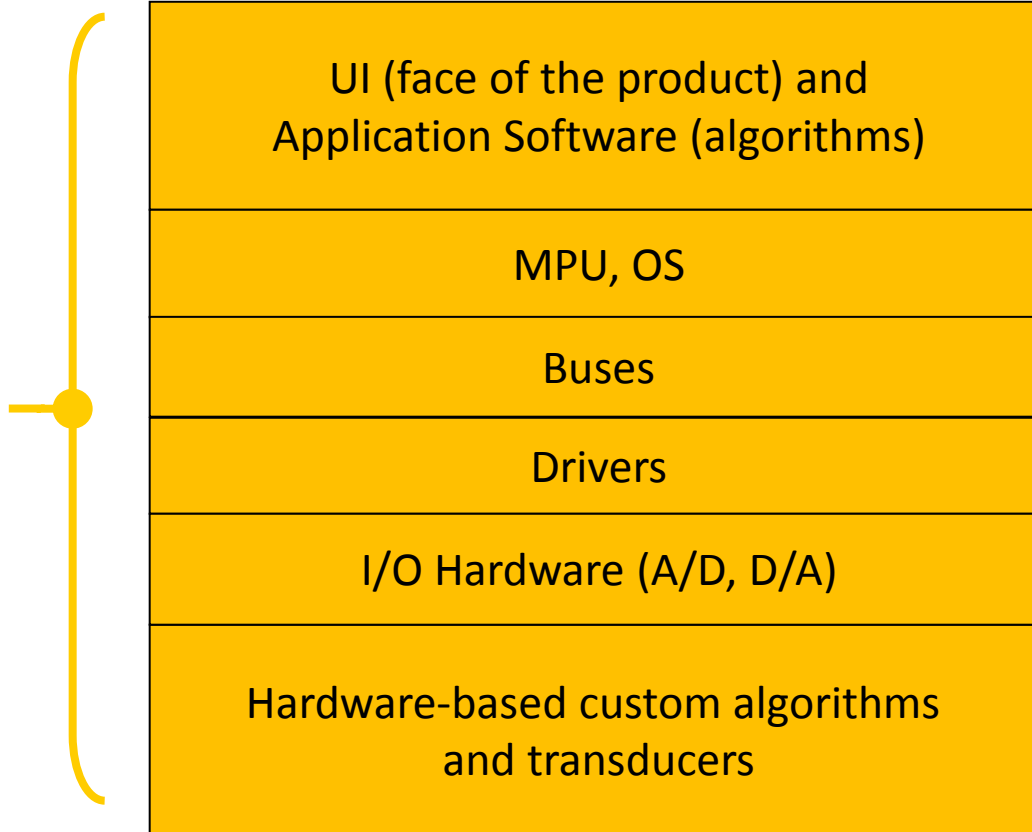




Graphical System Design

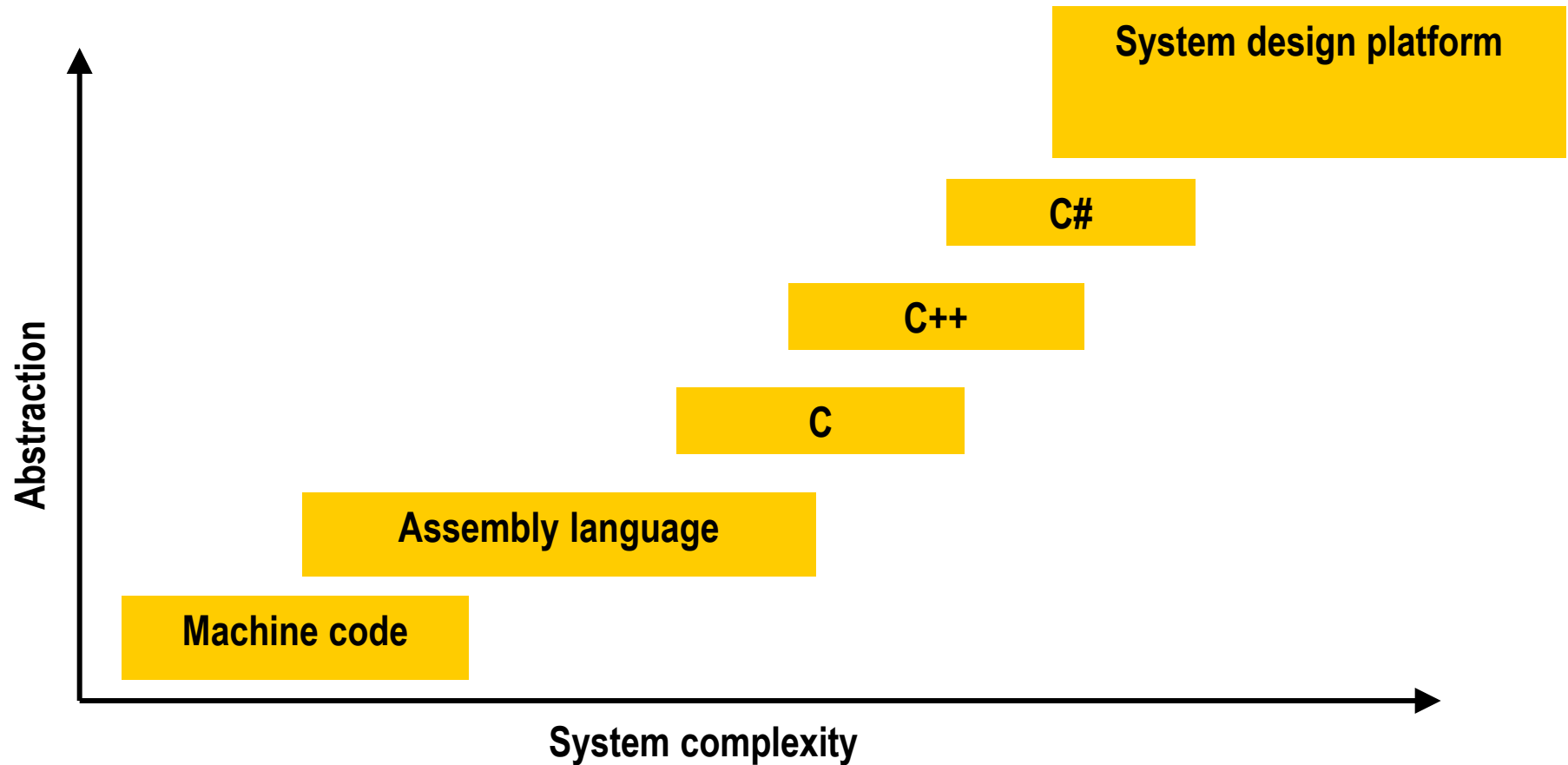
Bringing Embedded Design to the Masses

Graphical System Design
Domain and Embedded Tasks





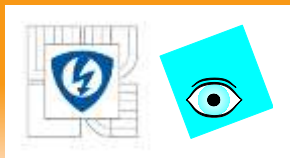
Evolution of Software Abstraction





High-level of Abstraction in LabVIEW

- Target different hardware (MPU, MCU, DSP, FPGA, GPU, hybrids....) from a High-level of Abstraction
- Graphical programming hides complexity of C, VHDL, Assembly code.....



NI Platform for Control

LabVIEW Development Tools for Control and Design Applications

Control Design and
Simulation Module

System ID Toolkit

PID & Fuzzy Logic
Toolkit

Statechart Module

Simulation Interface
Toolkit

NI Motion Control

LabVIEW Real-Time

LabVIEW FPGA

LV Embedded

LabVIEW Real-Time Hardware Targets



LabVIEW Real-Time



PXI



Desktop or Industrial PC



Industrial
Controllers



CompactRIO



Single-Board RIO

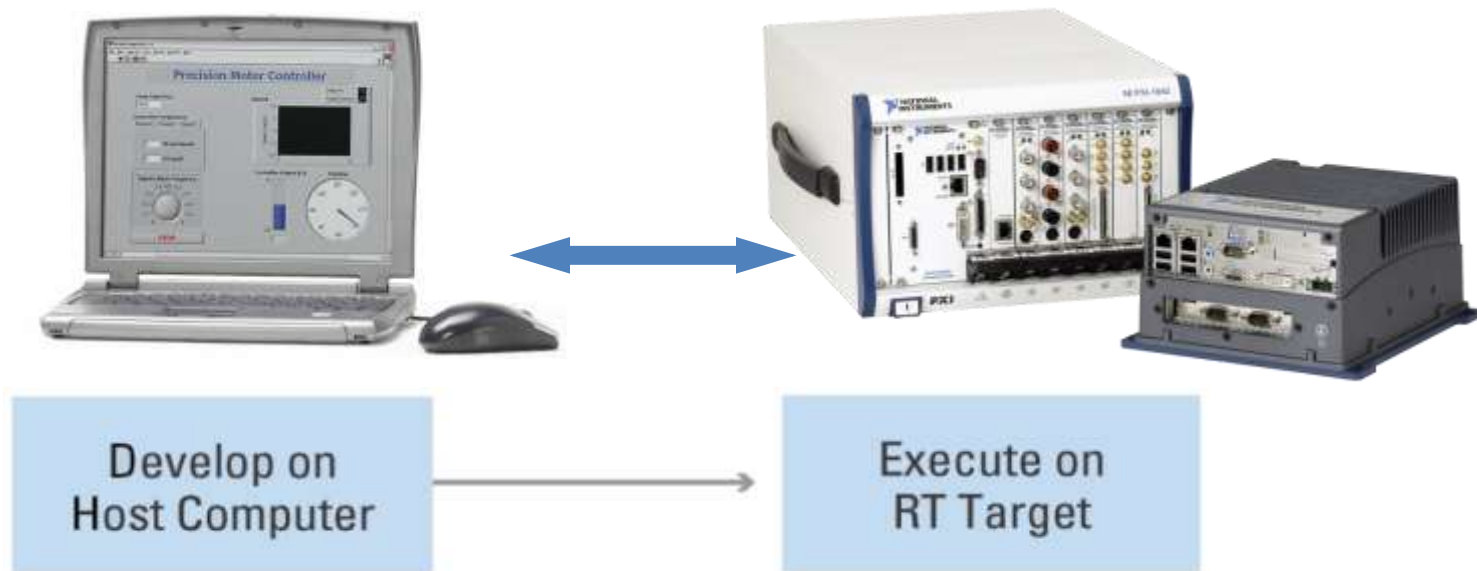
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LabVIEW Real-Time System Development



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LabVIEW RT Hypervisor



Develop on
Host Computer

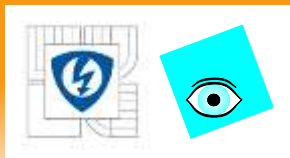
Windows XP



Execute on
RT Target

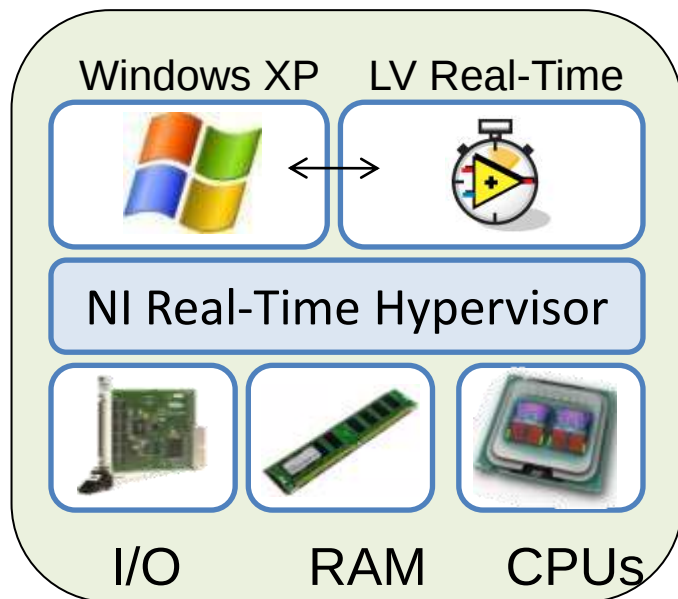
LV Real-Time





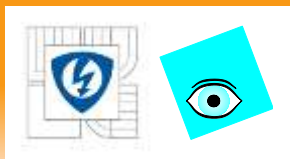
NI Real-Time Hypervisor

- Run LabVIEW Real-Time and Windows XP simultaneously
- Available on multicore PXI / PXIe and industrial controllers
- Uses virtualization technology and Intel-VT



Supported hardware:

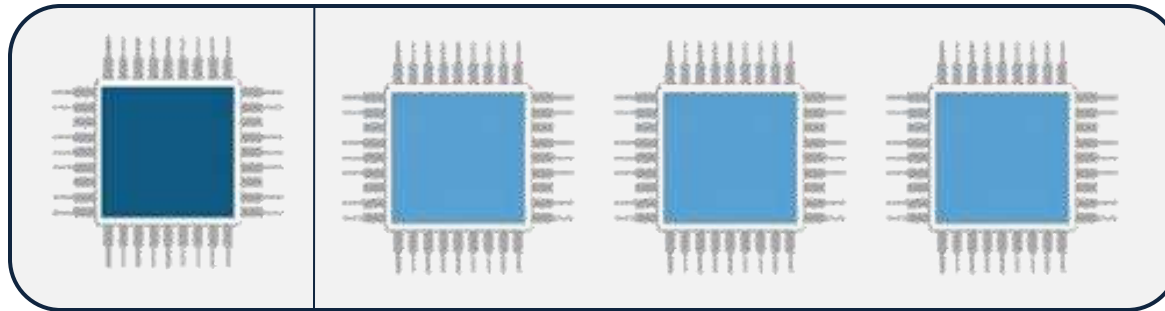
- PXI / PXIe 2-4 core controllers
- NI-3110 Industrial Controller



Benefits of the Real-Time Hypervisor

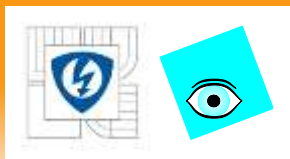
- **Efficiency:** take advantage of multicore processors effectively
- Custom distribution of computing power between RT and WIN
 - 1 : 3 or 2 : 2 or 3 : 1

Quad-Core Controller with Virtualization



Windows XP

LabVIEW Real-Time



Benefits of the Real-Time Hypervisor

- **Consolidation:** reduce hardware costs, wiring, and physical footprint
- **Capability:** make use of real-time processing and Windows XP services



Applications

Graphics

Services



Determinism

Real-Time I/O

Timing



PXI (PCI eXtensions for Instrumentation)

PXI Controller

- Embedded PC or remote PC interface
- Runs all standard software

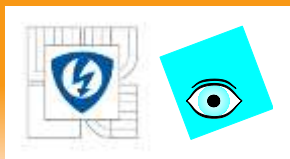
Chassis

PXI Backplane

- PCI bus
- Synchronization



Peripheral Slots



PXI Chassis

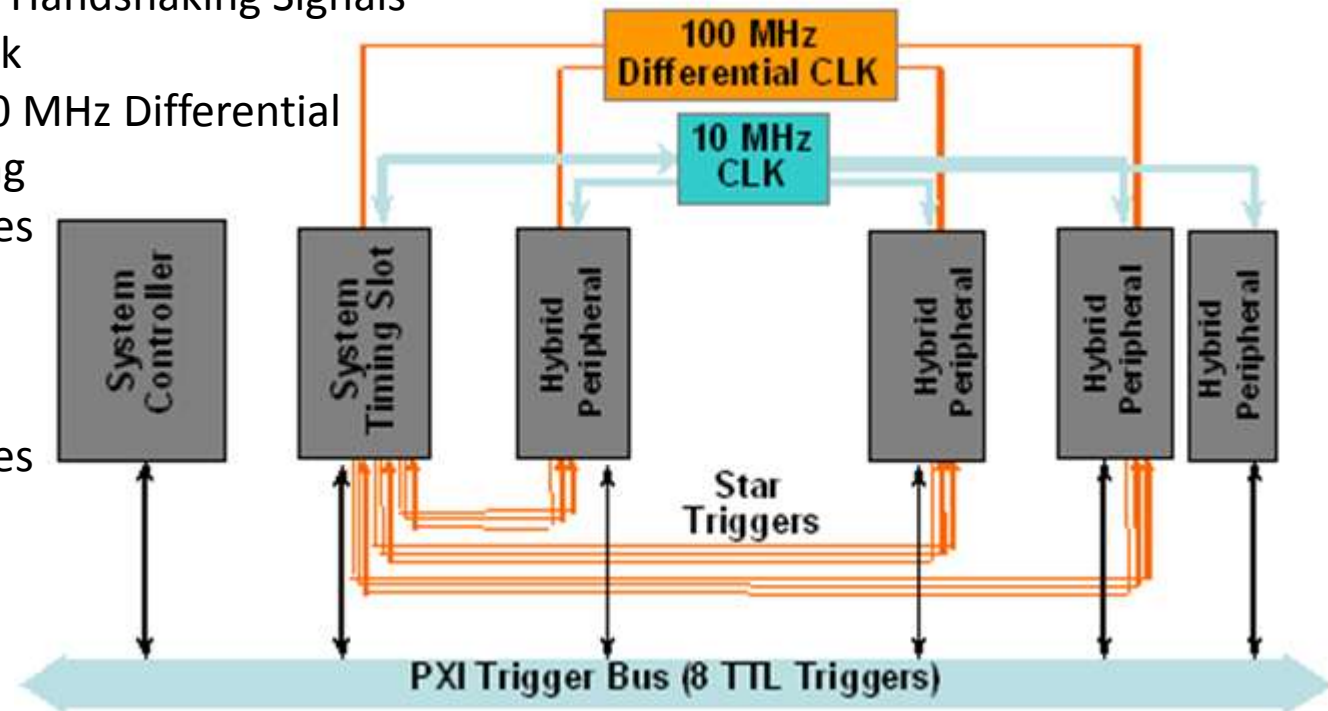
- 3U, 6U, and 3U/6U combo
- 4 through 26 slots
- Portable, benchtop, rack mount
- AC and DC power options
- Application specific
 - Ultra rugged, integrated signal conditioning, integrated LCD, etc.

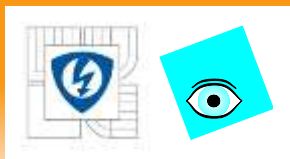




Timing and Synchronization Features of PXI

- PXI Trigger Bus
 - 8 TTL
 - Trigger, Clock, and Handshaking Signals
- System Reference Clock
 - 10 MHz TTL or 100 MHz Differential
 - Phase Lock Looping
 - Equal-Length Traces (< 200 ps skew)
- Star Trigger
 - Differential
 - Equal-Length Traces (< 150 ps Skew)





Embedded PXI System Controllers



General Purpose OSs

- Windows, Linux, etc.
- High performance
- Integrated peripherals
 - Gigabit Ethernet, USB 2.0, ExpressCard, etc.
- Ethernet / LAN control of PXI

Real-Time OSs

- LabVIEW Real-Time, VxWorks, etc.
- Determinism and reliability
- Headless operation





PXI Multiprocessing

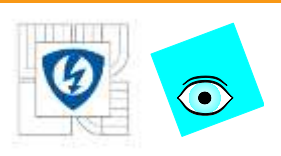


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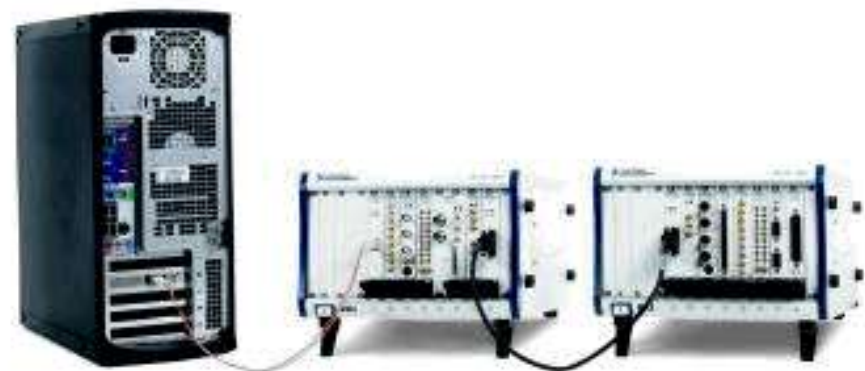


Remote PXI System Controllers



PC Control of PXI

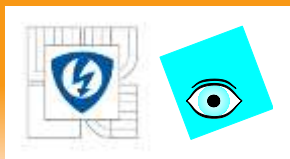
- Use latest high-performance PCs
- Build multichassis PXI systems



Laptop Control of PXI

- Control portable applications
- Use with DC-powered chassis for mobile systems





PXI Products...



Data Acquisition and Control

Multifunction I/O
 Analog Input/Output
 Digital I/O
 Counter/Timer
 FPGA/Reconfigurable I/O
 Machine Vision
 Motion Control
 Signal Conditioning
 Temperature
 Strain/Pressure/Force/Load
 Synchro/Resolver
 LVDT/RVDT
 Many More...



Modular Instrumentation

Digital Waveform Generator
 Digital Waveform Analyzer
 Digital Multimeter
 LCR Meter
 Oscilloscope/Digitizer
 Source/Signal Generator
 Switching
 RF Signal Generator
 RF Signal Analyzer
 RF Power Meter
 Frequency Counter
 Programmable Power Supply
 Many More...



Bus Interfaces

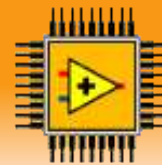
Ethernet, USB, FireWire
 SATA, ATA/IDE, SCSI
 GPIB
 CAN, DeviceNet
 Serial RS-232, RS-485
 VXI/VME
 Boundary Scan/JTAG
 MIL-STD-1553, ARINC
 PCMCIA/CardBus
 PMC
 Profibus
 LIN
 Many More...

Others

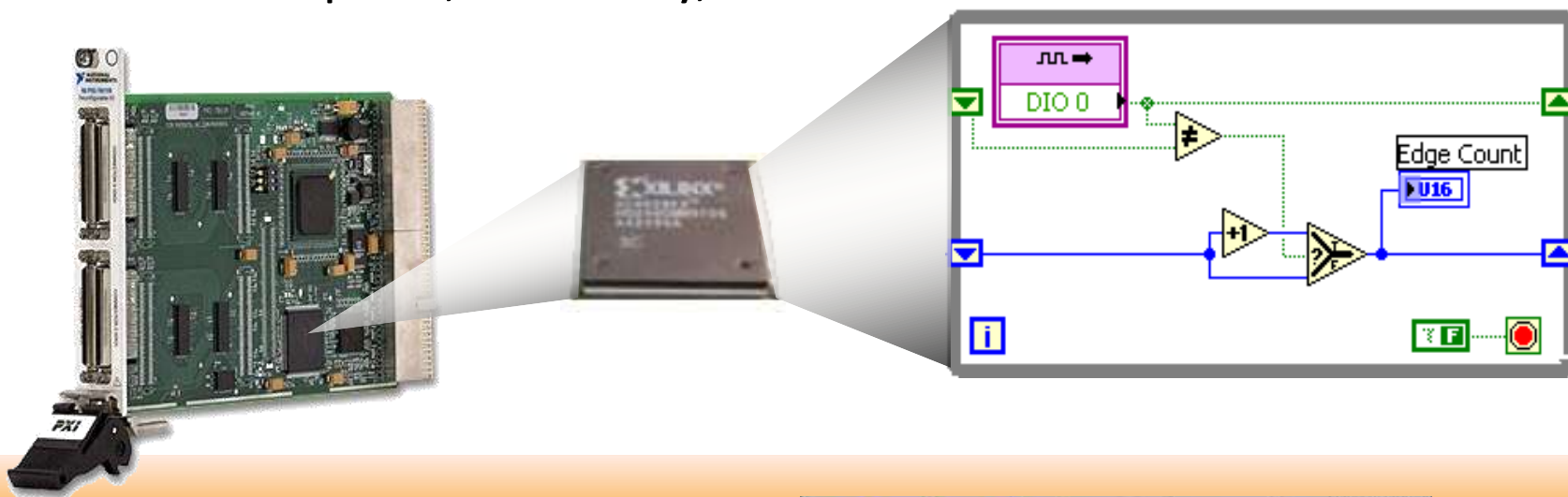
IRIG-B, GPS
 Direct-to-Disk
 Reflective Memory
 DSP
 Optical
 Resistance Simulator
 Fault Insertion
 Prototyping/Breadboard
 Graphics
 Audio
 Many More...

Over 1500 different modules from more than 70 manufacturers

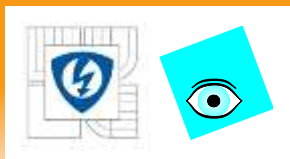
Reconfigurable IO FPGA



- Intuitive programming for both embedded engineers and domain experts
- High-speed timing and synchronization
- Custom digital protocols **User-defined COTS**
- In-line signal processing
- Hardware speed, reliability, and determinism

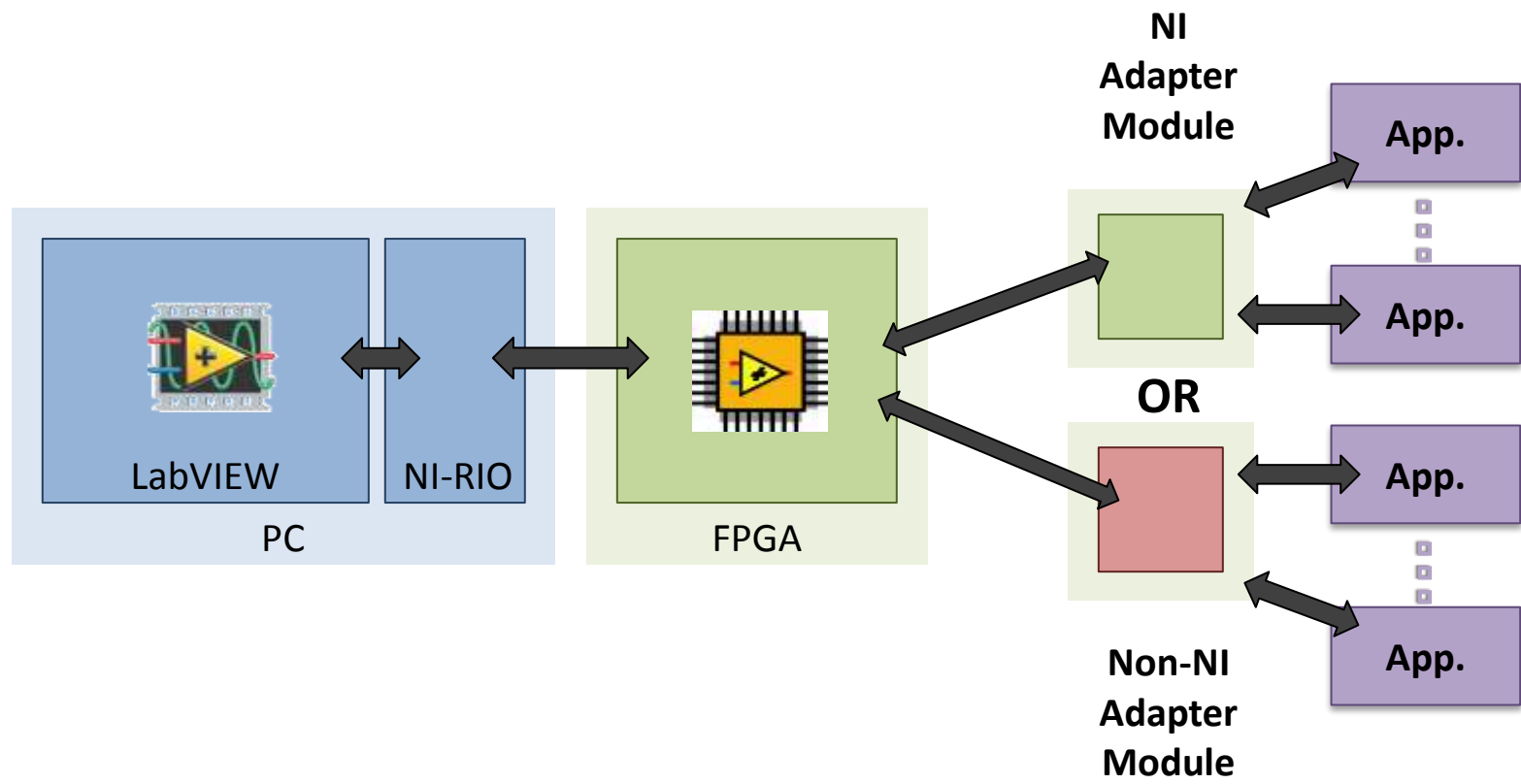


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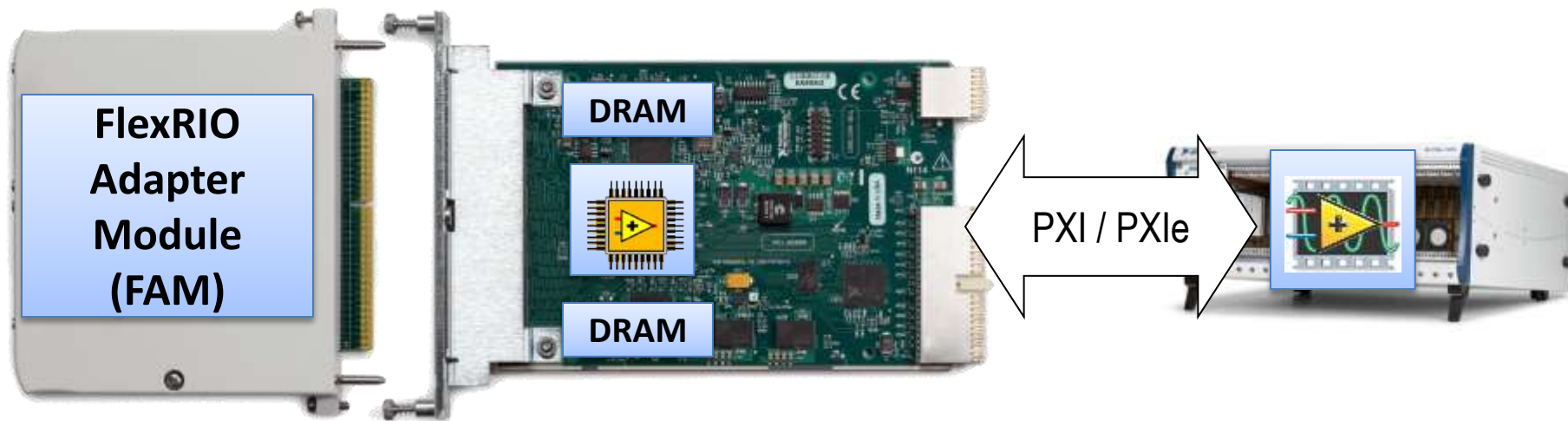


What is FlexRIO?

FlexRIO System Model



What's in the Box?



NI FlexRIO Adapter Module

- Interchangeable I/O
- Customizable by users
- Adapter Module Development Kit (MDK)

NI FlexRIO FPGA Module

- Virtex-5 FPGA
- 132 digital I/O lines
- 128 MB of DDR2 DRAM
- Adapter module power supplies and interface

PXI Platform

- Synchronization
- Clocking/triggers
- Power/cooling
- Data streaming

NI FlexRIO Adapter Modules



- Digital



**100 MHz
SE DIO**



**200 MHz
LVDS DIO**



**200 MHz
SE/LVDS DIO**



**Camera
Link**



**RS-
485/422**

- Analog



**2 ch. 100 MS/s
AI/AO**



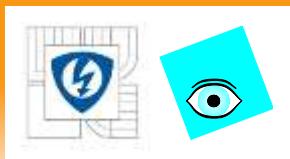
**32 ch. 50
MS/s
AI**



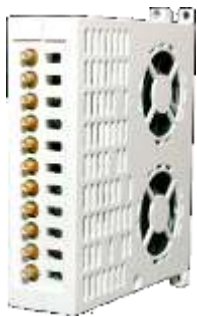
**4 ch. 250 MS/s
AI**



**16 ch. 50
MS/s
AI**



NI FlexRIO Partner Modules



**100 MHz
PPMU**



**Camera
Link and
GigE**



**MultiGigab
it optical**



**Dual
Gigabit
Ethernet**

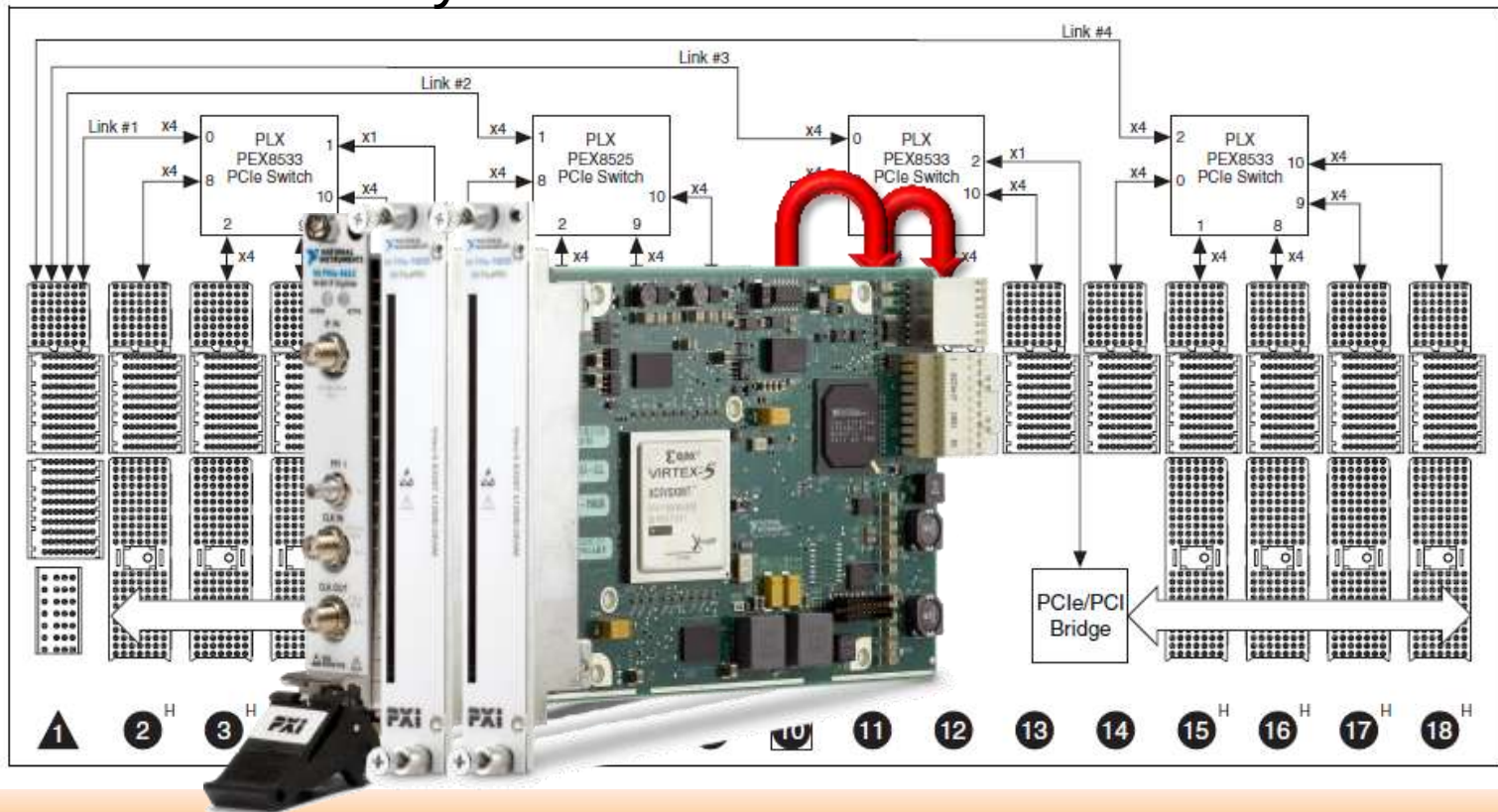


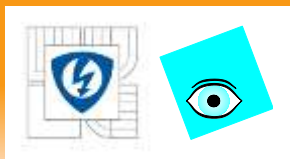
**Video and
Automotiv
e**



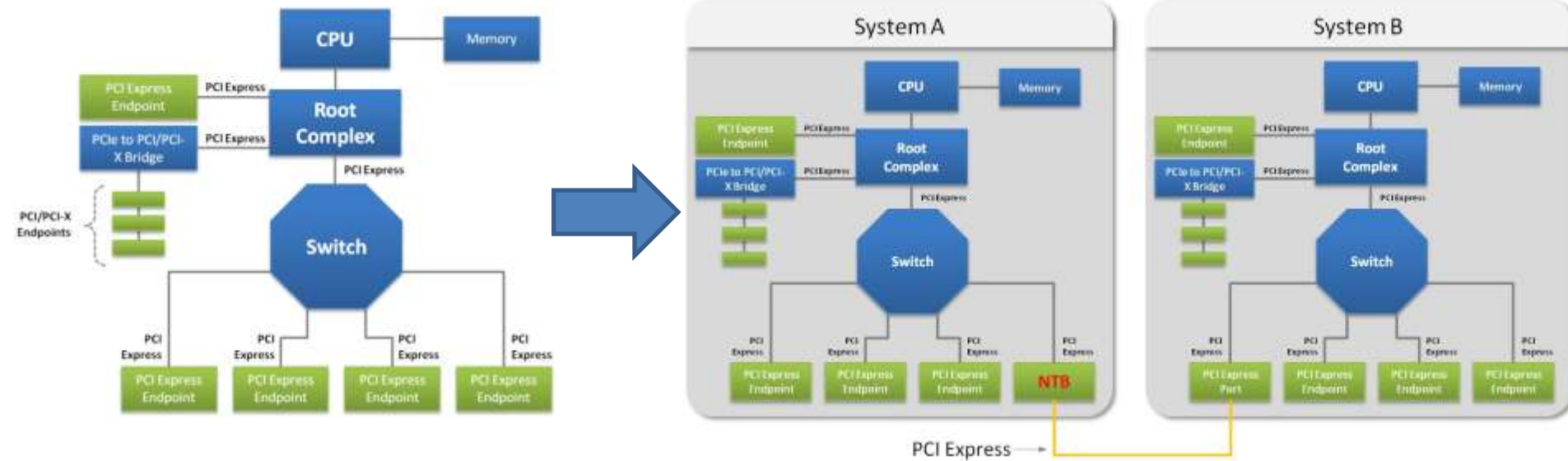
NI FlexRIO Peer-to-Peer Architecture

- >800 MB/s one-way
- >700 MB/s both ways
- ~10 us latency
- Up to 16 streams per FPGA

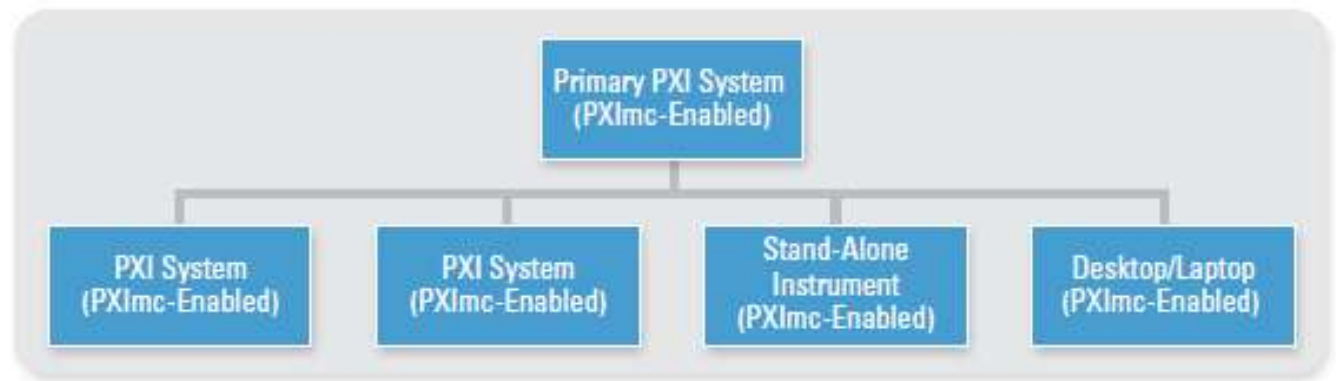


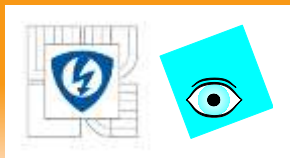


PXImc - High Performance Computing in PXIe



Where
extreme
computing
power is
required





PXImc - High Performance Computing in PXIe

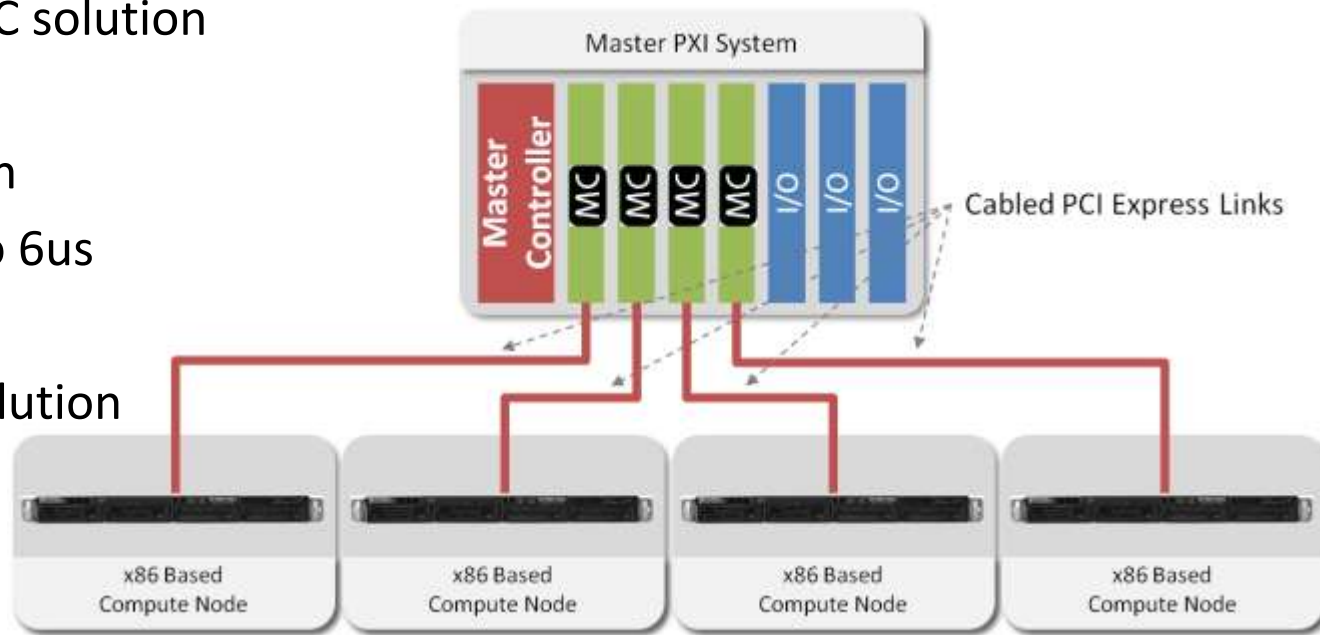
Example

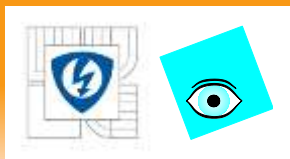
PXIe 1078 chassis HPC solution

- PCI x4 gen 1
- 1GB/s / direction
- Latency down to 6us

Gbit Ethernet HPC solution

- 100MB/s
- 600us latency
- 10x better data bandwidth
- 100x better data latency

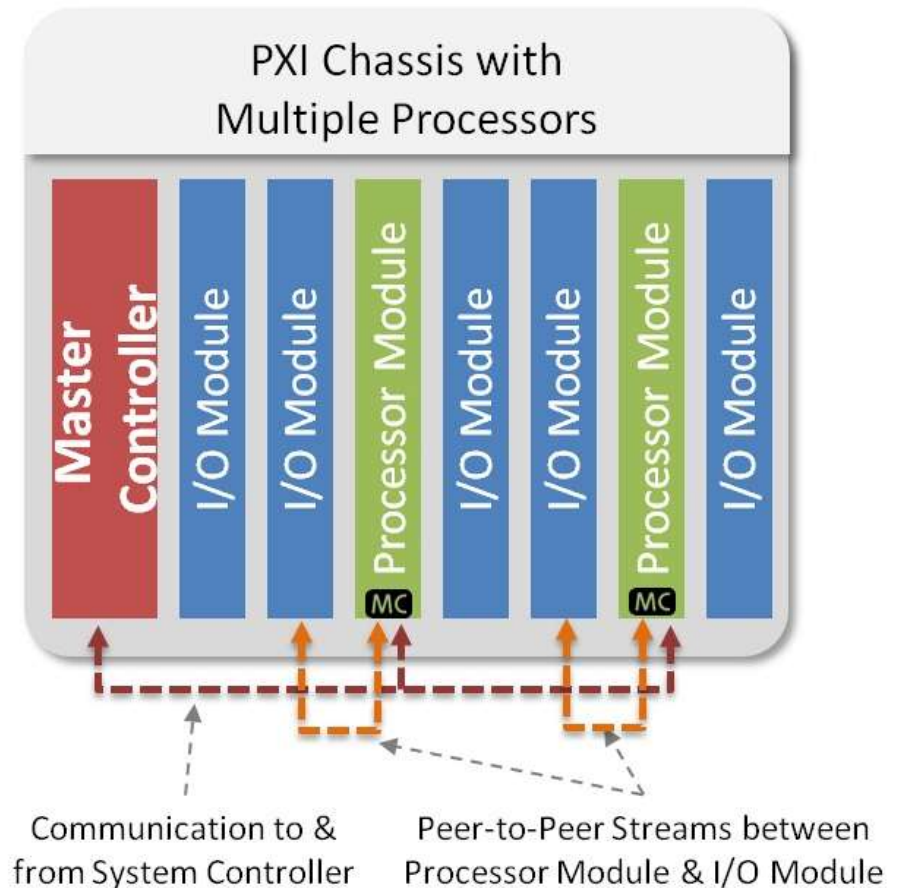




PXImc + Peer 2 peer technology

PXIe Peer2Peer

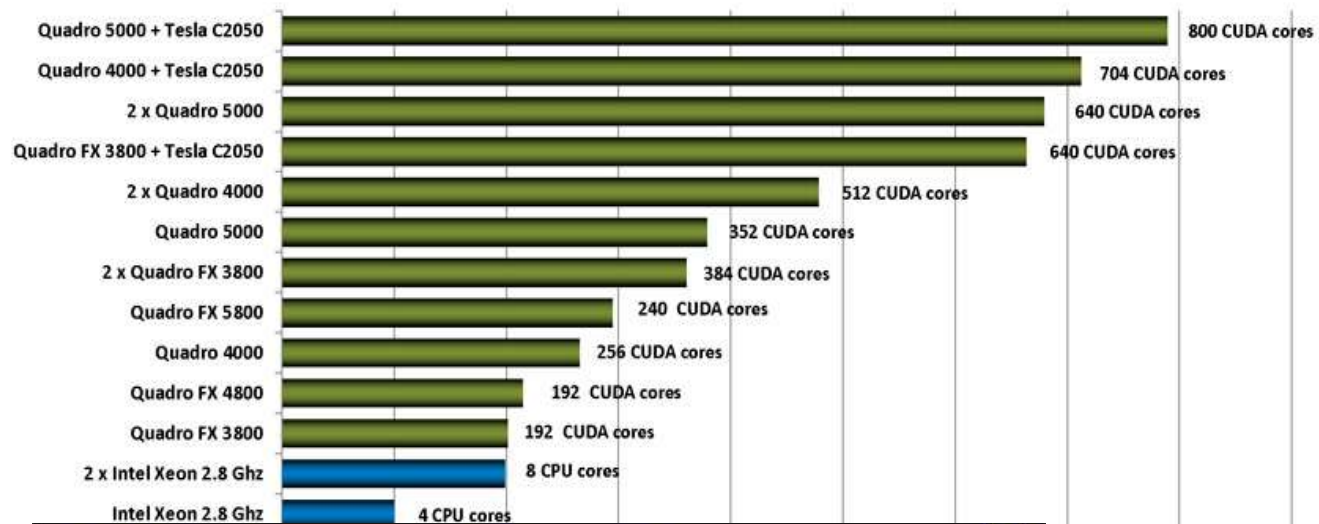
- Allows stream data between slots without passing data through controller
- PXImc + P2P allows high performance computing power for each I/O module





GPU computing – Why?

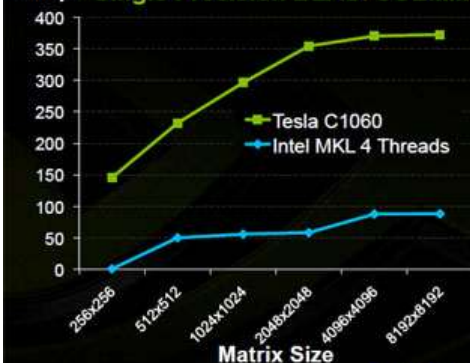
GPUs are for matrix
math intensive
application much
faster



BLAS Performance: CPU vs GPU

(Got Performance boost in CUDA 2.0)

Gflops Single Precision BLAS: SGEMM



Gflops Double Precision BLAS: DGEMM



CUBLAS: CUDA 2.2, Tesla C1060

MKL 10.0.3: Intel Core2 Extreme, 3.00GHz

NVIDIA Confidential: Under NDA only

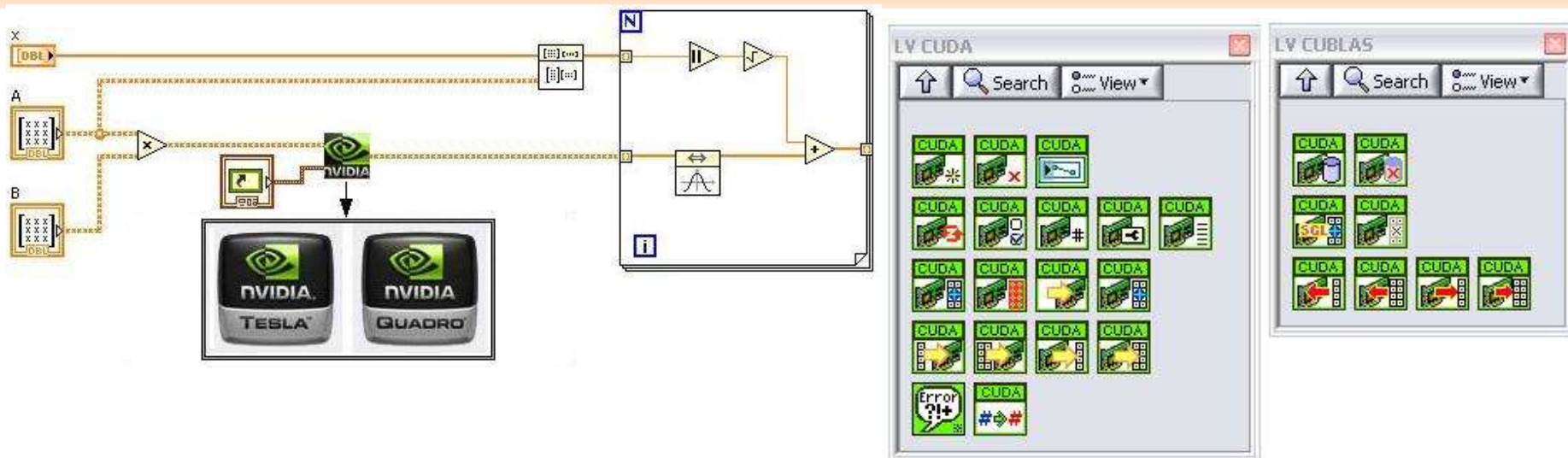
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GPU computing – How?



Runs on nVidia Quadro and Tesla GPUs

Search for “LabVIEW GPU Computing” on ni.com



CompactRIO

Real-Time OS

Up to 800 MHz PowerPC
Reliable embedded control,
analysis, and logging

Networked

Ethernet 10/100 BaseT.
embedded Web and file
servers; connectivity to
modems

Extreme Durability

-40 to 70 °C temperature range
50 G shock, Industrial
certifications

Small Size, Low Power Consumption

179.6 x 88.1 mm (7.07 x 3.47 in)
11 to 30 VDC power, 17 W max (7-10 W typ.)

Reconfigurable FPGA Circuitry

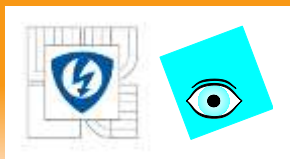
Custom hardware reliability; flexible
timing, triggering, synchronization



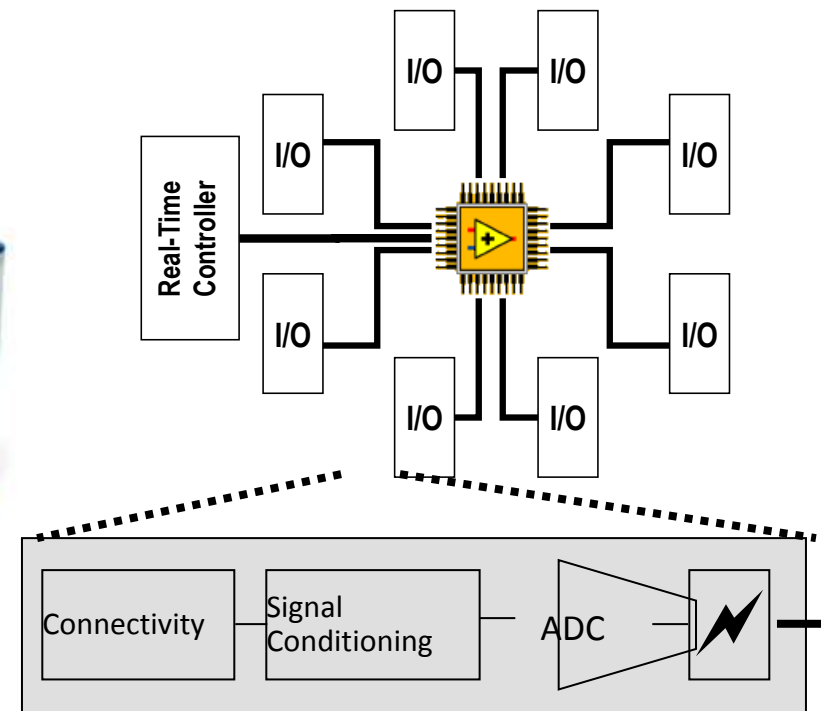
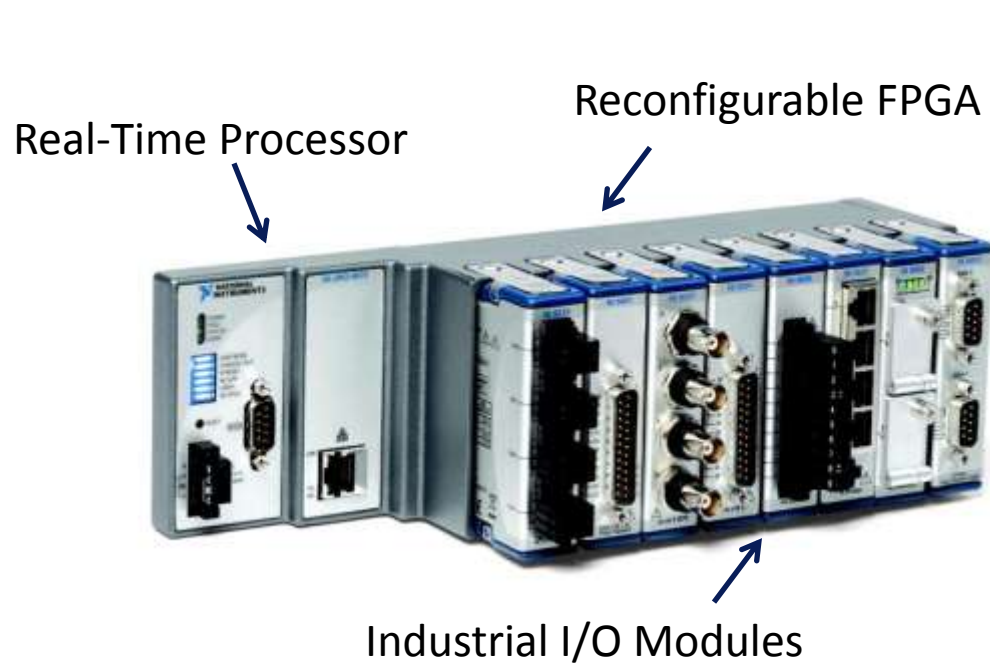
Measurement I/O Modules

Isolated, industrial and high-precision options

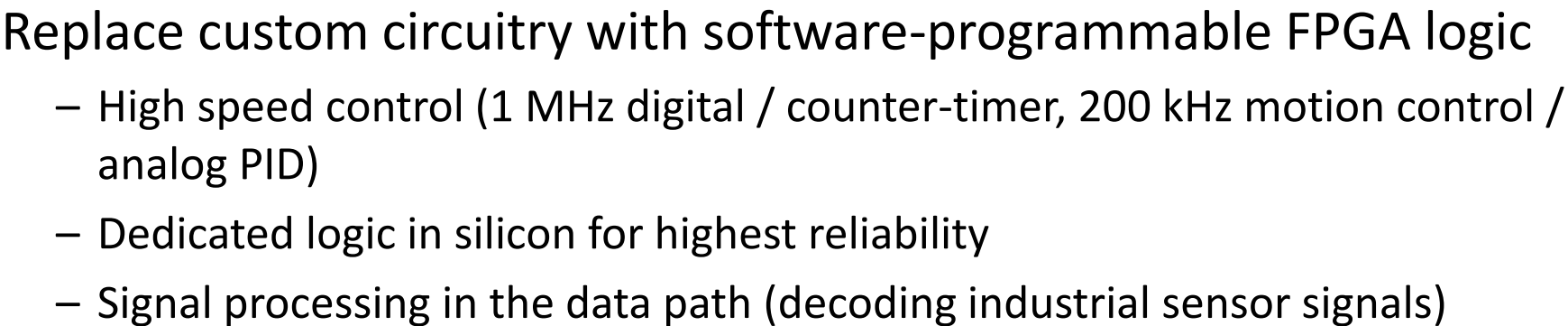
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NI CompactRIO Embedded System Architecture



- Industrial I/O Modules with built-in signal conditioning for direct connection to industrial sensors/actuators
- Reconfigurable FPGA for high-speed and custom I/O timing, triggering, processing, control
- Real-Time Processor for deterministic, stand-alone operation and advanced analysis

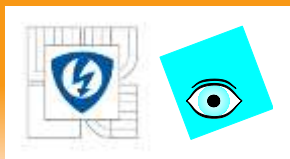




High precision Industrial grade I/O for Control Design

- ✓ Analog I/O
 - ✓ Up to 24 bit
 - ✓ Up to 1MSa/s
 - ✓ Built in excitation
- ✓ Digital I/O
 - ✓ LVTTL to 250V
 - ✓ Up to 30MHz
- ✓ Accelerometer
- ✓ Strain Gauge
- ✓ Load Cells
- ✓ Digital I/O
- ✓ Thermocouples
- ✓ 4 to 20mA
- ✓ RTD
- ✓ High Voltage (+/-400V or 300Vrms)
- ✓ High Current (10Amps)
- ✓ Servo and stepper drive motion
- ✓ CAN, Serial, custom communication
- ✓ Relay
- ✓ Pulse generation
- ✓ TEDS
- ✓ Quadrature encoders and counters

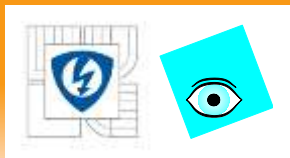




Benefits of CompactRIO

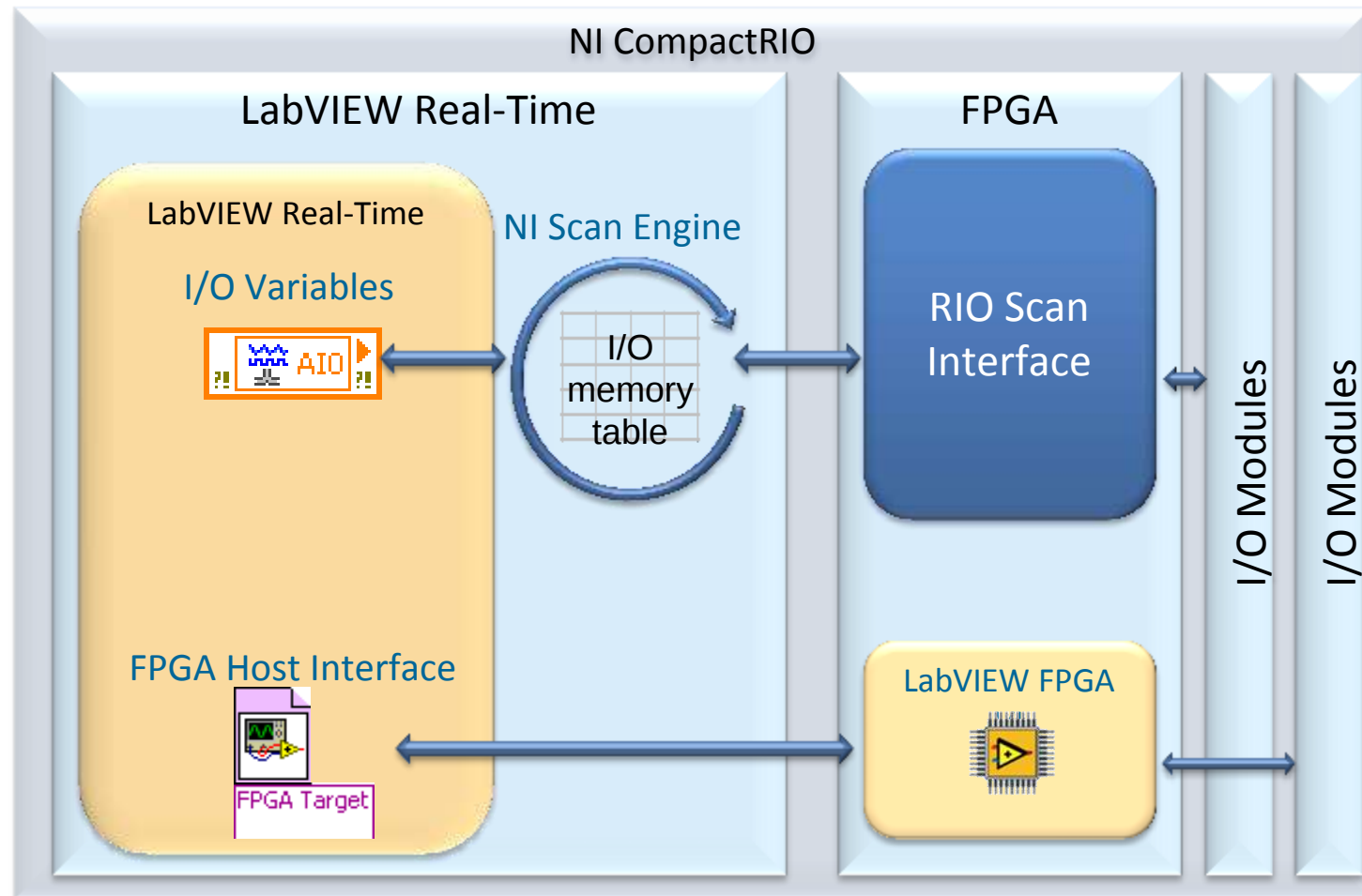
- Reconfigurable FPGA – great versatility
- Widely used in different industries
- Open Embedded System
- High performance
- Extreme Ruggedness
- Connectivity
- High academic discounts





Programming CompactRIO

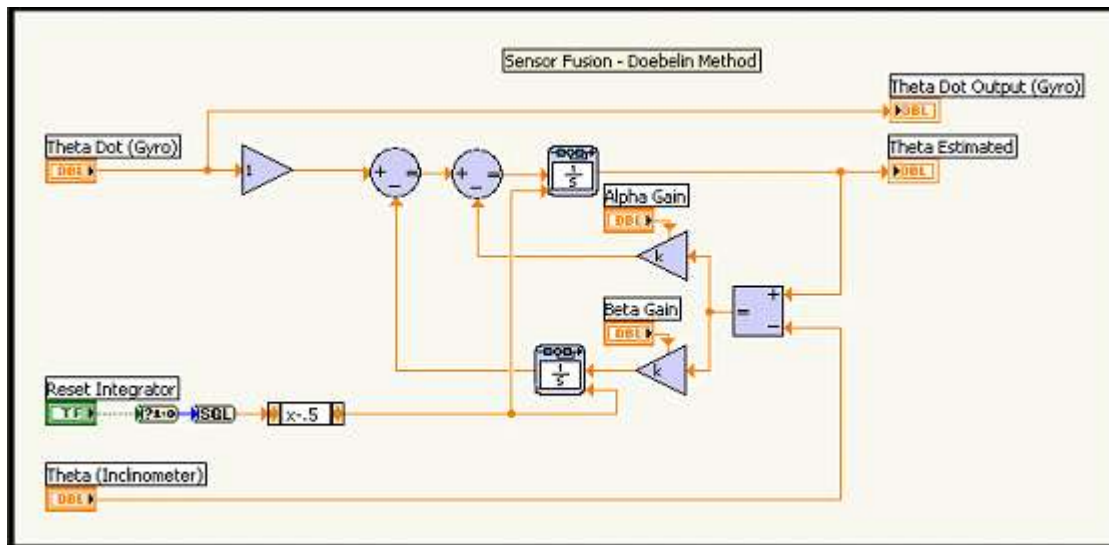
ScanEngine and LabVIEW FPGA

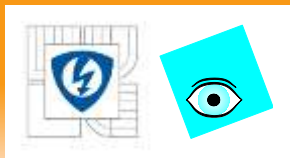




RPI Human Object Transporter

- Professor Kevin Craig, Rensselaer Polytechnic Institute (RPI)
- LabVIEW Simulation Module, CompactRIO, LabVIEW Real-Time, LabVIEW PDA
- Team of undergrads completed project in 4 months!





MXI CompactRIO

High Channel Count C-Series I/O

- 14 slots per chassis
- Up to 6 chassis per daisy chain
- Up to 8 daisy chains per controller

Best-in-Class FPGA

- NI 9157: Virtex5 LX85
- NI 9159: Virtex5 LX110

High-Throughput Cabled PCI-express x1 Connection

- 250MB/s theoretical throughput (20x EtherCAT or Ethernet)
- Connect to high performance PXI, PC, rack-mount, or industrial controllers
- Up to 7m cable length between chassis



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NI 31x0 Industrial Controller

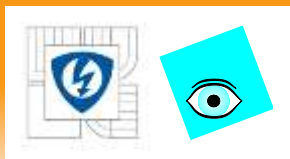
- The NI 3110 features an Intel SL9JT L2400 1.66 GHz Core Duo Processor
- The NI 3100 features an Intel 1.06 GHz Celeron M 423 processor
- Both controllers are configured with the Windows XP or RT operating system
- NI 3110 supports RT Hypervisor
- Controllers can be used as an interface to control remote I/O with hardware such as NI CompactDAQ, NI PXI, and NI plug-and-play PCI and PCI Express devices

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NI Single-Board RIO Embedded Device

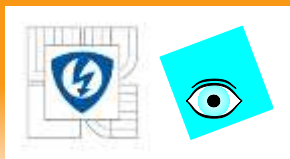
- Single-Board Computer based on CompactRIO
 - Real-Time OS, Reconfigurable FPGA, uses C Series I/O Modules
- Several I/O modules included onboard (DIO, AI, AO, 24V DI & DO)
- Ideal for high-volume and OEM applications



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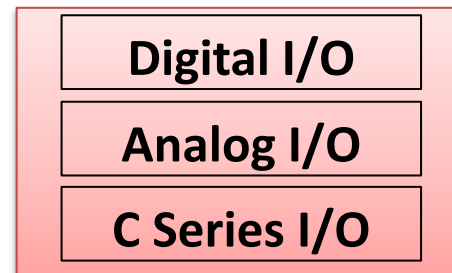
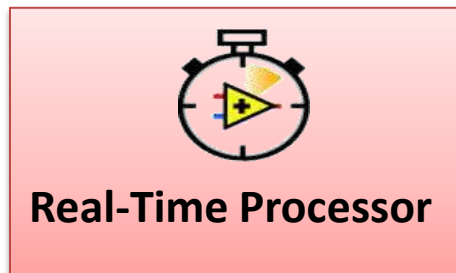
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



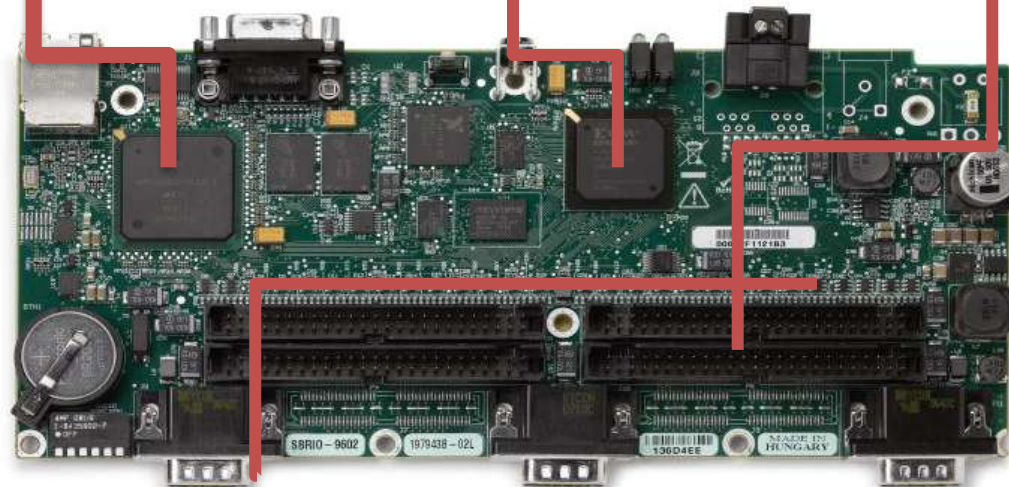


NI Single-Board RIO Platform

“The power of CompactRIO on a single board.”



9.4 – 14.22 cm



20.83 cm

Up to:

- 400MHz Processor Speed
- 32 AI Channels
- 4 AO Channels

ni.com/singleboard



Single-Board RIO Variants

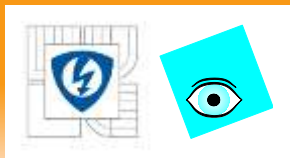


Model	Processor Speed (MHz)	FPGA Size (Gates)	3.3V DIO Lines	AI Channels	AO Channels	24V DIO Lines	C Series Expansion (Slots)	Size (Inches)
sbRIO-9601	266	1M	110	0	0	0	3	8.2x3.7
sbRIO-9602	400	2M	110	0	0	0	3	8.2x3.7
sbRIO-9611	266	1M	110	32	0	0	3	8.2x5.6
sbRIO-9612	400	2M	110	32	0	0	3	8.2x5.6
sbRIO-9631	266	1M	110	32	4	0	3	8.2x5.6
sbRIO-9632	400	2M	110	32	4	0	3	8.2x5.6
sbRIO-9641	266	1M	110	32	4	32/32	3	8.2x5.6
sbRIO-9642	400	2M	110	32	4	32/32	3	8.2x5.6

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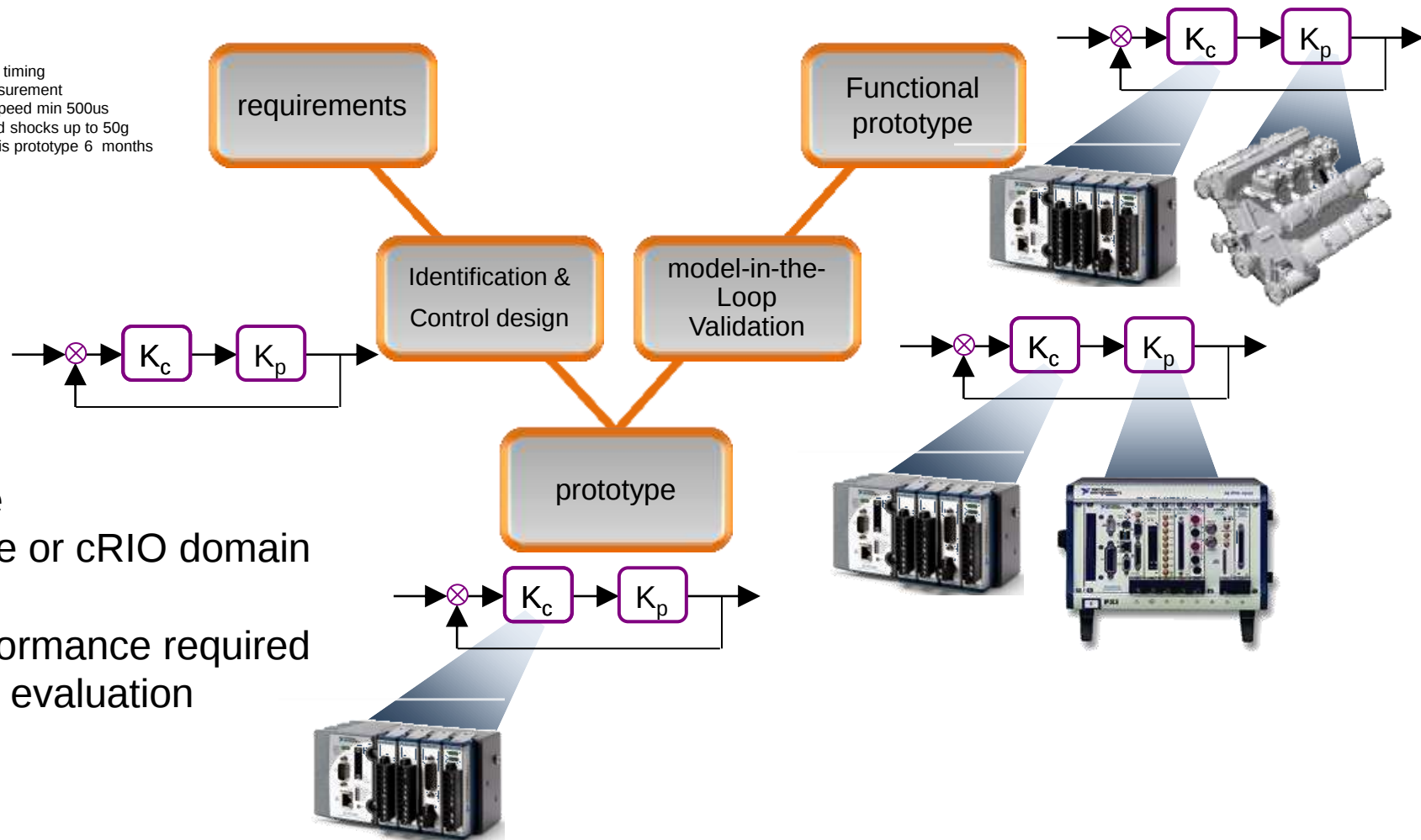
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Prototyping V diagram

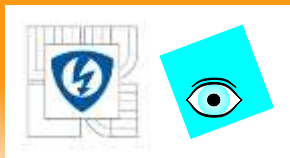
Gas Engine
Variable valve timing
Vibration measurement
Control loop speed min 500us
Must withstand shocks up to 50g
deadline to finish prototype 6 months



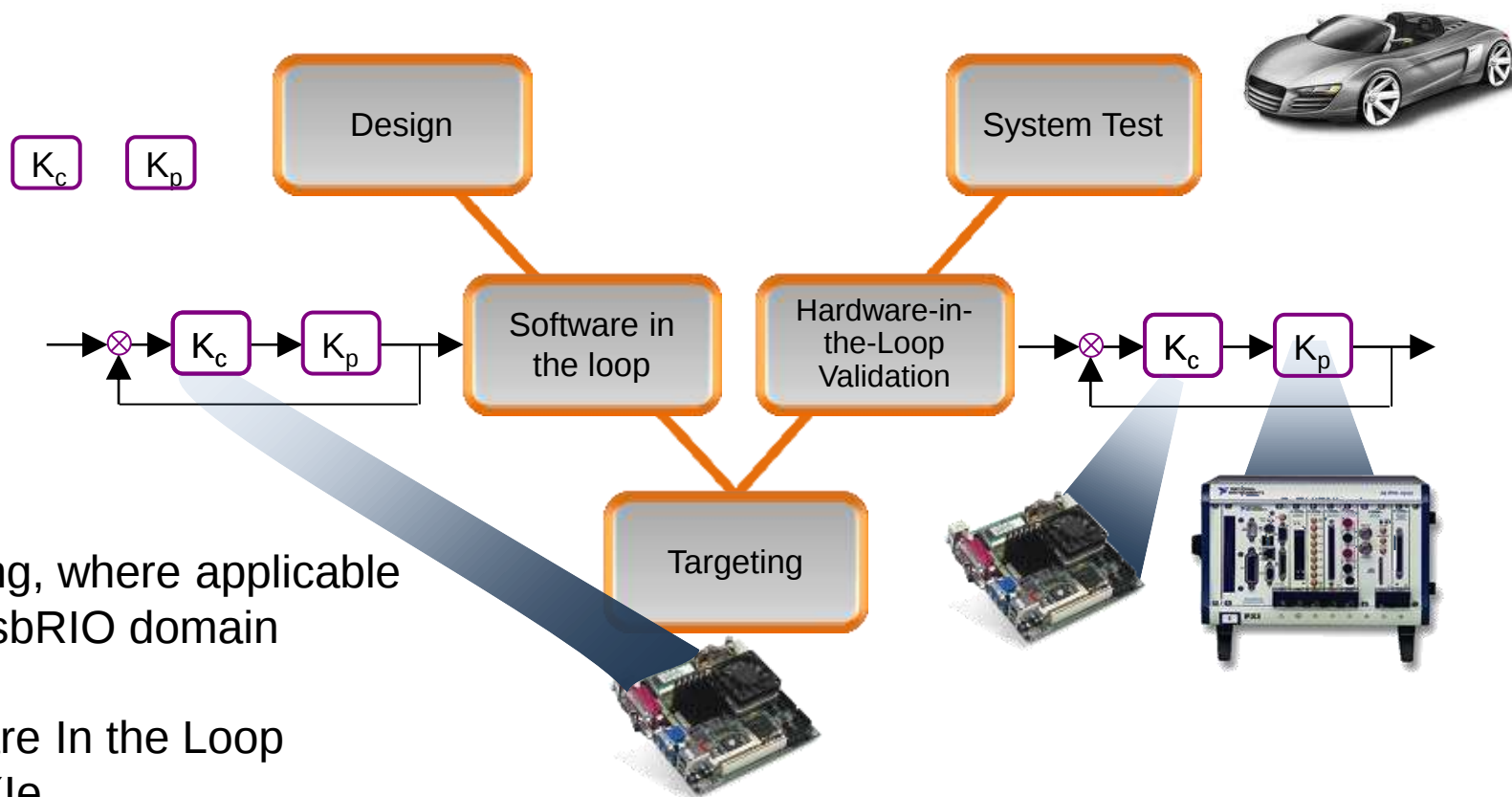
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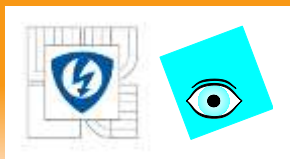
Target deployment V Diagram



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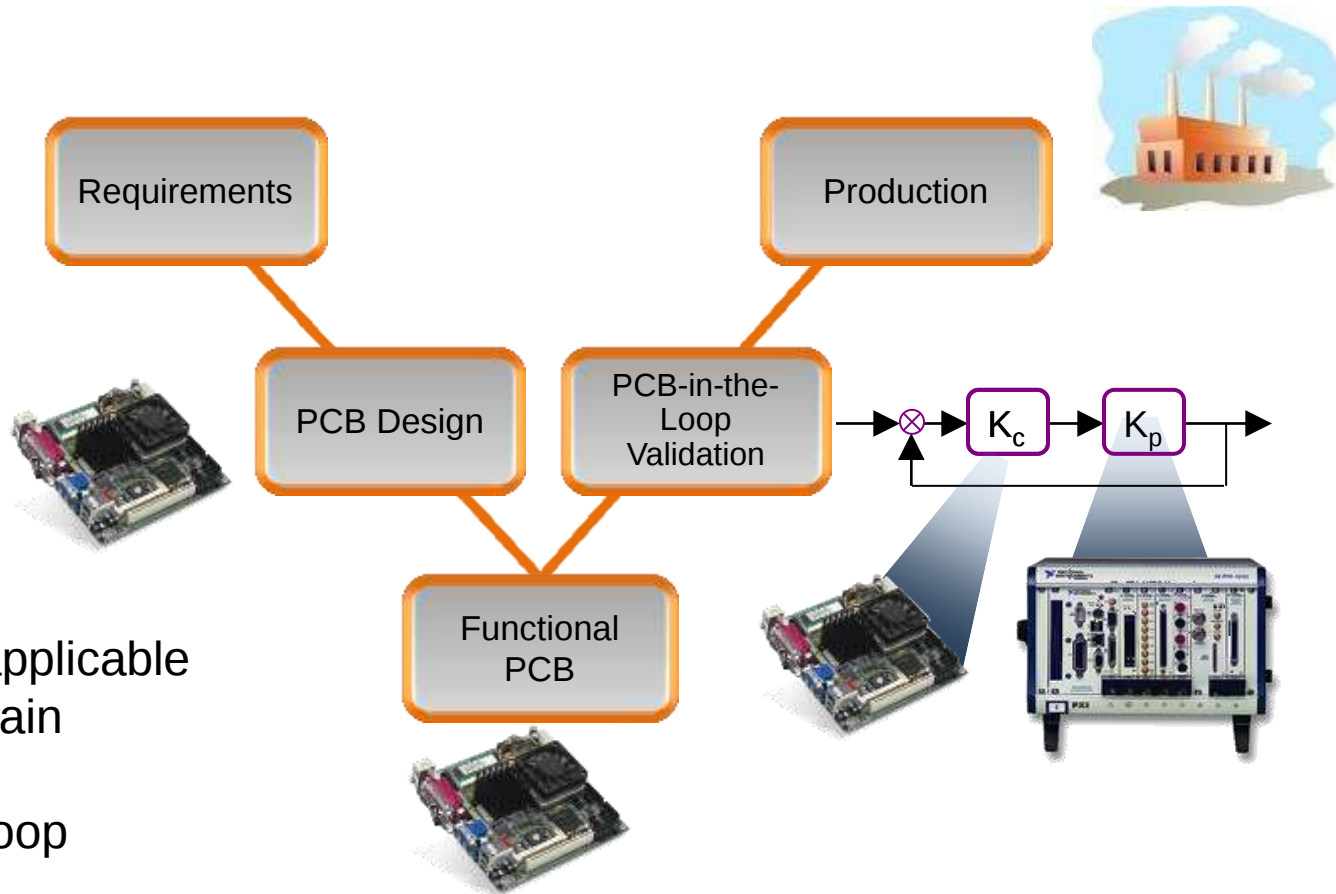




Manufacturing V diagram

Based on uP architecture
All tantal capacitor design
Control loop speed min 500us
Must withstand shocks up to 50g
deadline to finish production 6 months

K_c



Targeting, where applicable
cRIO / sbRIO domain

Hardware In the Loop
PXI/ PXIe