

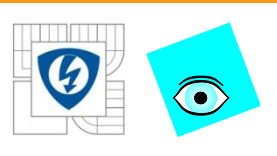
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

Návrh, simulace a ověření elektronických obvodů na platformě NI ELVIS a Multisim

Ing. Roman Vala (National Instruments)

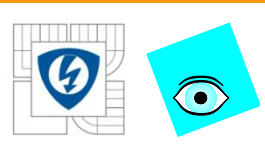
13. dubna 2012

Tato prezentace je spolufinancována Evropským sociálním fondem a státním rozpočtem České republiky.

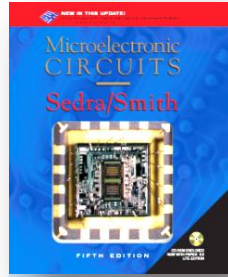


Agenda

- Úvod
- NI ELVIS II a NI MyDAQ
- Multisim
- Propojení s LabVIEW

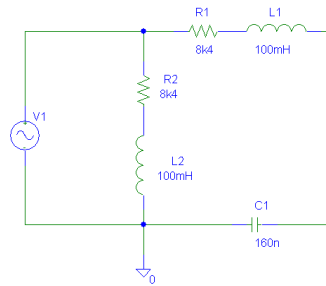


Traditionally...

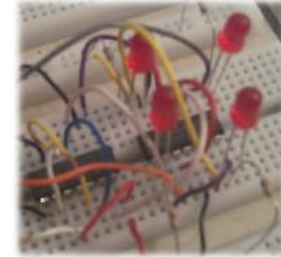


Textbooks

Classroom



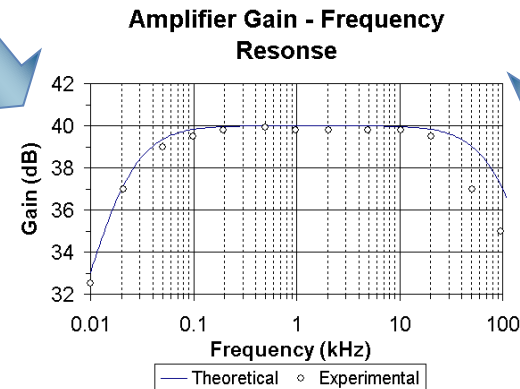
Simulation

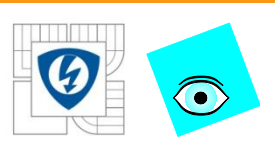


Hardware

Laboratory

Comparing simulated data
with measurements





PC-Based Electronic Circuit design

“We have never really, as educators, gotten these three elements [of theory, simulation, and experimentation] to work together well. The weakest has been the laboratory. With the advances in simulation with [NI] Multisim and the advances in experimentation with [NI] myDAQ, we'll be able to bring all of these elements together in a more exciting way.”

- Adel Sedra, Dean and Professor of Engineering at University of Waterloo



<http://www.ni.com/academic/circuits.htm>

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STANFORD
UNIVERSITY

UNIVERSITY OF
LIVERPOOL

VirginiaTech
Invent the Future



Massachusetts
Institute of
Technology

UNIVERSITÄT
SALZBURG



Pennsylvania College
of Technology



UtahState
UNIVERSITY



northumbria
UNIVERSITY



SINGAPORE
POLYTECHNIC



Georgia
Tech



McGill



東京大学
THE UNIVERSITY OF TOKYO

PURDUE
UNIVERSITY



Used Worldwide



DeVry
University



KOREA
UNIVERSITY



TECHNISCHE
UNIVERSITÄT
DRESDEN



National University
of Singapore



THE HONG KONG
POLYTECHNIC UNIVERSITY
香港理工大學



NANYANG
TECHNOLOGICAL
UNIVERSITY

THE UNIVERSITY OF
NEW SOUTH WALES

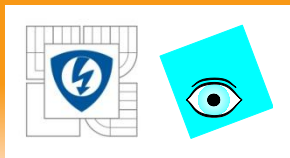


Imperial College
London



UNIVERSITY OF HOUSTON
CULLEN COLLEGE OF ENGINEERING





National Instruments

Offering graphical system design solutions for Test and Measurement and Industrial Embedded

Non-GAAP Revenue: \$1.04B revenue in 2011, \$280M revenue in Q4 2011

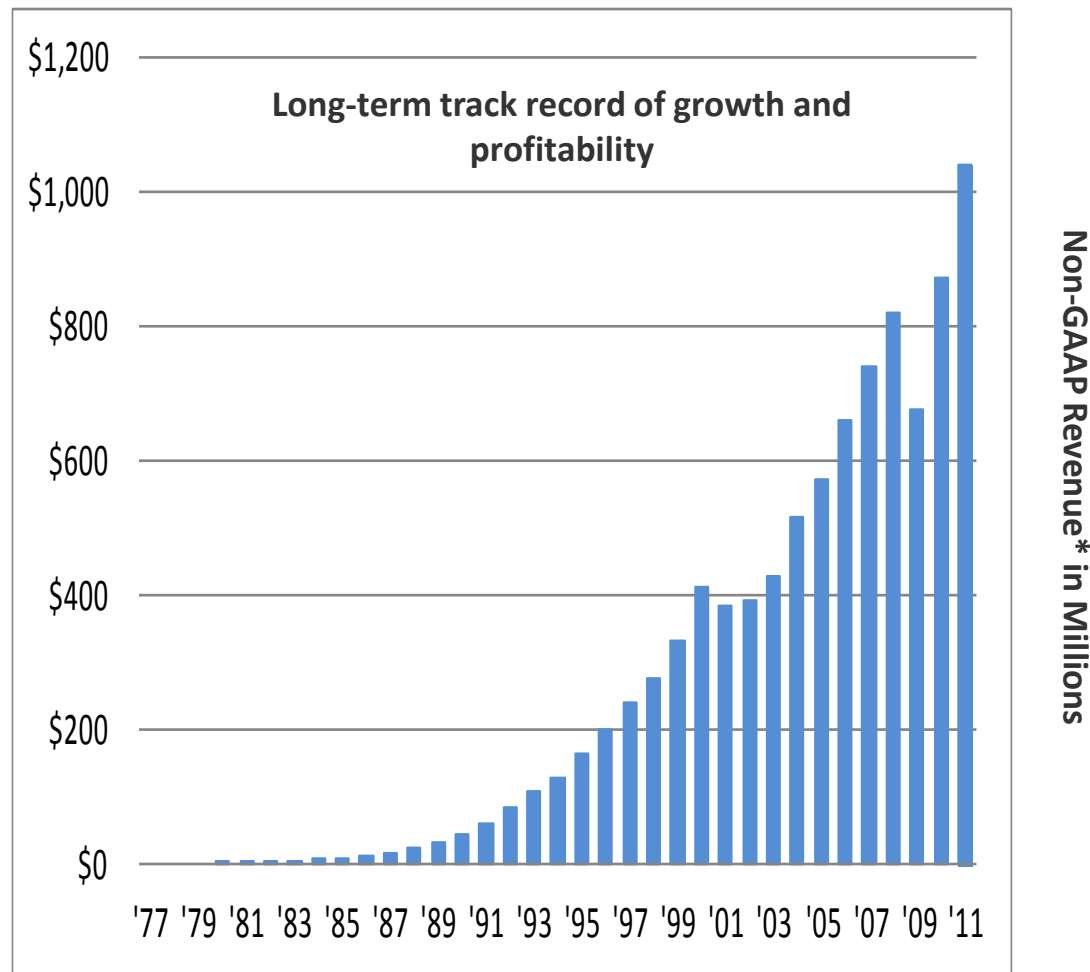
Global Operations: Approximately 6,200 employees; operations in more than 40 countries

Broad customer base: More than 35,000 companies served annually

Diversity: No industry >15% of revenue

Culture: Ranked among top 25 companies to work for worldwide by *FORTUNE* Magazine and the Great Places to Work Institute

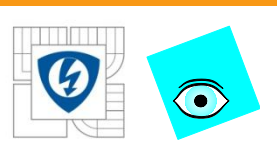
Strong Cash Position: Cash and short-term investments of \$366M at December 31, 2011



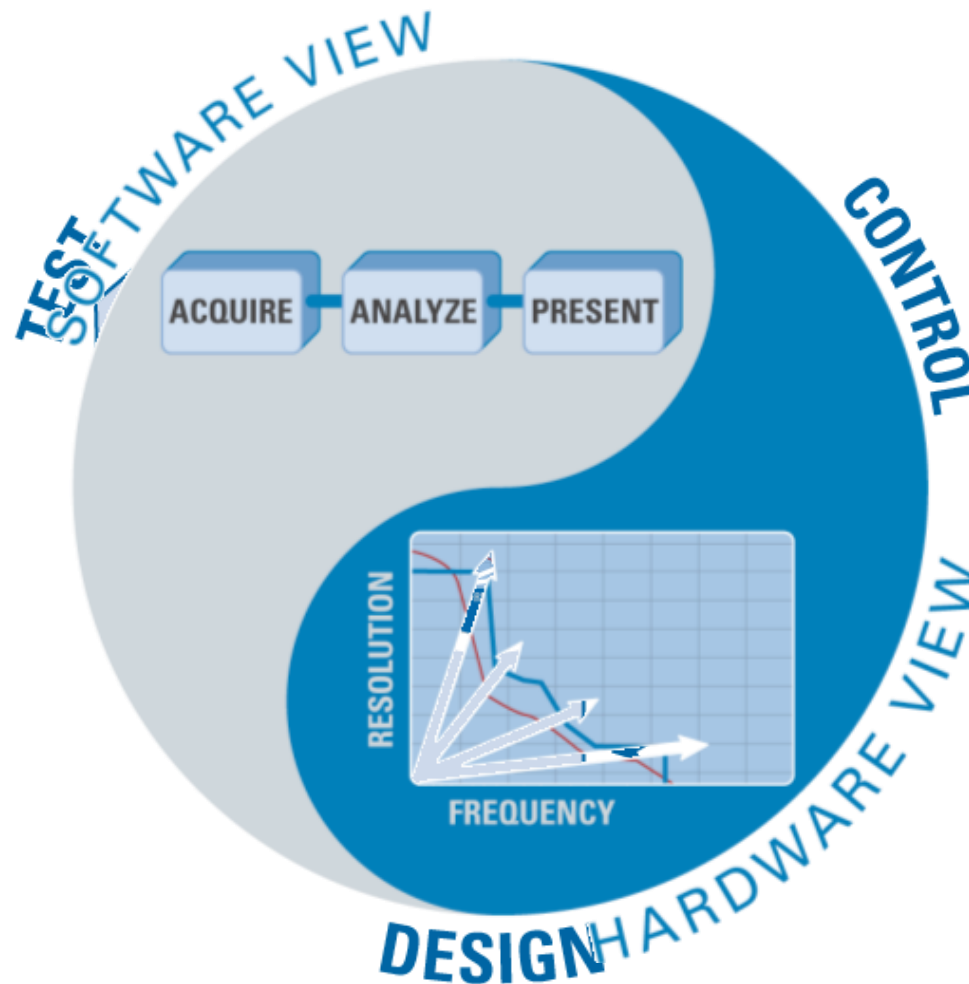
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INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





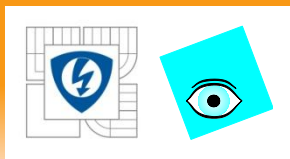
What is Virtual Instrumentation?



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INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

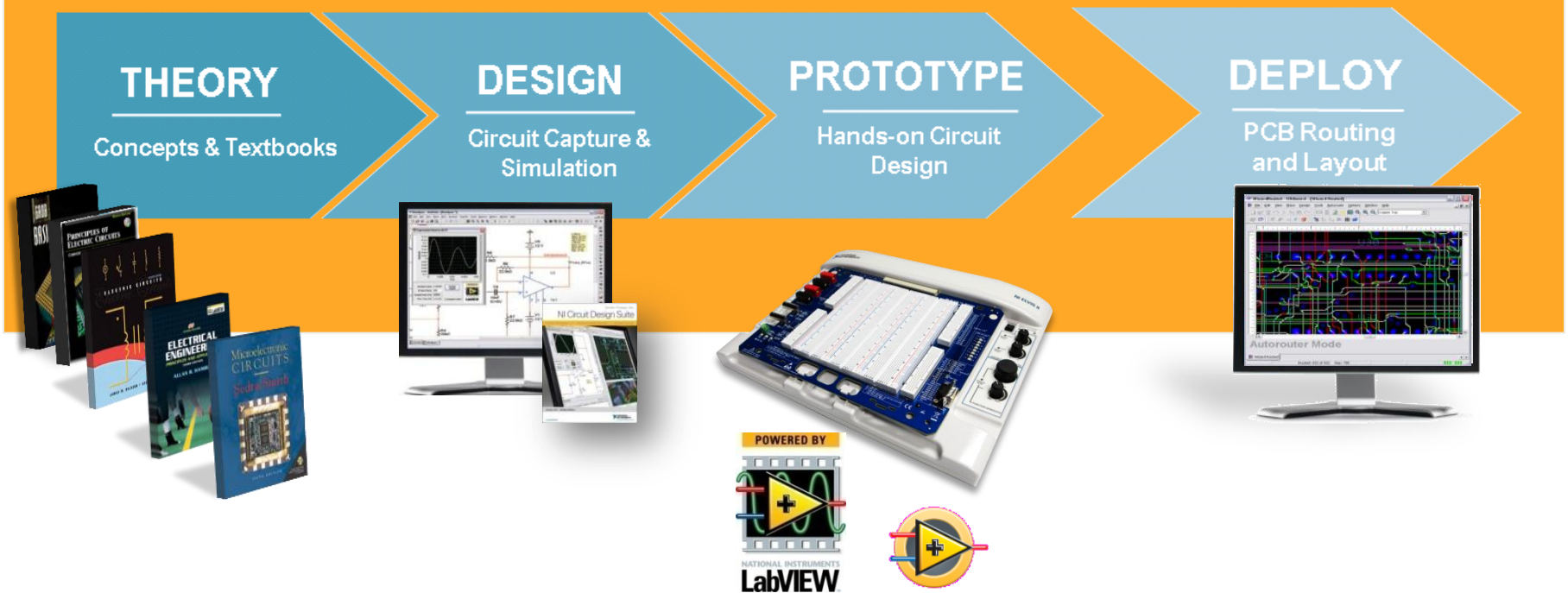




NI Electronics Education Platform

National Instruments tools address challenges of circuit education

Electronics Education Platform



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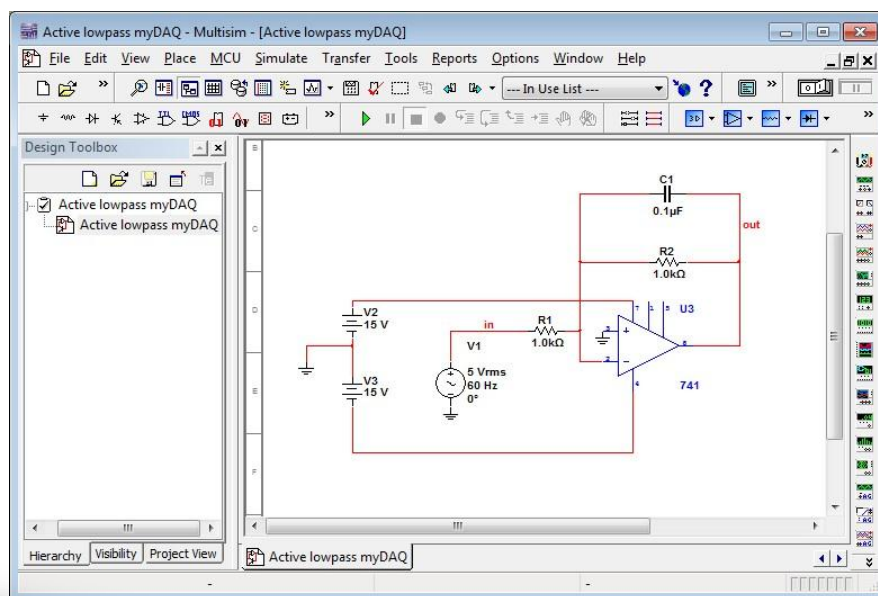




Necessary Equipment



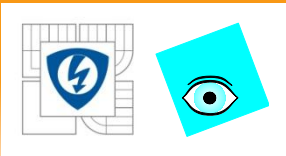
Multisim



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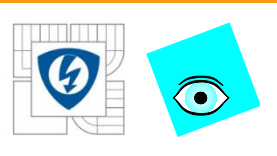


ELVIS HW

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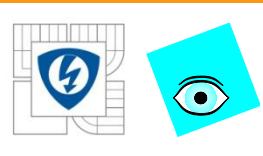
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Agenda

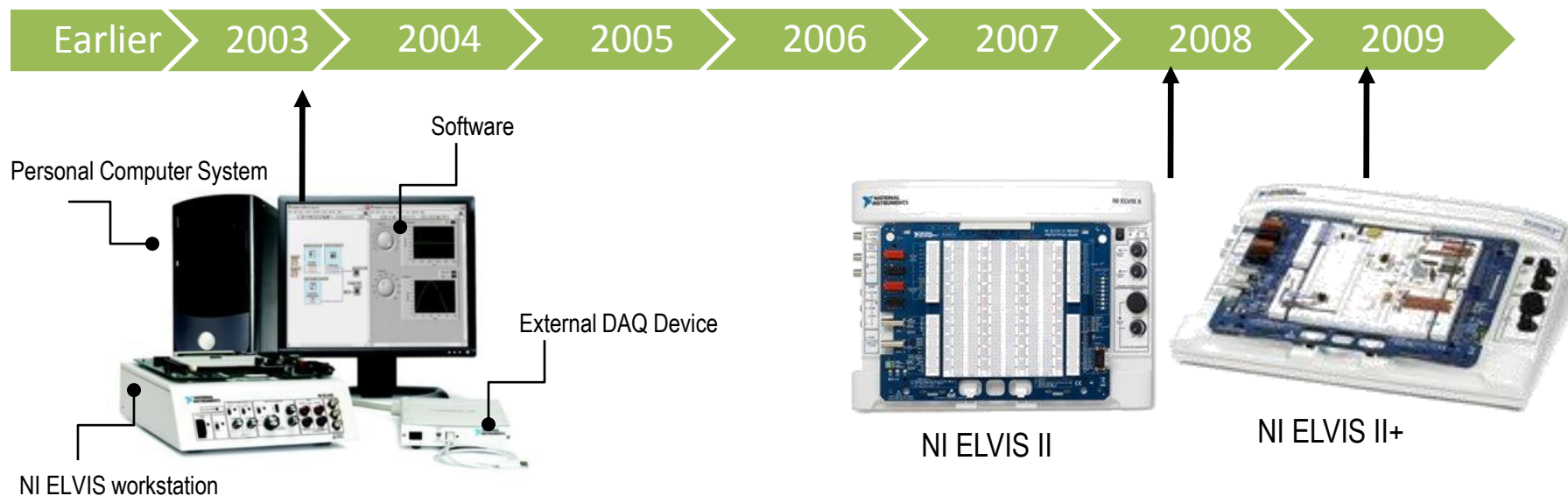
- ELVIS – Electronic Laboratory for Virtual Instrumentation
- ELVIS addons
- MyDAQ



Introduction | From concept to reality

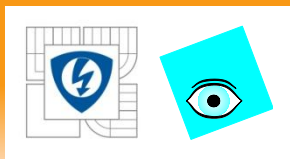


- LabVIEW / DAQ based system
- Removable prototyping board
- Integrated instrument capability



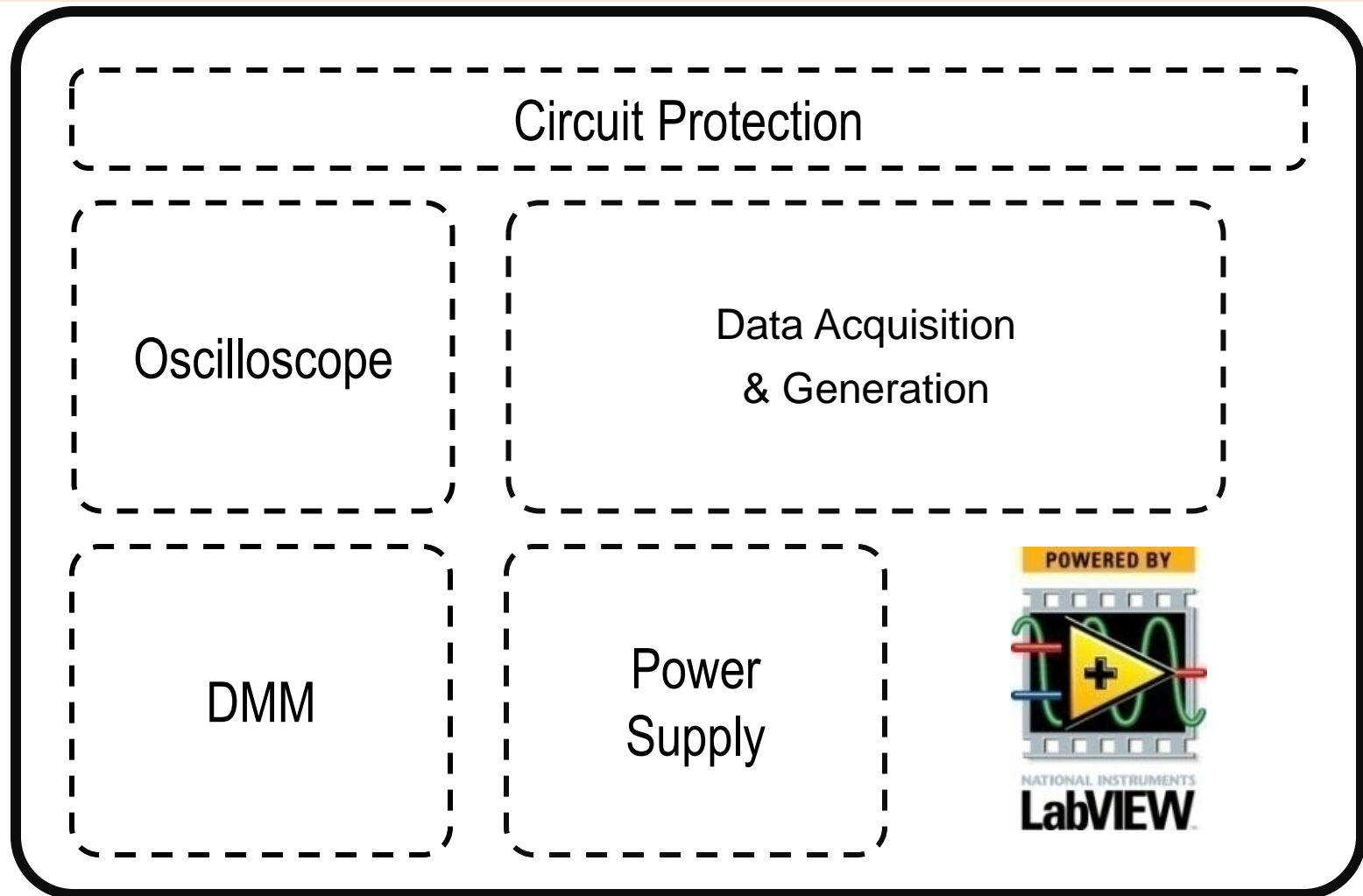
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What is NI ELVIS? | At the core...12

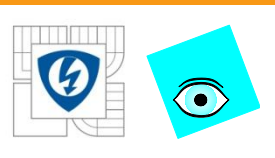
Instruments



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INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





NI ELVIS II | Hardware Specifications

Oscilloscope

- 16-bit resolution
- 1.25 MS/s single channel, 500kS/s two channel aggregate
- 1 to 1.5 MHz Bandwidth
- 1x and 10x probe
- ± 10 V input range
- AC/DC coupling

Internal Circuit Protection

- Resettable fuses

USB Connectivity

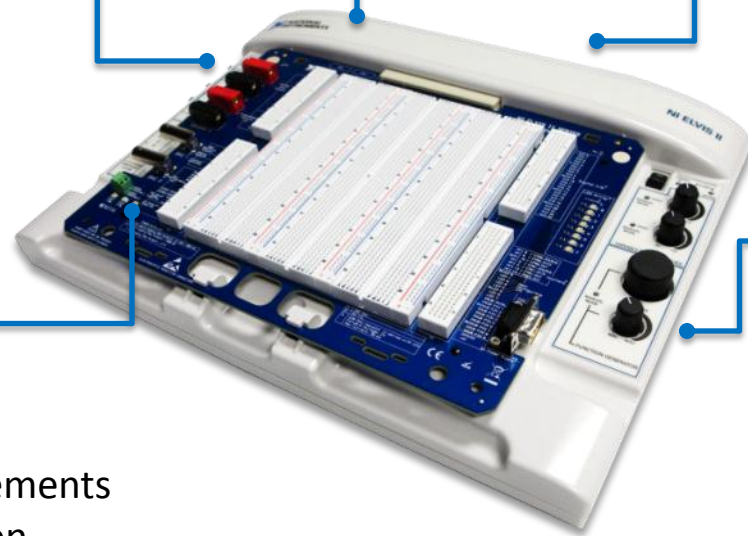
- Plug-and-play capability
- USB 2.0 Connection

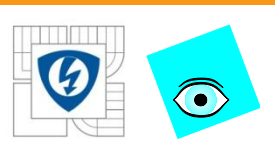
Function Generator

- 10 bit, ± 5 V range
- 0.2 Hz to 5 MHz Sine
- 0.2 Hz to 1 MHz Triangle/Square
- Software or manual control
- BNC or prototyping board connection

Digital Multimeter

- Isolated measurements
- $5\frac{1}{2}$ digit resolution
- 60 VDC, 20Vrms, 2 ADC, 2 Arms, 100M Ω





NI ELVIS II | Hardware Specifications

Impedance Analyzer

- 0.2 Hz to 35 kHz Range
- NPN, PNP, Diode

Other Analyzers:

- Bode Analyzer
- 2-wire Current Voltage Analyzer
- 3-Wire Current Voltage Analyzer

Prototyping Board

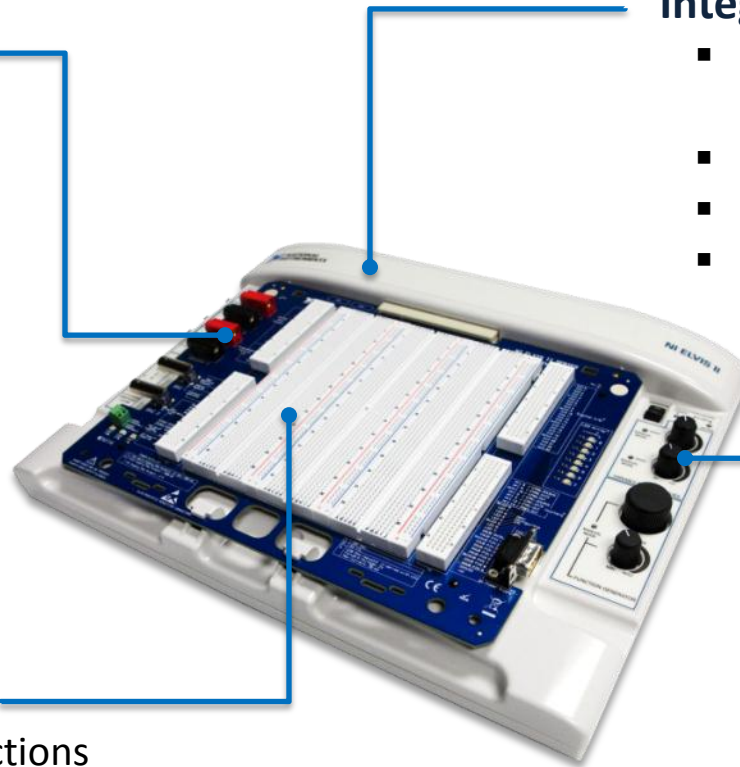
- Updated connections
- Detachable
- User-defined Banana Plugs, BNC, D-Sub connectors

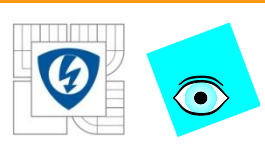
Integrated DAQ

- AI sampling rate 1.25 MS/s single channel, 500kS/s two channel
- 16-bit resolution
- AO 2.8 MS/s update rate
- 24 DIO lines, 15 PFI, 2 CTR

Variable Power Supply

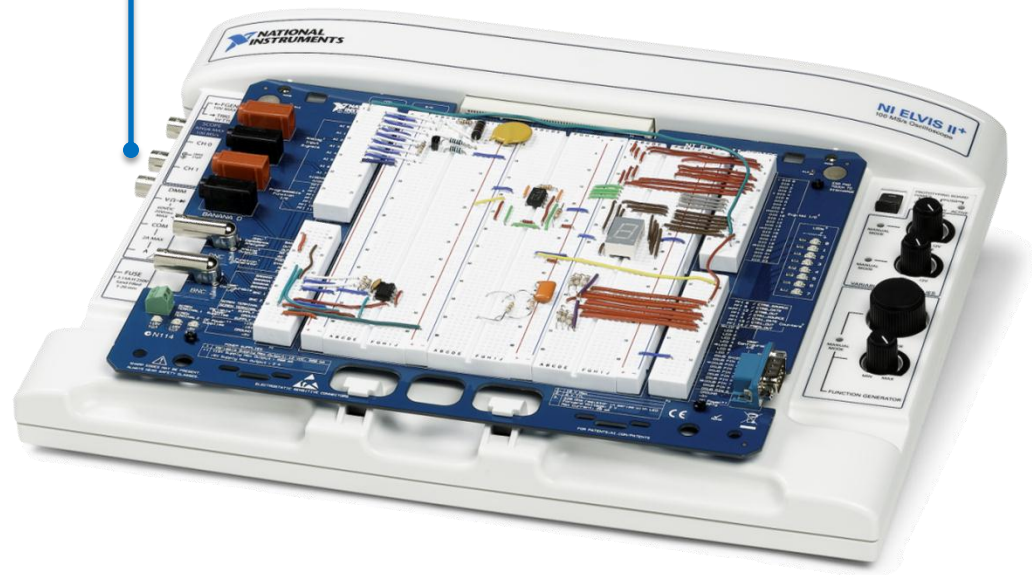
- 10-bit resolution
- 0 to +12V, 0 to -12V
- 500 mA current range

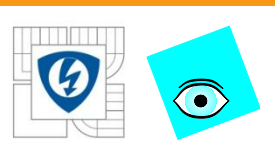




Oscilloscope

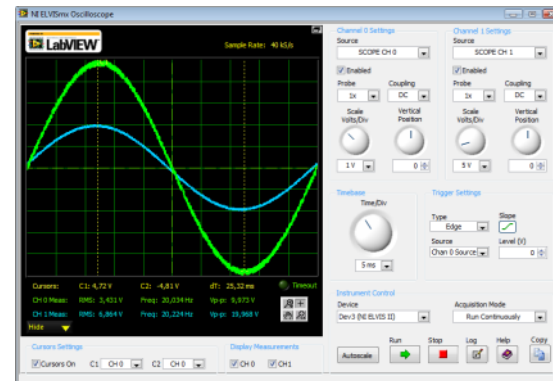
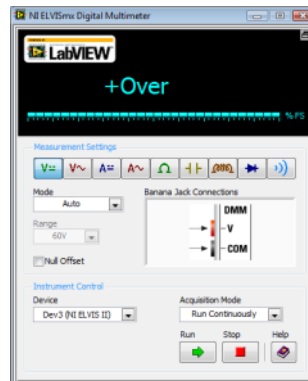
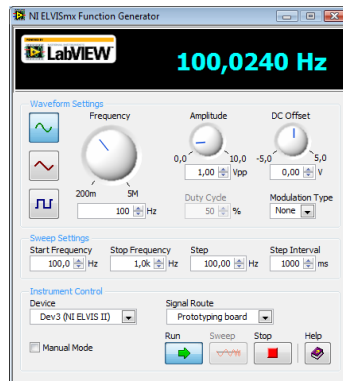
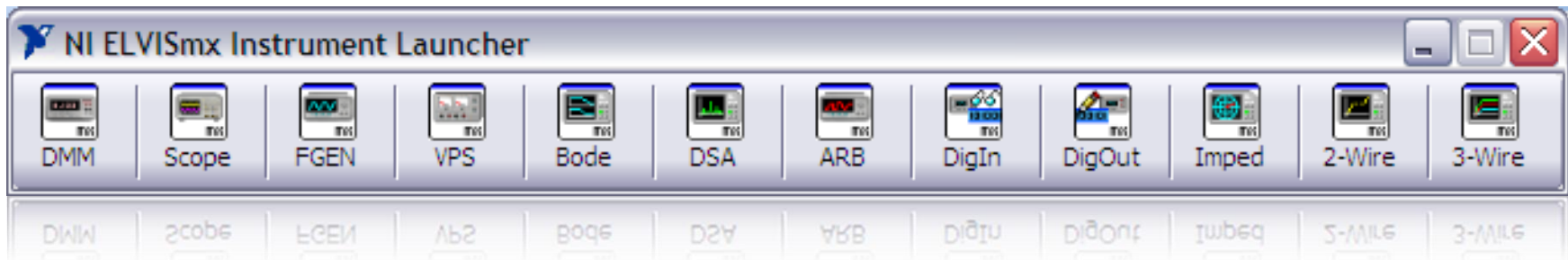
- 100MS/s Sampling Rate
- 50MHz Bandwidth(-3dB)
- 8-bit resolution
- ± 20 V max. input range
- AC/DC/GND coupling
- 20MHz Optional Noise Filter
- BNC connection





NI ELVISmx Driver | Software Specifications

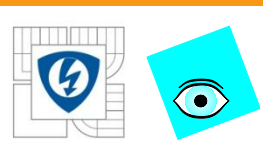
- Ready-to-use instruments – Soft Front Panels
- Customizable instruments



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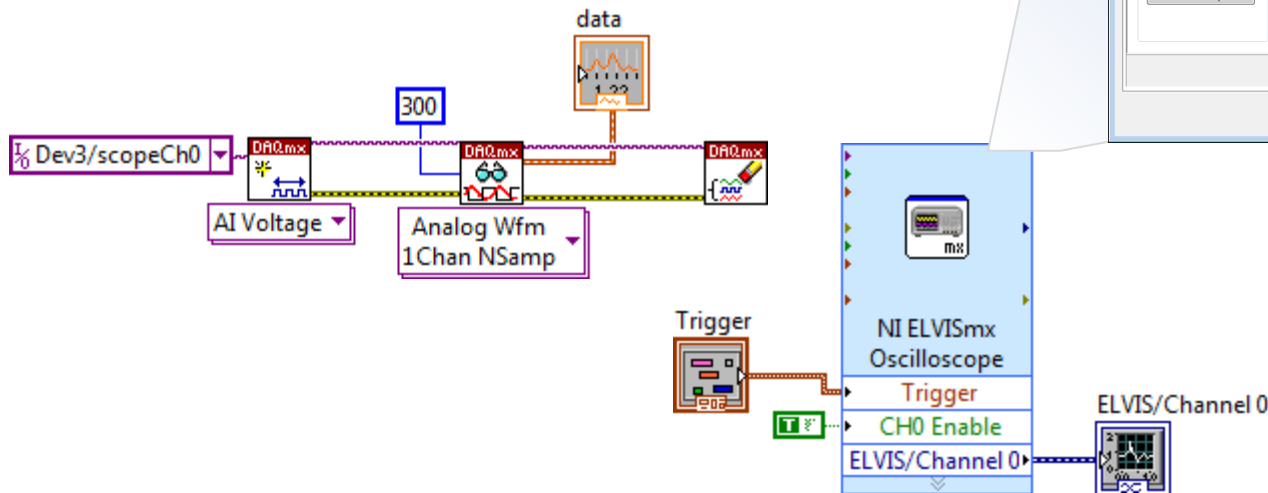
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

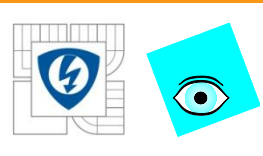




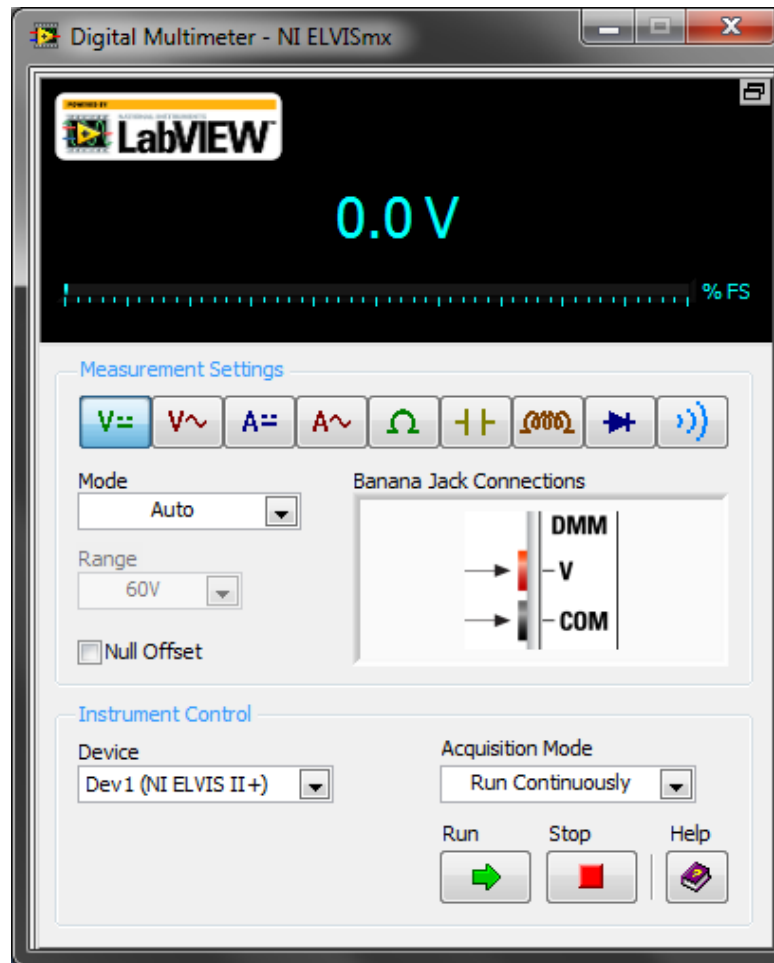
NI ELVISmx Driver | Software Specifications

- NI LabVIEW Express VIs
- NI DAQmx API
- NI LabVIEW SignalExpress





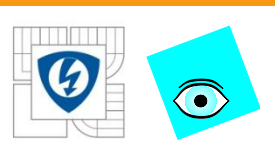
DMM



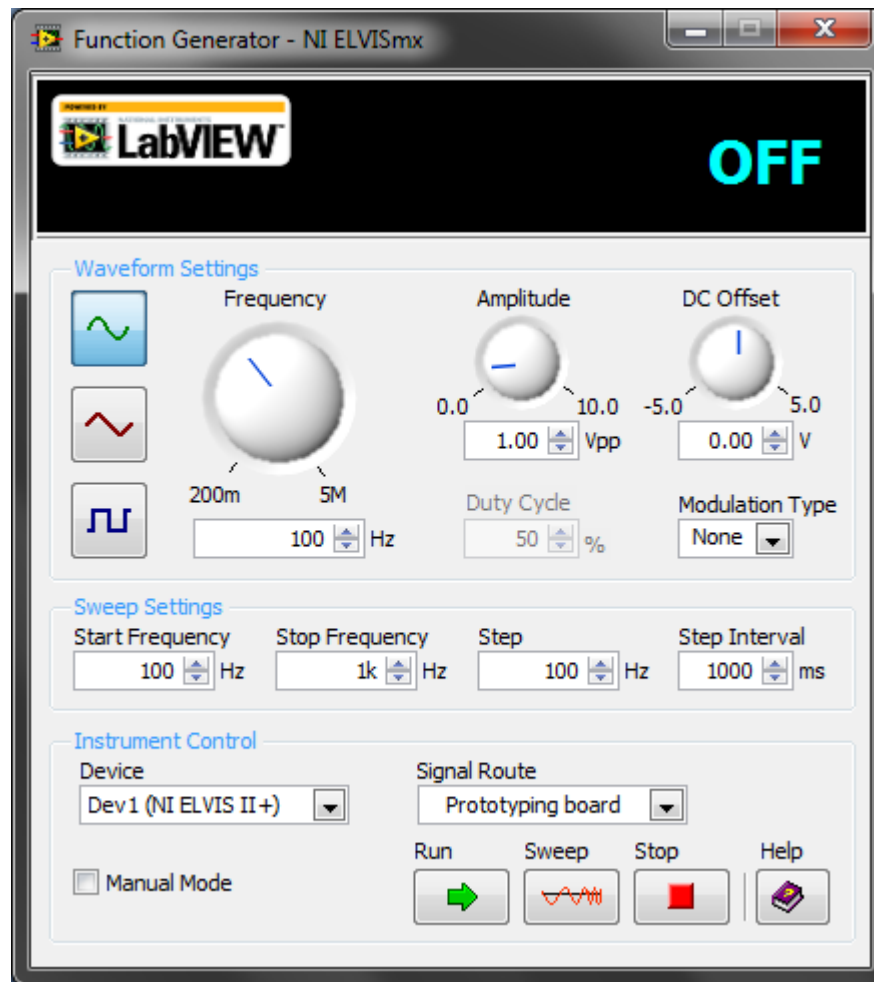
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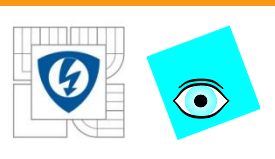
Function Generator



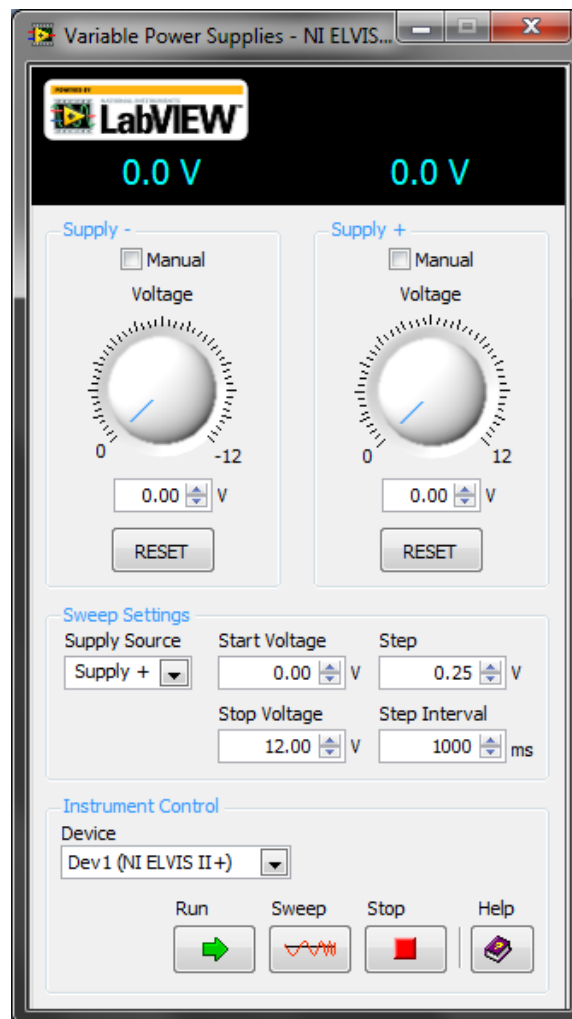
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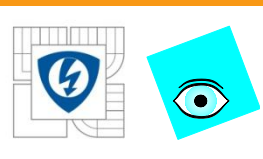
Programmable Power Supply



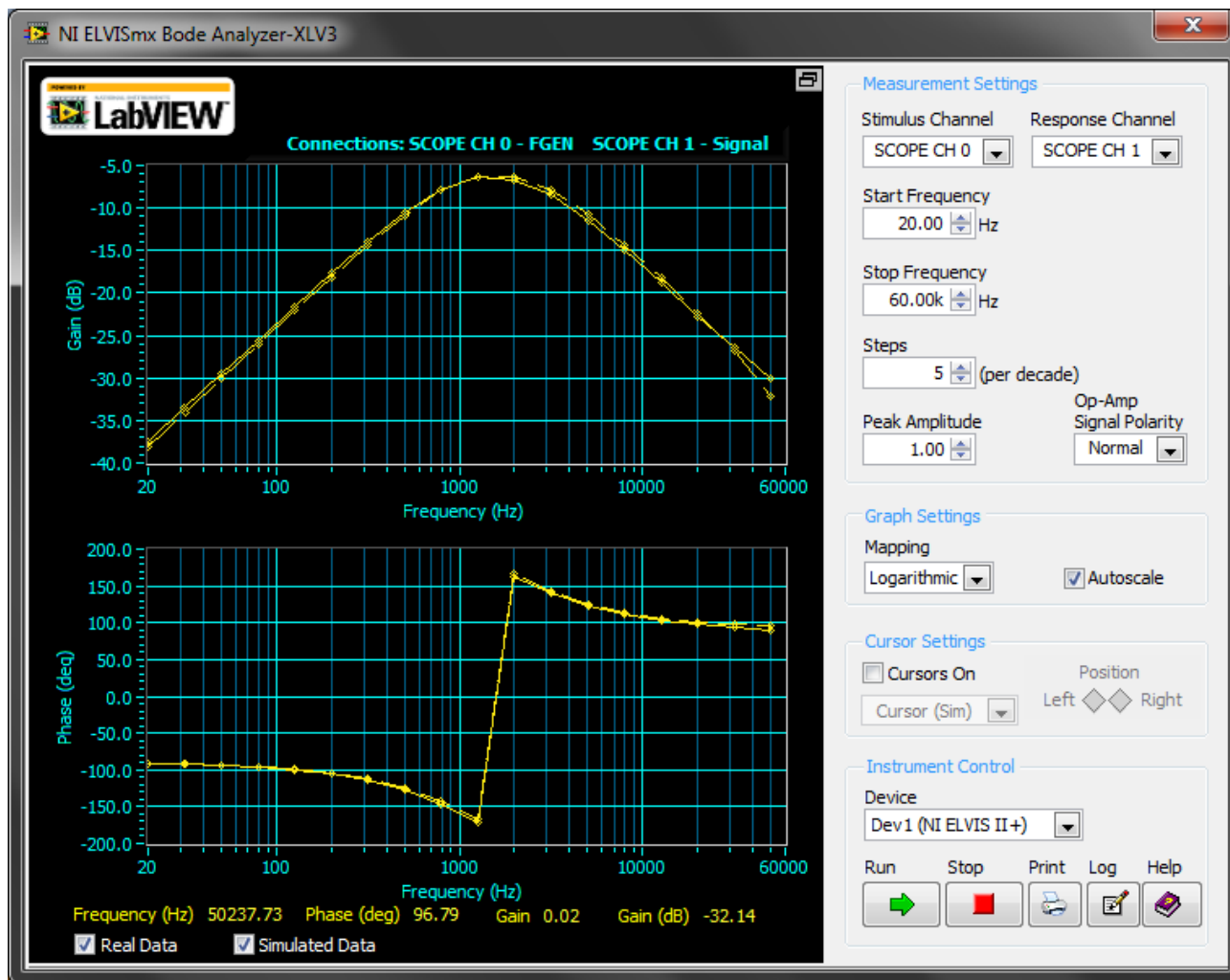
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INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



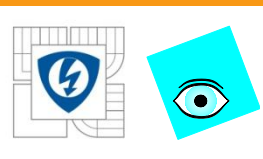


Bode Analyzer

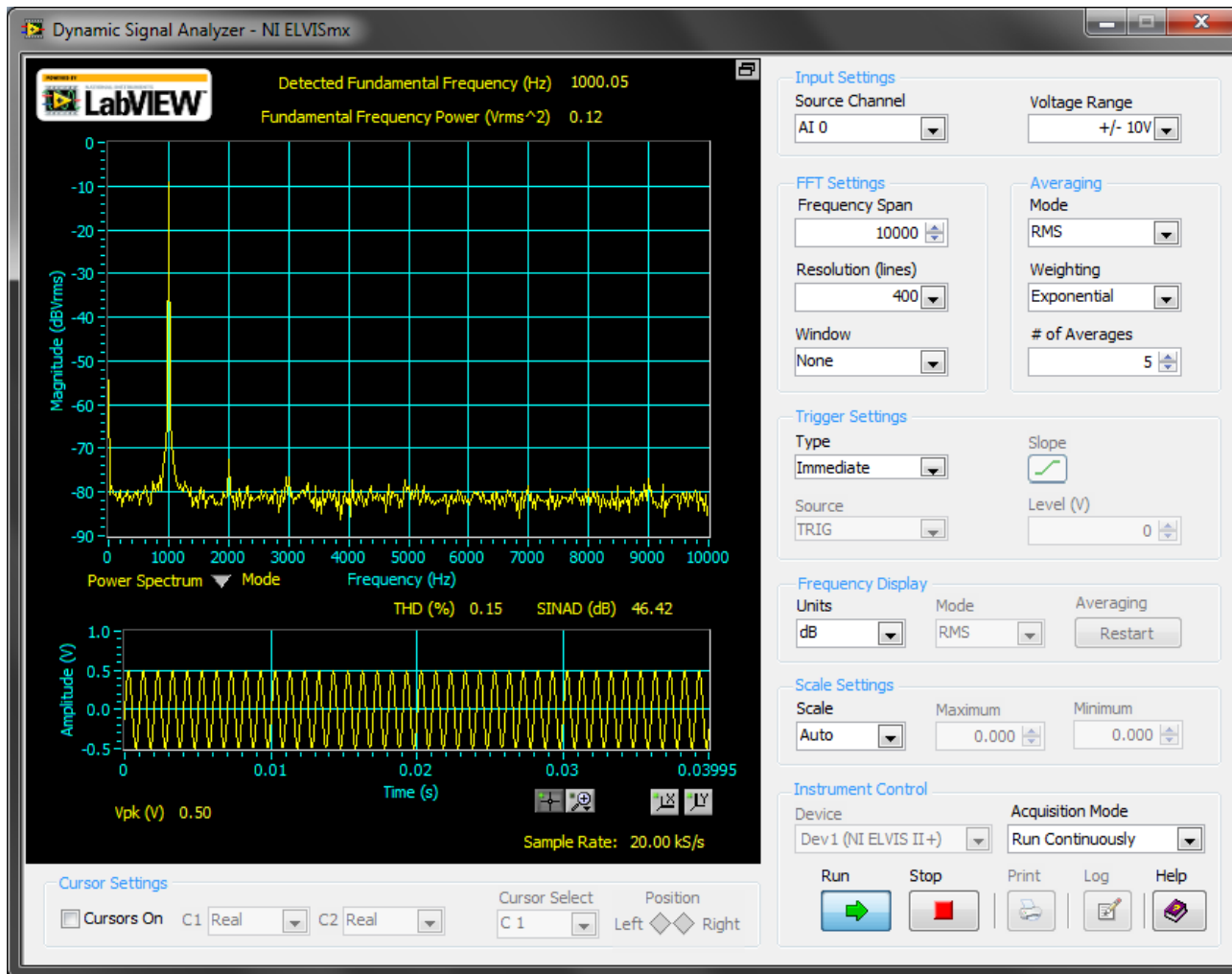


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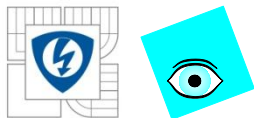


Dynamic Signal Analyzer

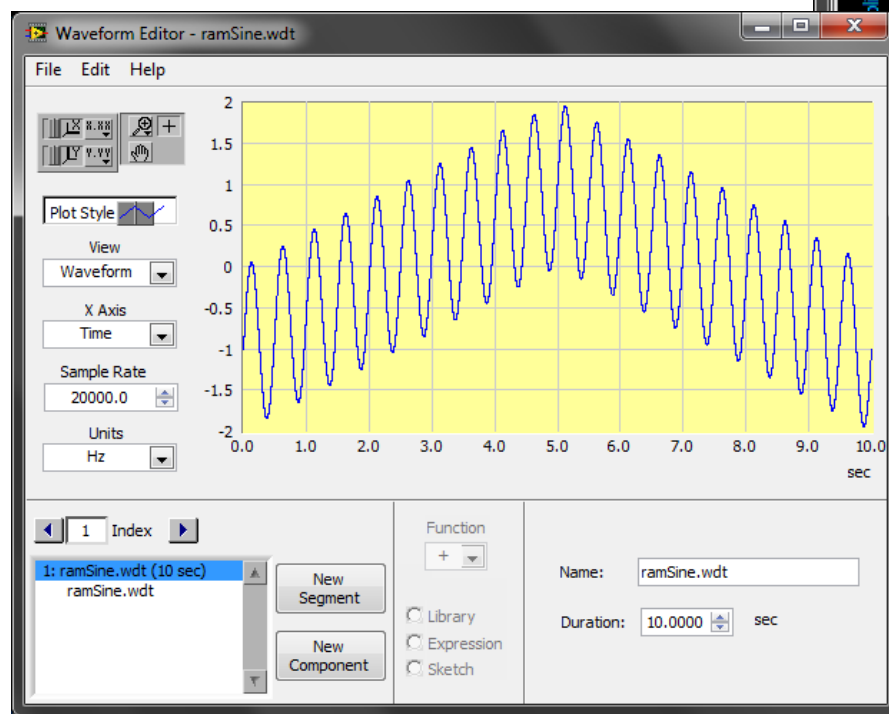


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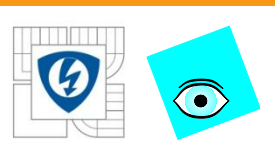


Arbitrary Waveform Generator

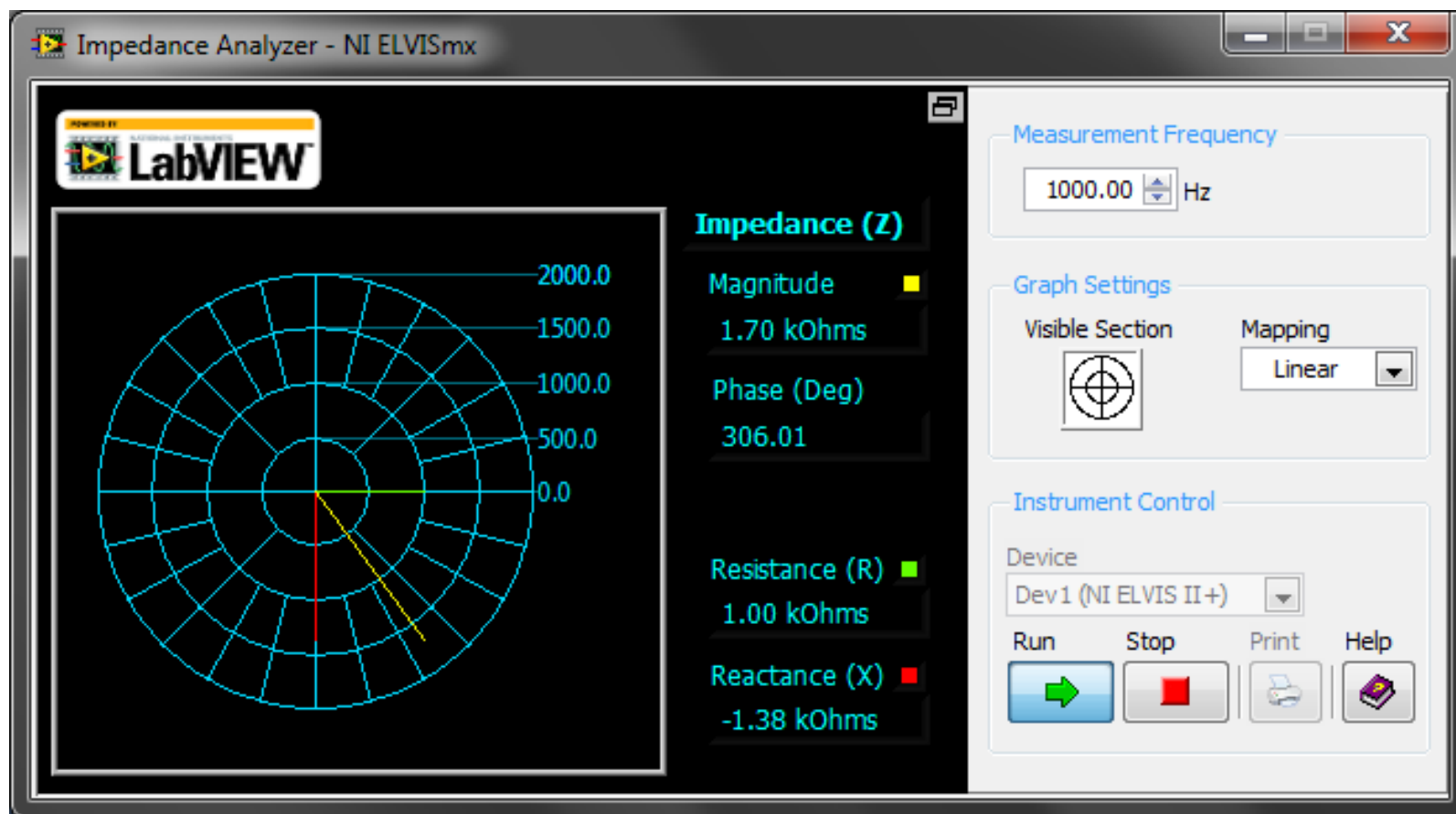


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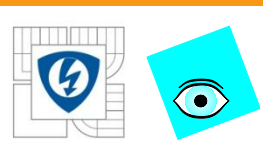
Impedance Analyzer



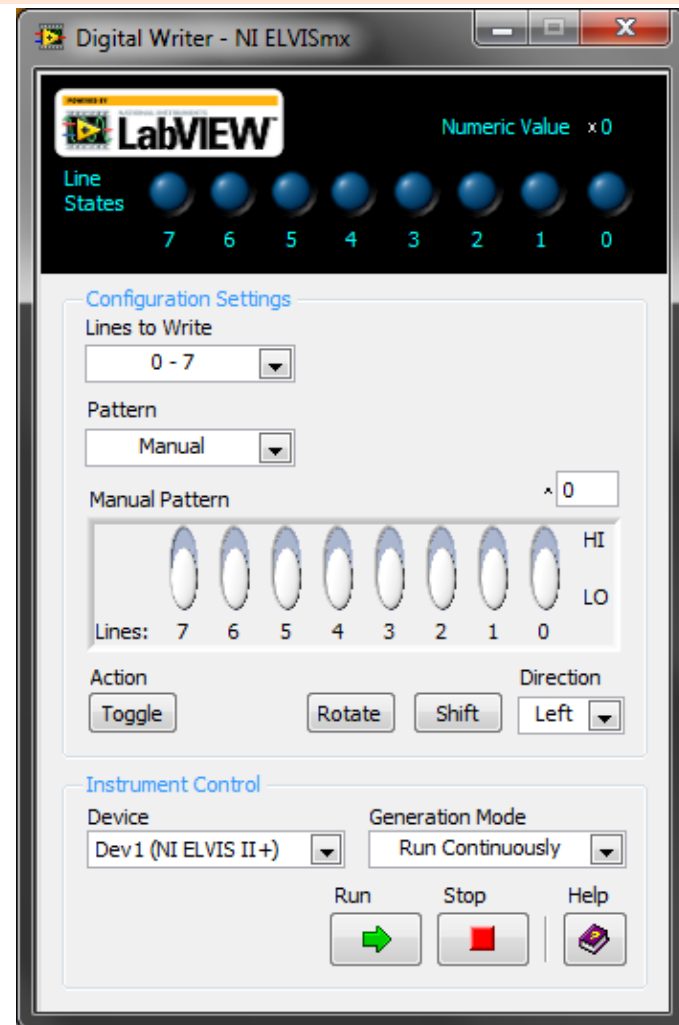
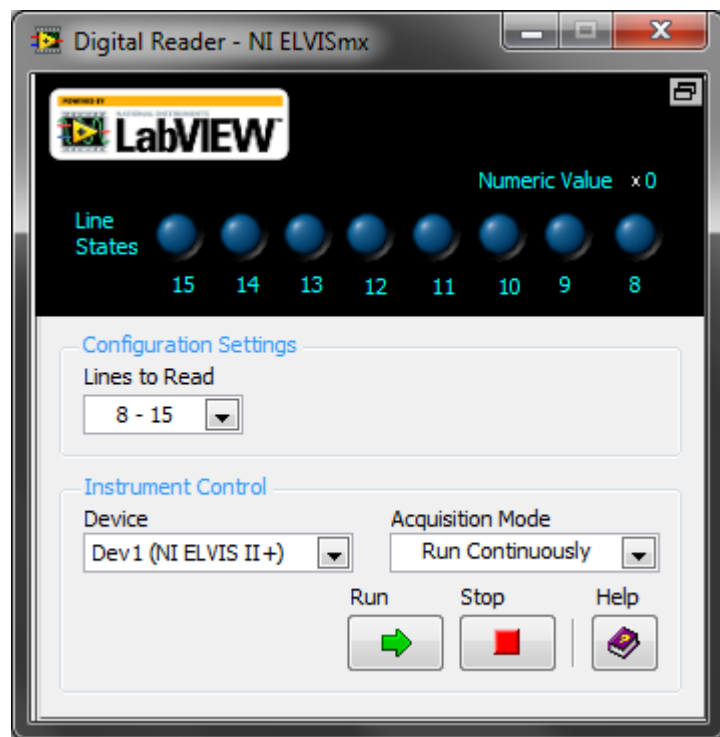
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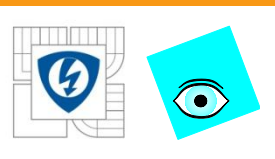


Digital In/Out

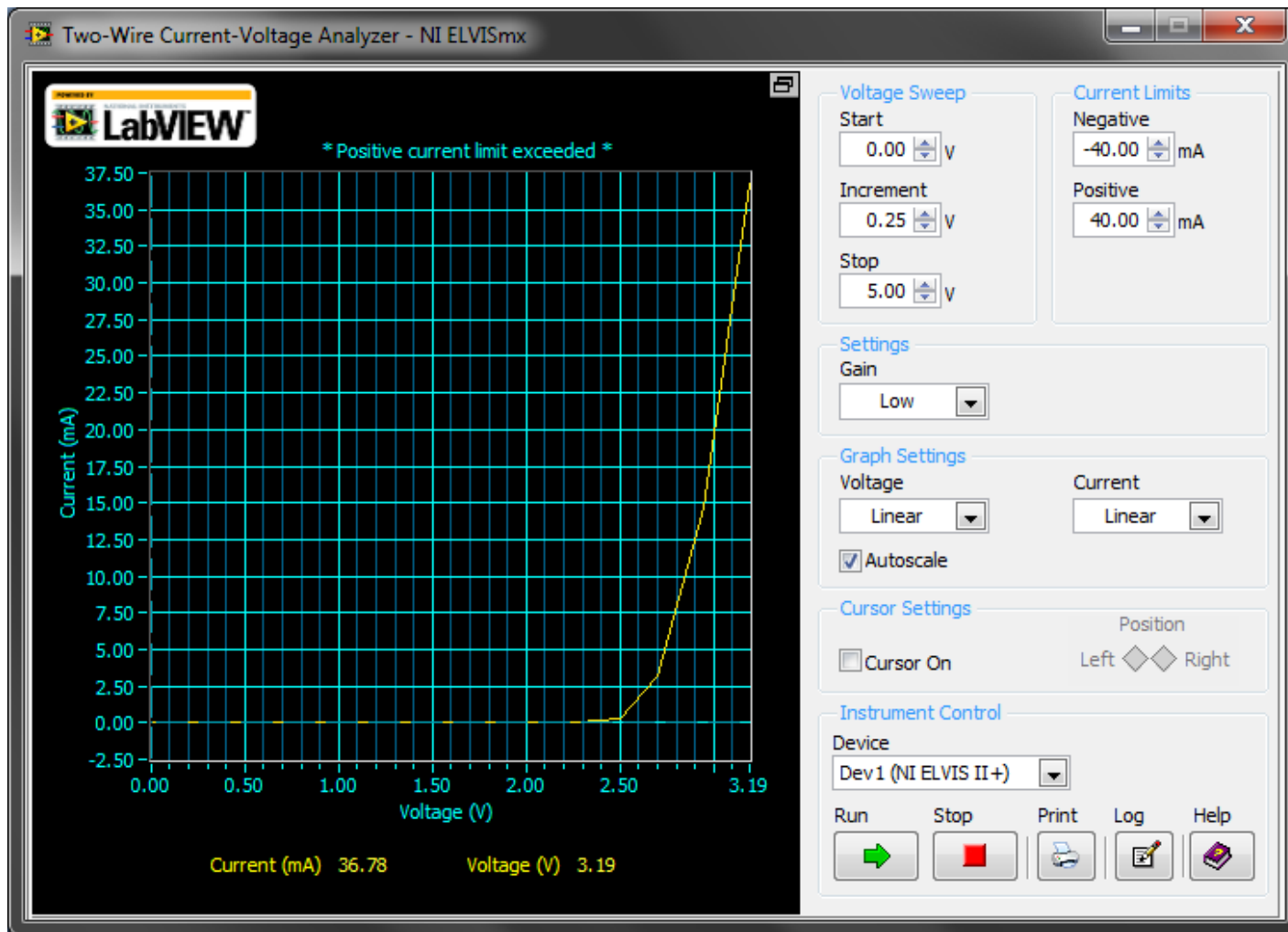


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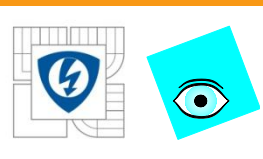


2-Wire Current Voltage analyzer

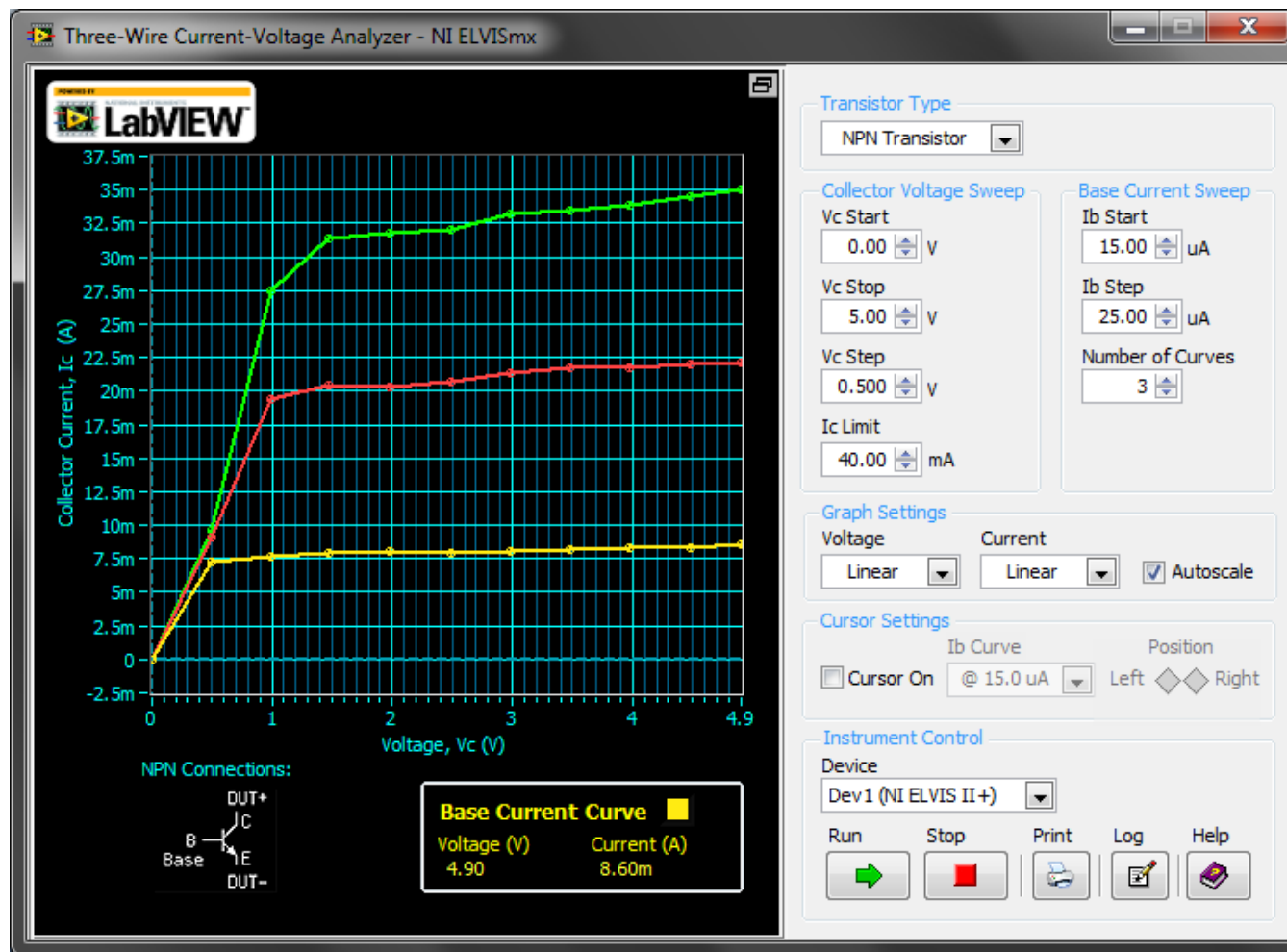


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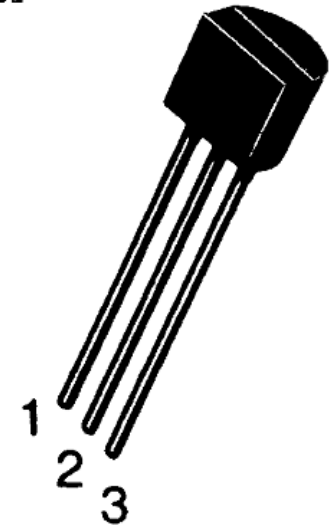
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3-Wire Current Voltage Analyzer



TO-92



1. Collector 2. Base 3. Emitter

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Controls and Mechatronics



Telecommunications



NATIONAL INSTRUMENTS™ NI ELVIS Platform



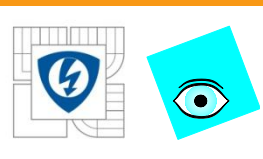
Circuits and Measurements



Digital Electronics



Embedded Design



Digital Electronics FPGA

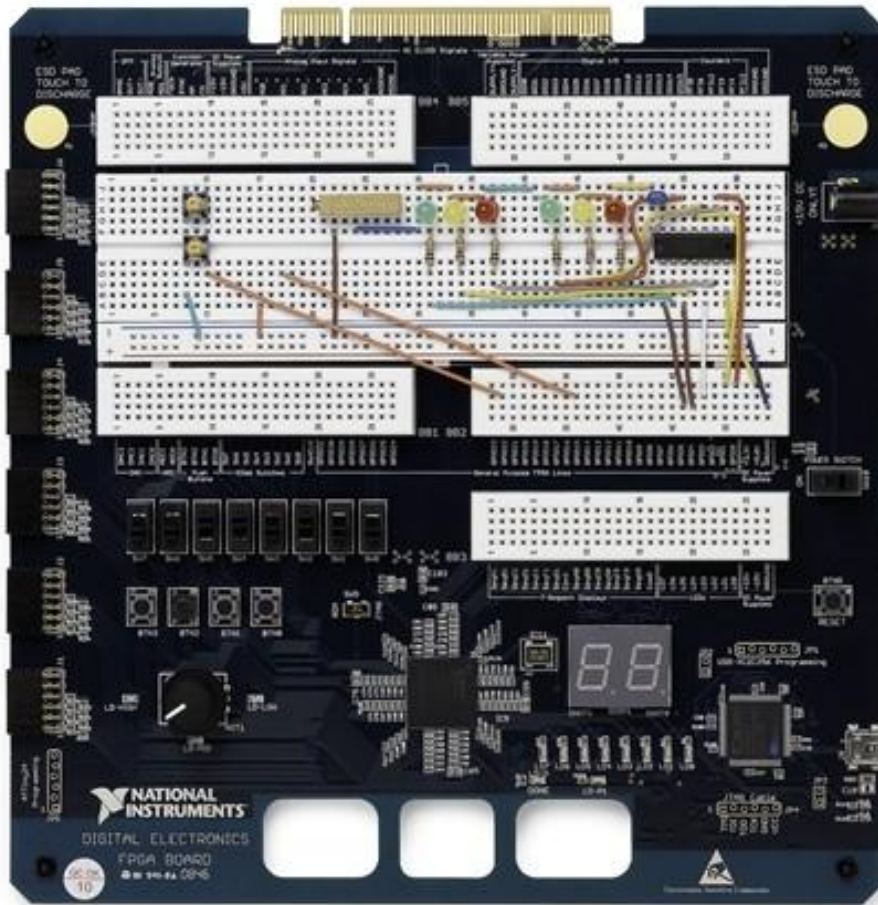


NATIONAL INSTRUMENTS

LabVIEW



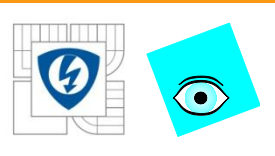
XILINX®



- Xilinx Spartan 3E FPGA
- Integrated Breadboard
- Power Supply
- ADC and DAC
- LEDs
- Push Button Encoder
- 7 Segment Display
- Switches & Buttons
- USB Connection

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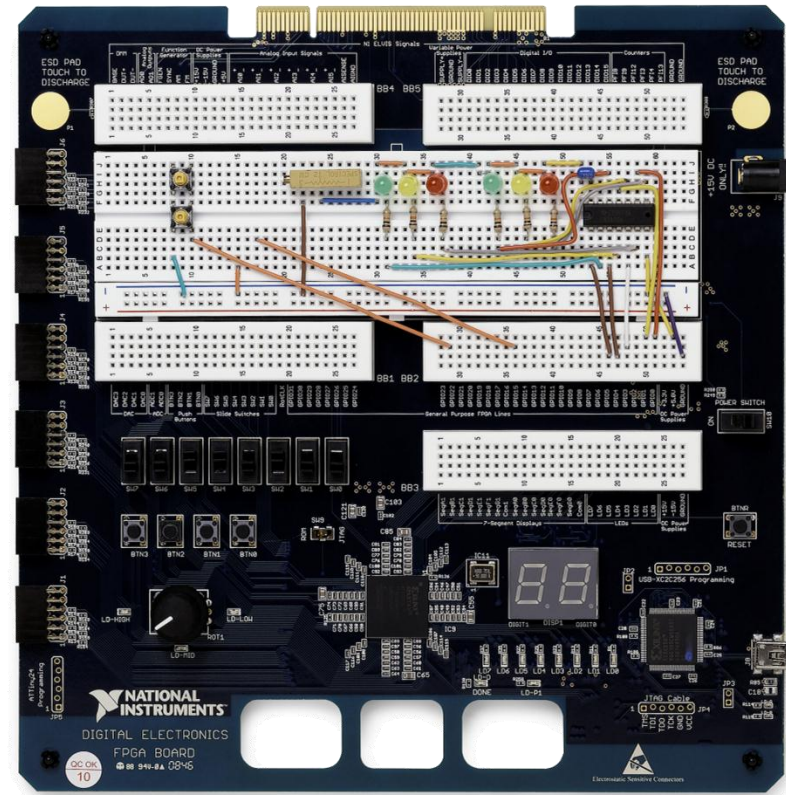
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

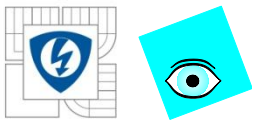


Digital Electronics FPGA

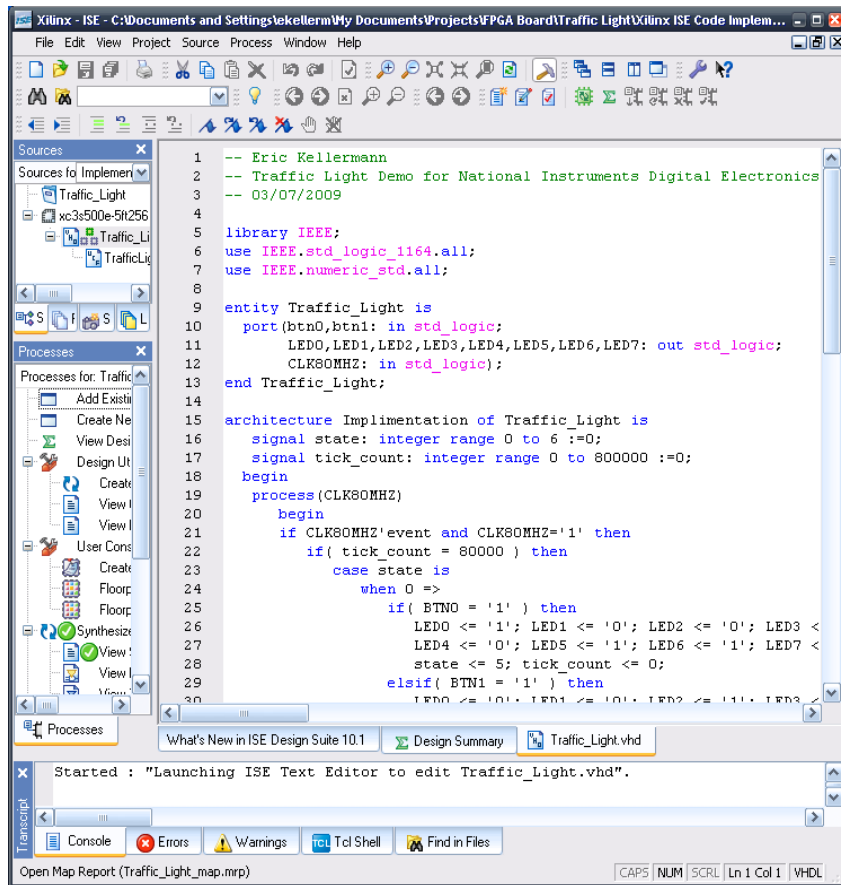
Digital Circuit development platform based on the Xilinx Spartan 3E FPGA

- I/O to teach basic to advance digital electronics concepts
- JTAG-over-USB connectivity
- 6 Pmod connectors

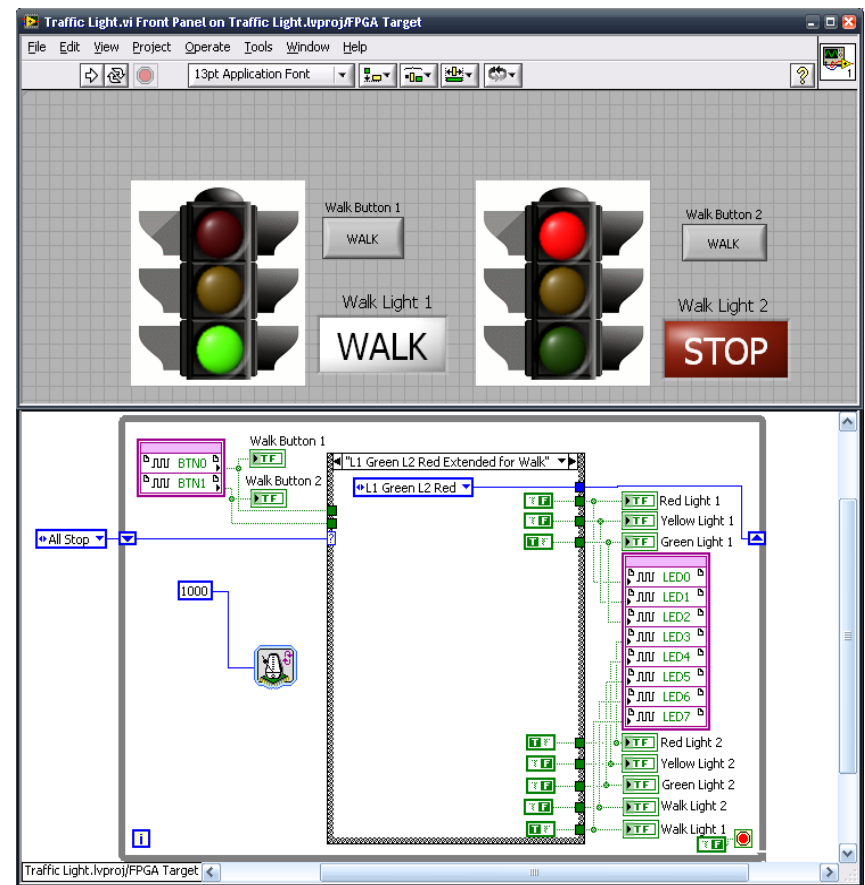




NI DE FPGA Board | Programming



VHDL/Verilog

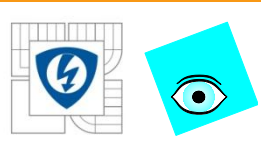


NI LabVIEW

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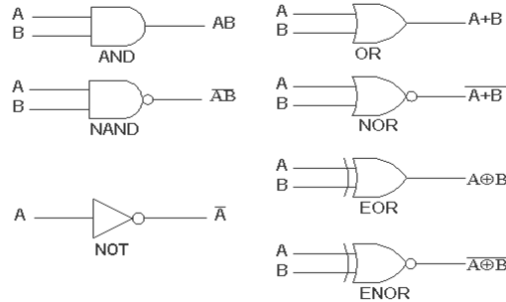


Challenge: Digital Electronics → VHDL

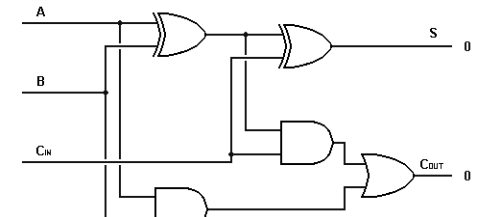
	BC				
A \	00	01	11	10	
0			1		
1		1	1	1	

$$\text{Output} = AB + BC + AC$$

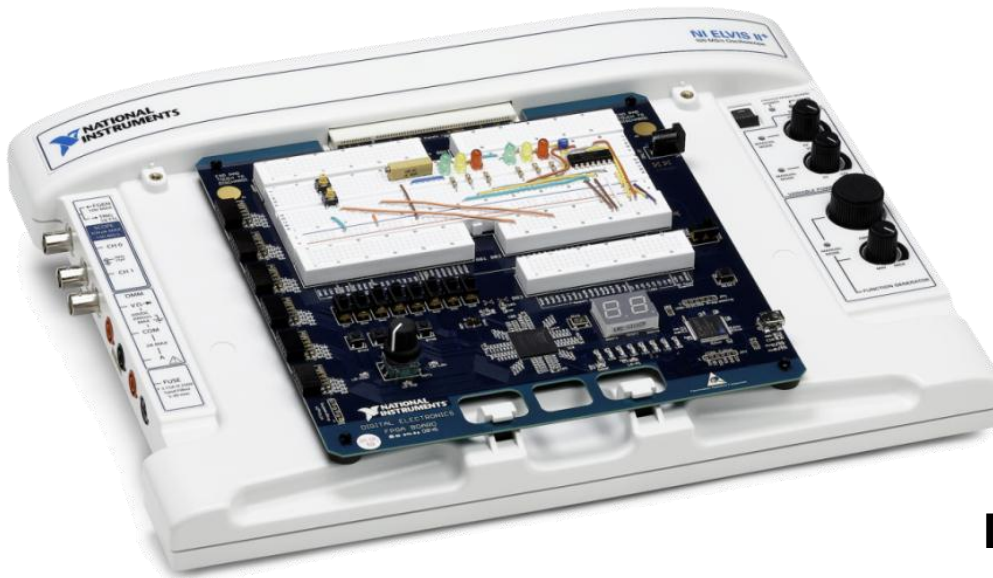
Boolean Algebra



Logic Gates



Digital Logic Design

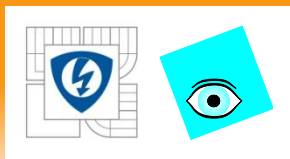


DE FPGA

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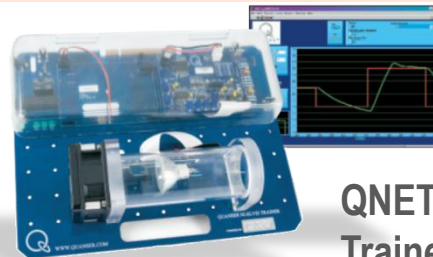




NI ELVIS | Controls & Mechatronics Plants



QNET-011 Rotary Inverted Pendulum



QNET-012 HVAC Trainer



QNET-010 DC Motor Control Trainer



QUANSER
INNOVATE. EDUCATE.



NATIONAL INSTRUMENTS

LabVIEW

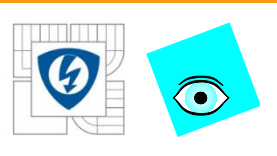
NEW! QNET-014 Mechatronics Sensors 1 Board

NEW! QNET-013 VTOL 1DOF Helicopter Plant



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INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



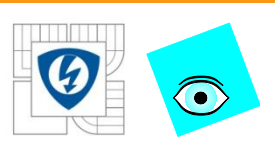
Exammple approach QPSK

Quadrature Phase Shift Keying

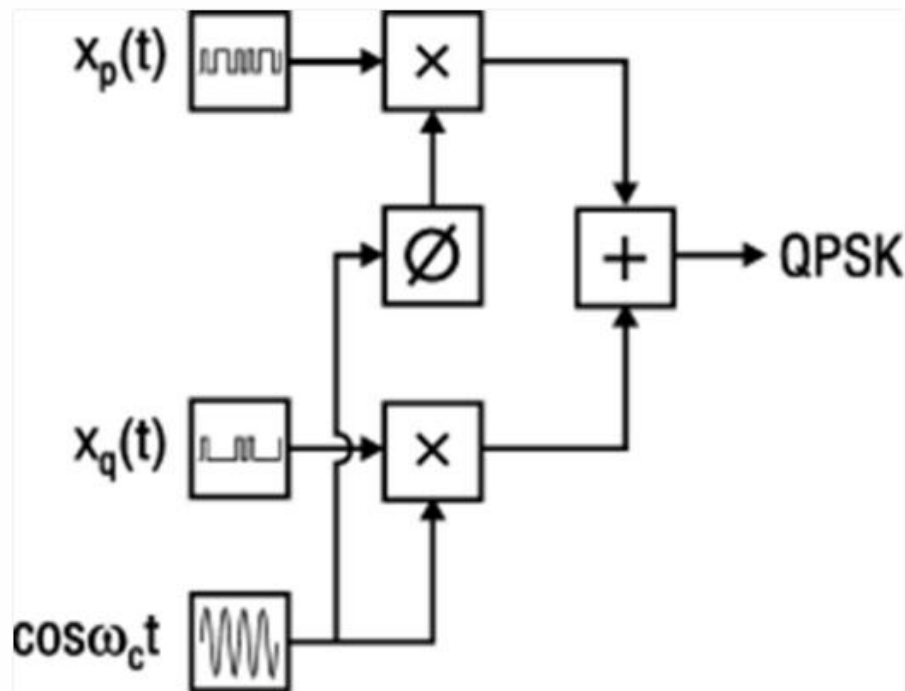
Start with Math and Theory

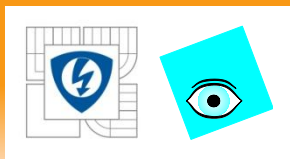
$$\text{QPSK} = x_p(t) * \cos(w*t) + x_q(t) * \sin(w*t)$$

where $x_p(t)$ and $x_q(t)$ are aternate elements of a digital sequence



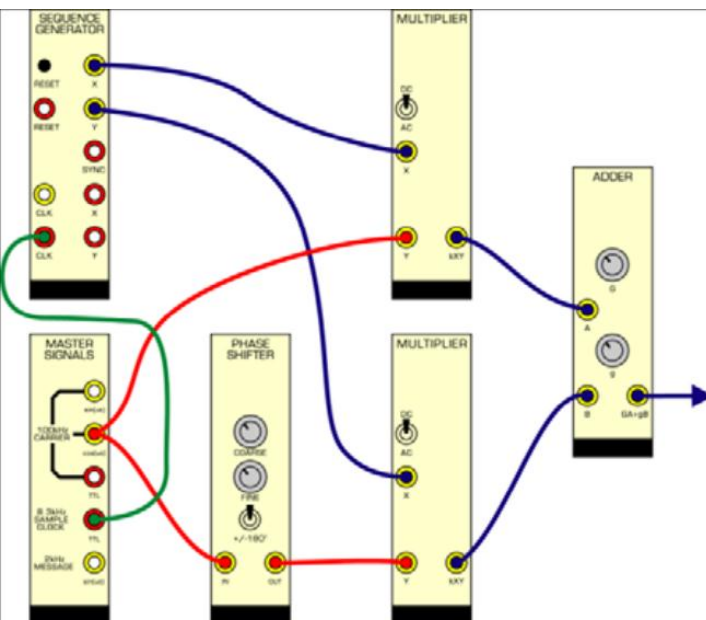
- Represent it as a Block Diagram





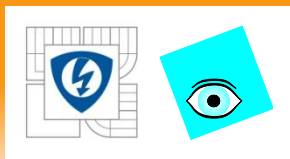
DATEx

- Build it using DATEx modules

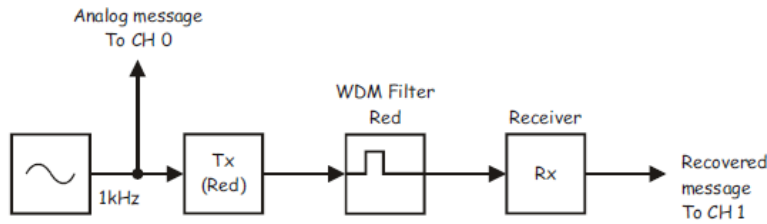


13. 4. 2012

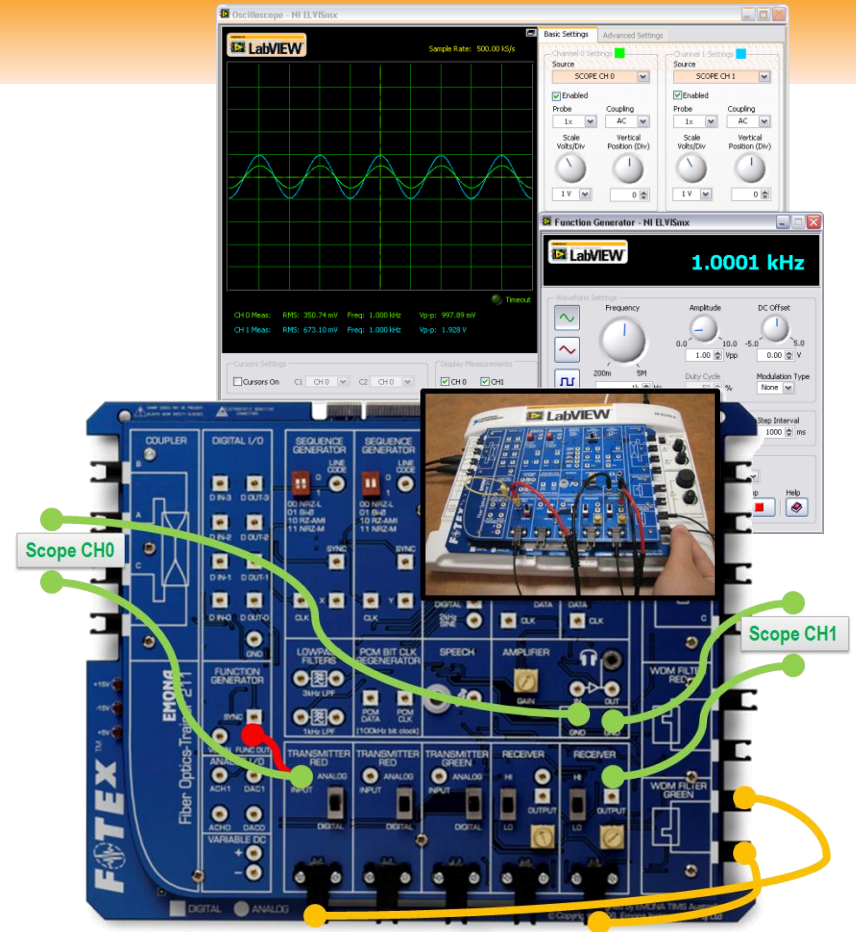
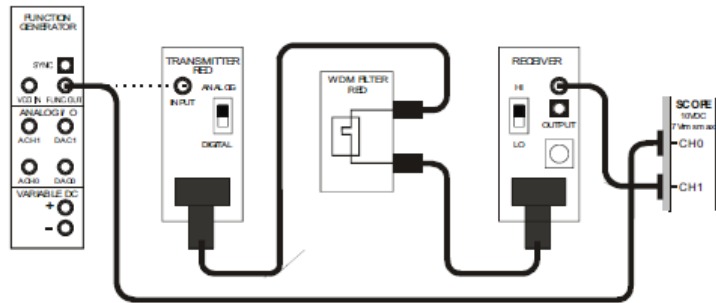
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



Teaching | Fiber Optics



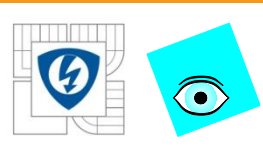
Step 1: Block diagram approach to optical signal filtering, splitting and combining



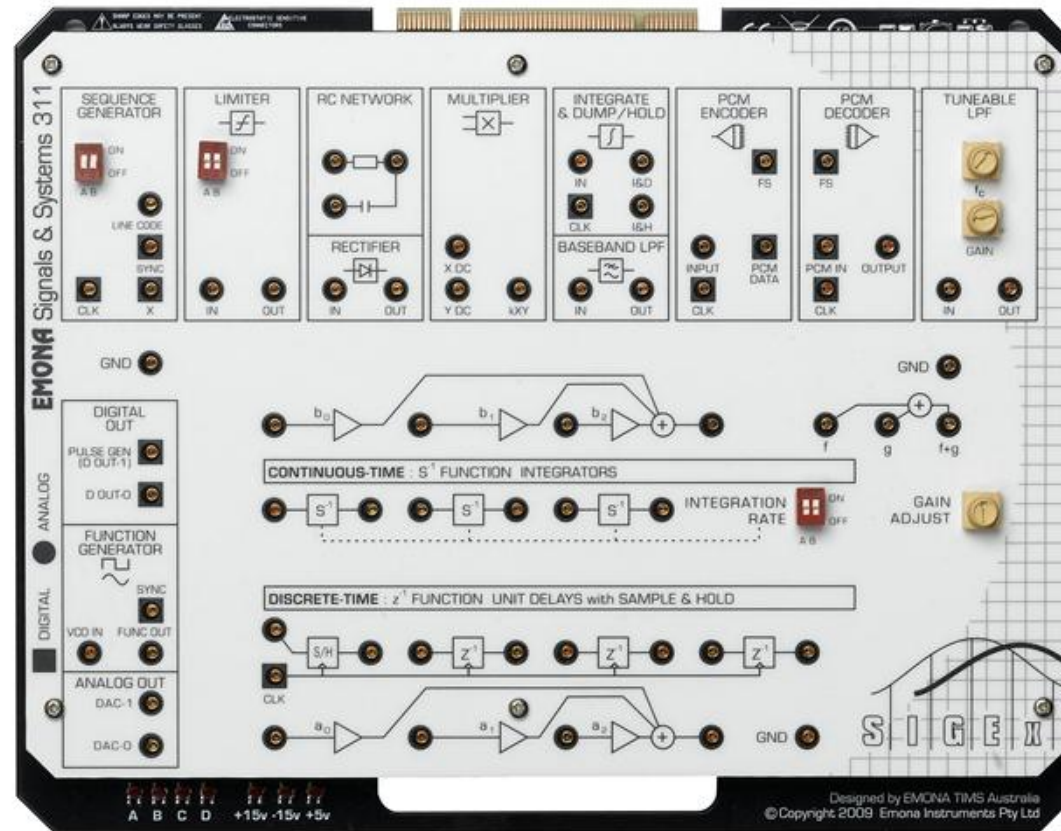
Step 2: Connecting FOTex Modules and NI ELVIS Instruments

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INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



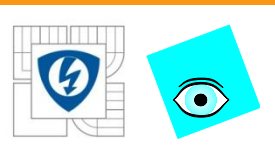
SIGEx



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INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





REAL HARDWARE FUNCTIONAL BLOCKS - FULLY INTEGRATED WITH NI ELVIS™

A Complete Suite of Signals & Systems Functional Blocks

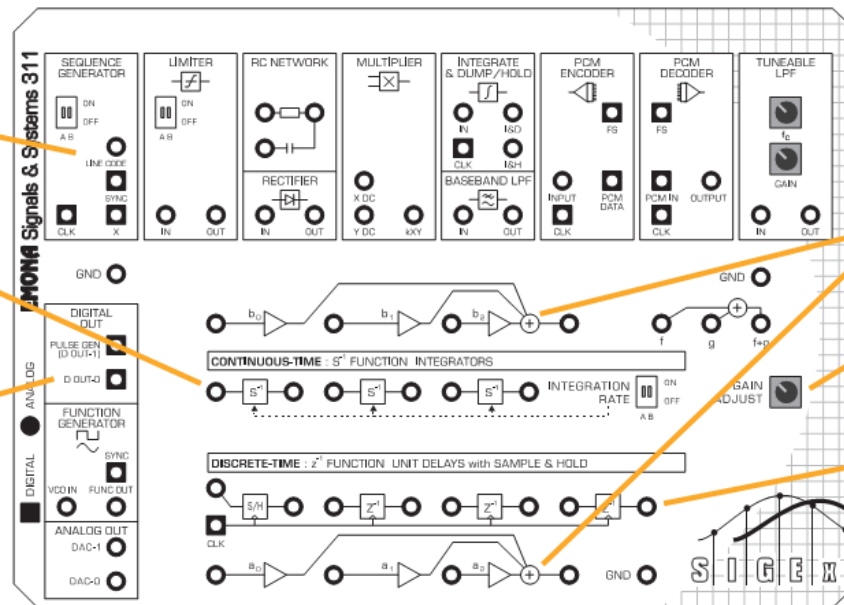
The SIGEx-311 board includes all of the functional blocks - integrators, sample-and-hold, unit delays and supporting blocks - required for all experiments, as well as access to powerful instruments from NI ELVIS™

A selection of independent functional SYSTEM blocks

Three 1/s functions

Access to NI ELVIS instruments, including

- Clock generator
- Function generator
- Dual ARB generator

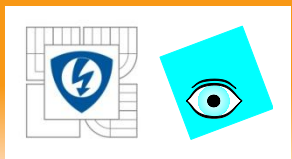


Three input ADDERS with user adjustable gains

Manual adjustment of on-screen ADDER gain values

Three UNIT DELAYS, preceded by a SAMPLE & HOLD

SIGEx add-on board for the NI ELVIS™ platform



NI ELVIS | Telecommunications & Fiber Optics

EMONA
times

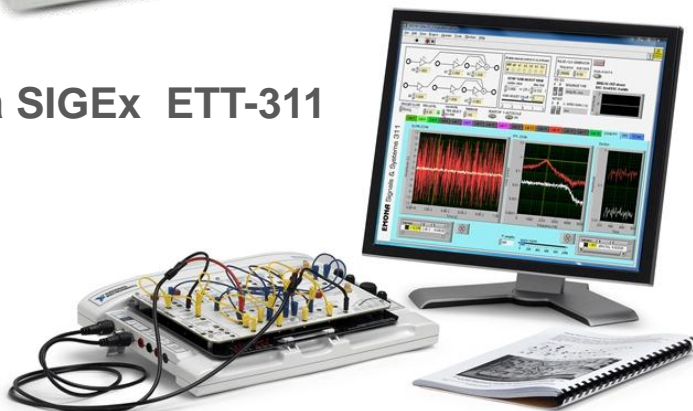
Emona FOTEx ETT-203



Emona DATEx ETT-202



Emona SIGEx ETT-311



Teaching materials
included

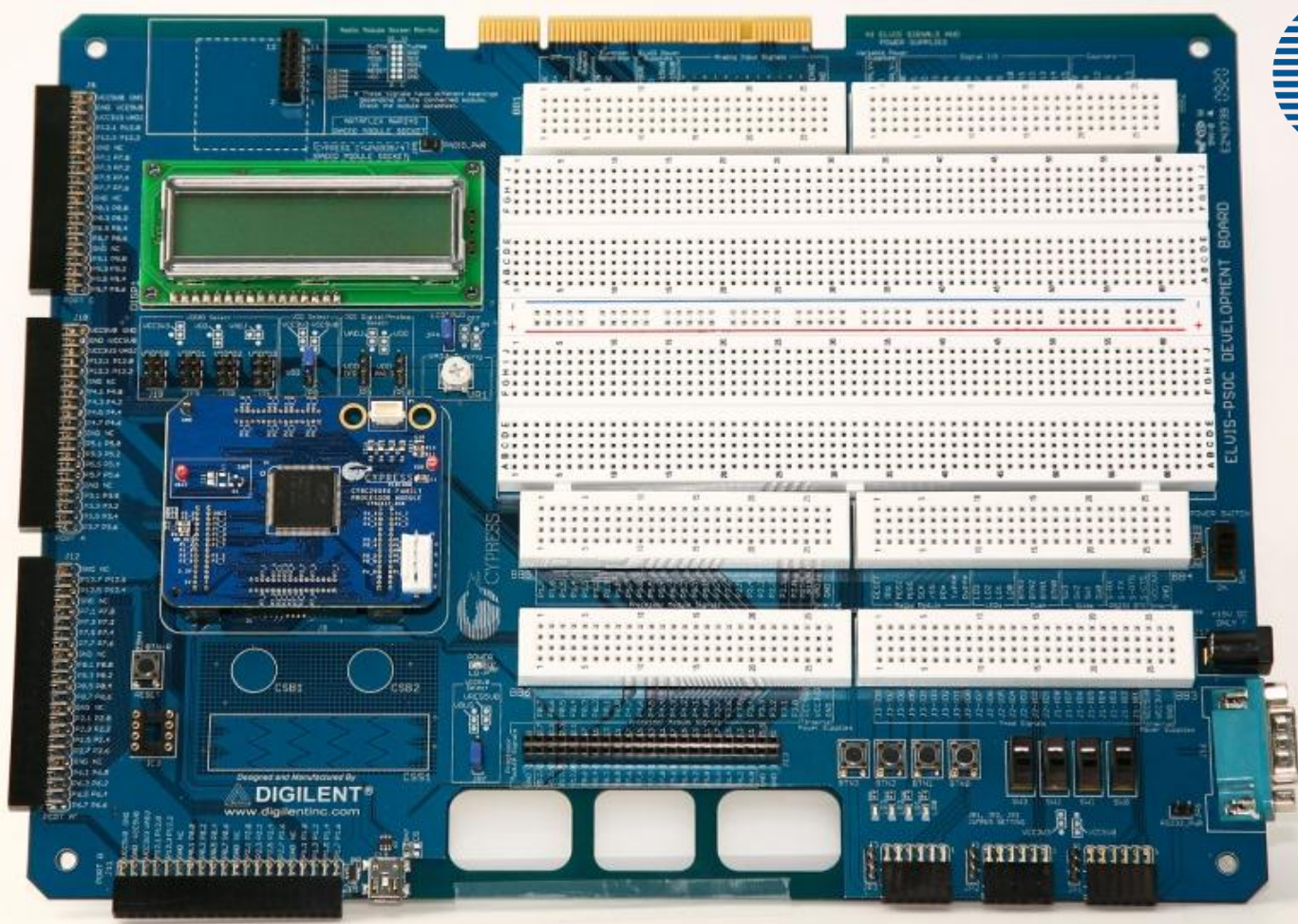
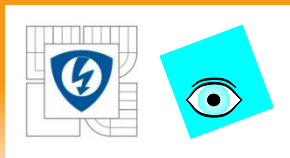


13. 4. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



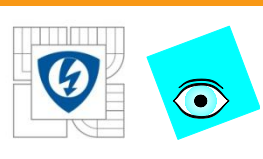
Cypress PSoc NI ELVIS board



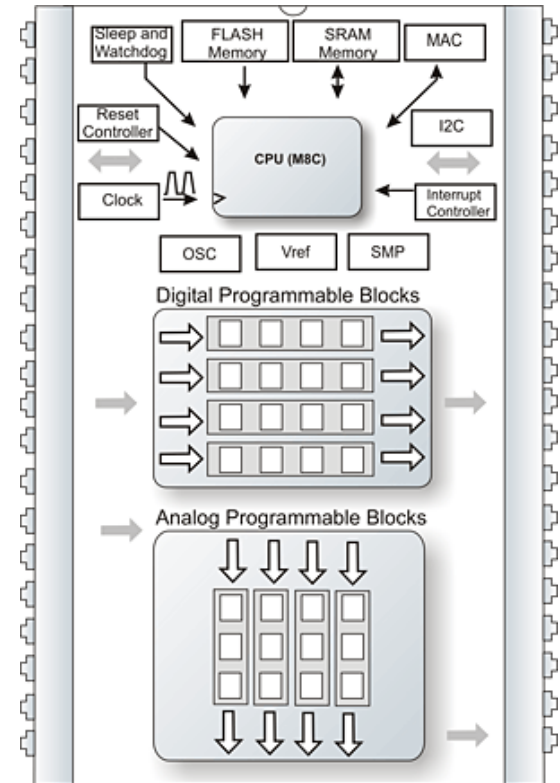
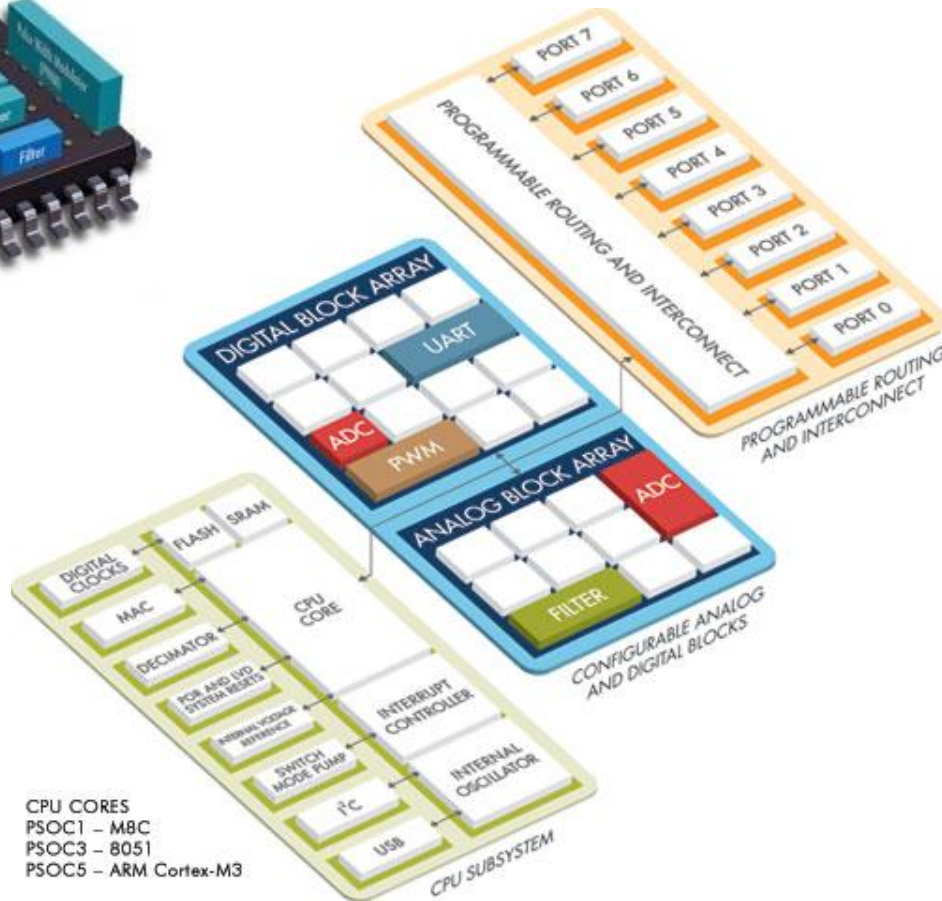
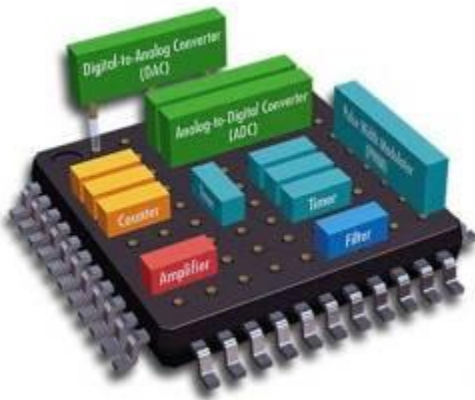
13. 4. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Cypress PSoc NI ELVIS board



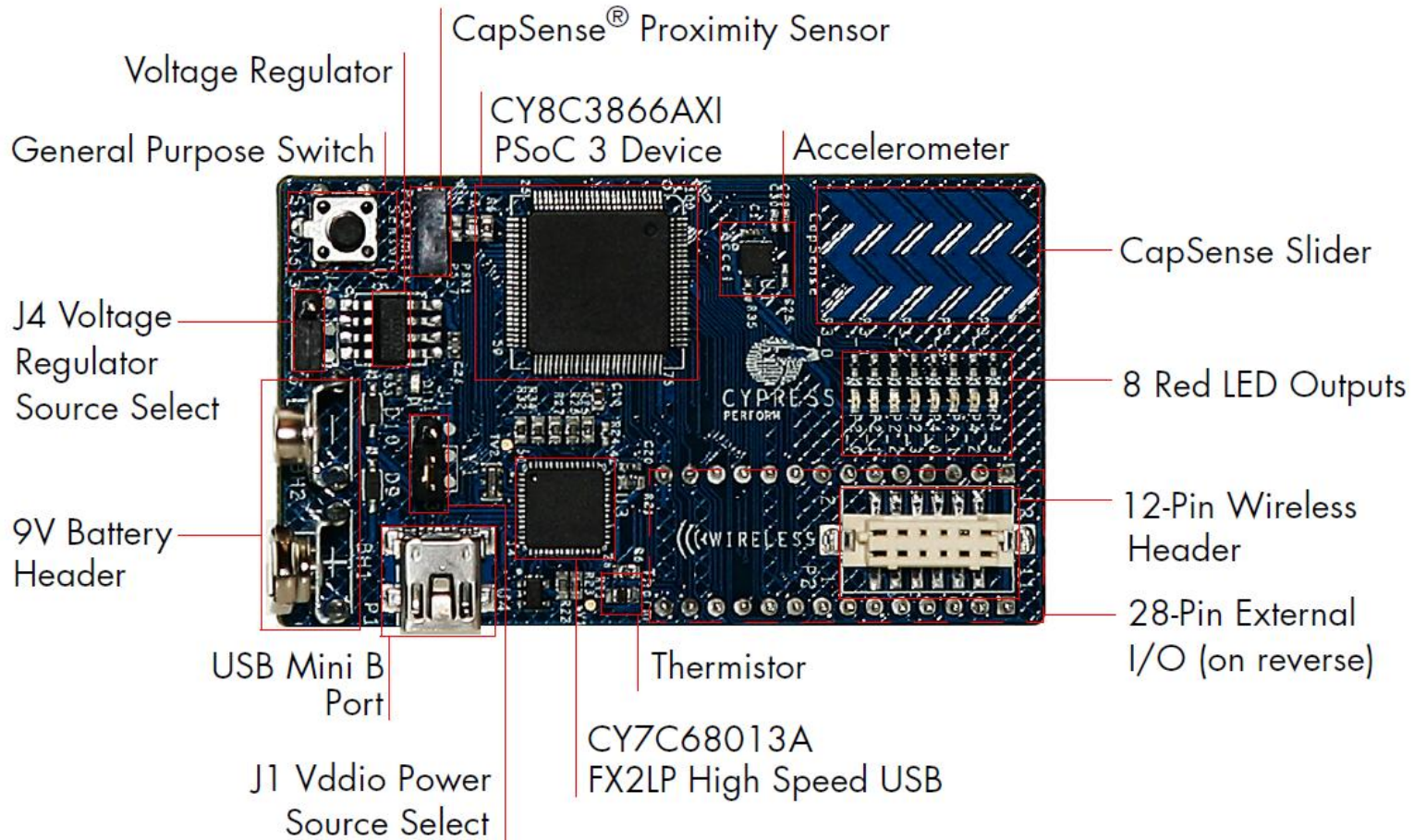
13. 4. 2012

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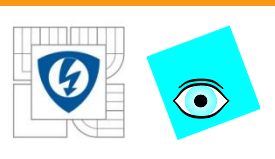


Example of daughterboard PSoC 3 kit



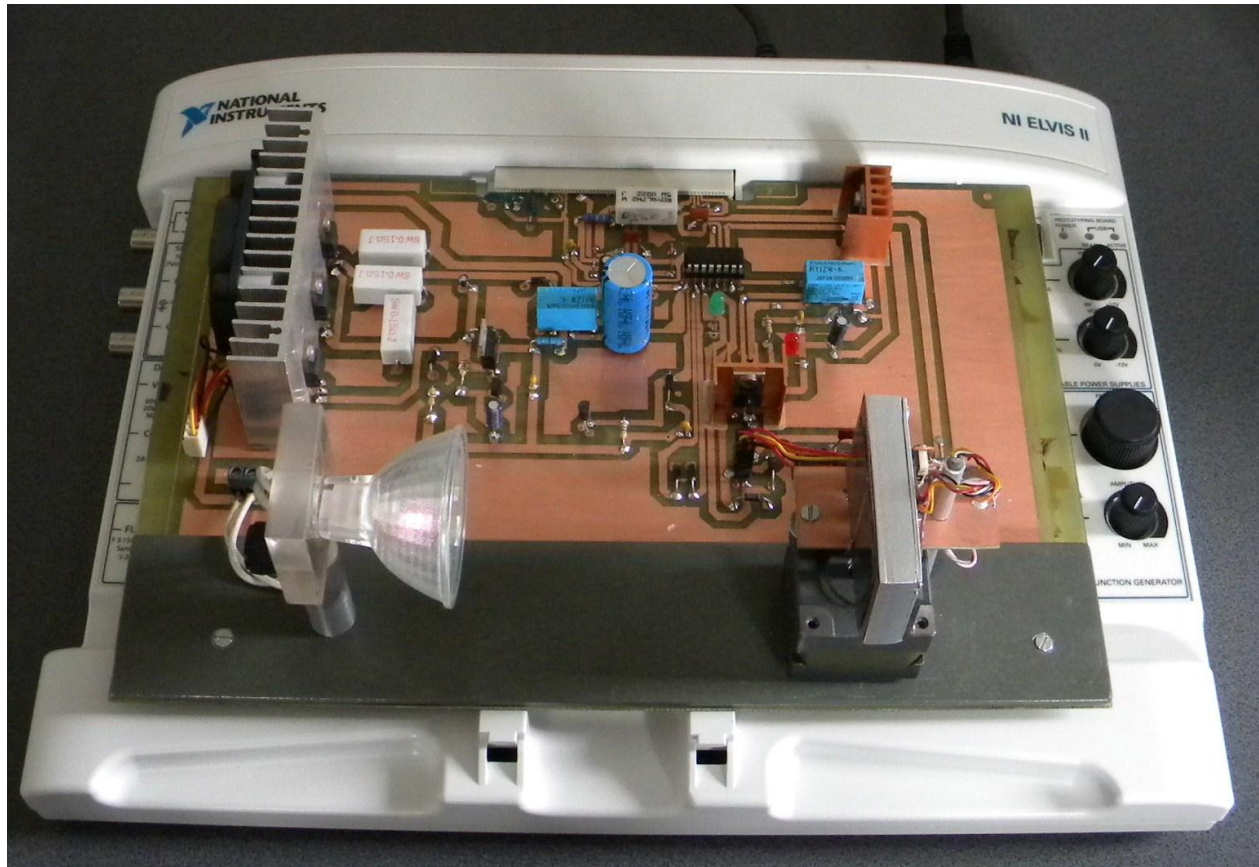
13. 4. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



In case it's still not enough....

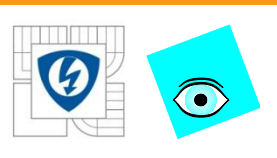
DYI boards for Elvis



13. 4. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

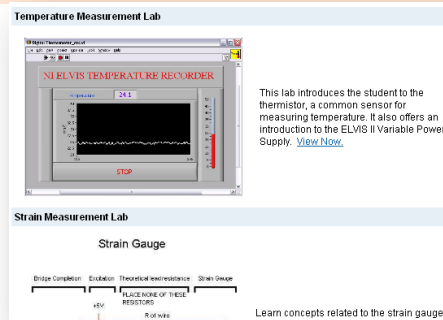




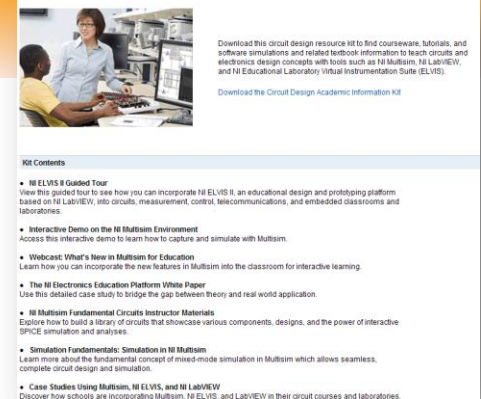
Online Resources



NI ELVIS II Guided Tour



Courseware

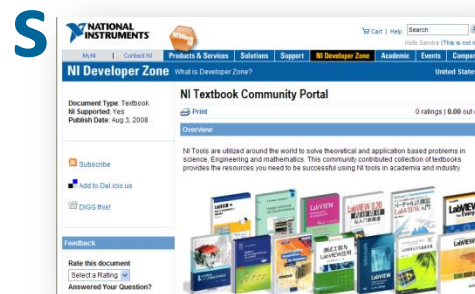


Download Resource Kits

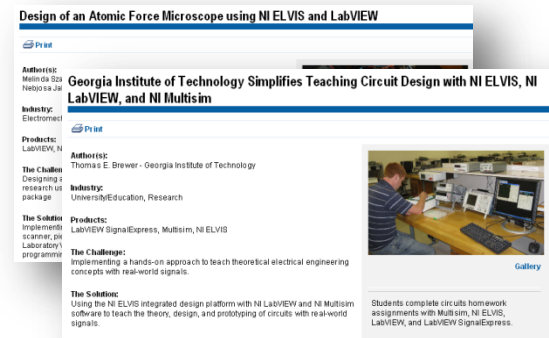
ni.com/nielvi



Webcast



Textbook Resources

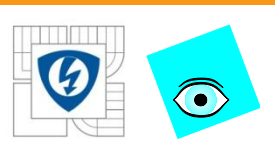


Case Studies & White Papers

13. 4. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





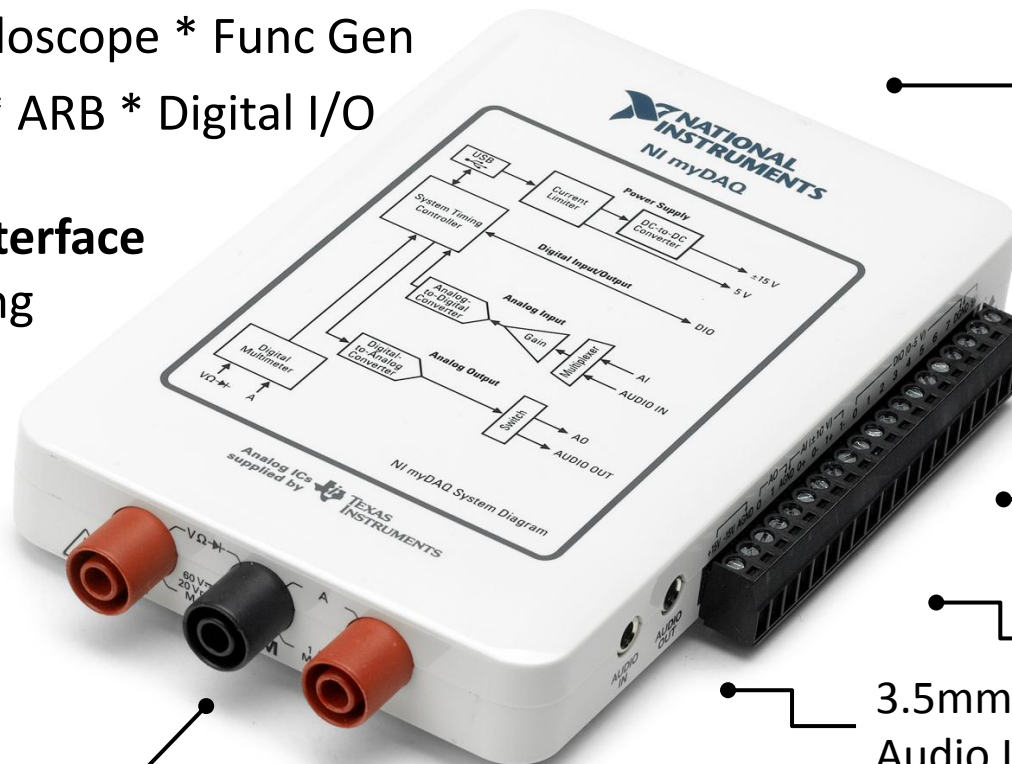
NI myDAQ Features

Plug & Play Instruments

DMM * Oscilloscope * Func Gen
Bode * DSA * ARB * Digital I/O

Computer Interface

LabVIEW using
NI DAQmx



USB Bus Powered

± 15 V and 5V
Power Supply

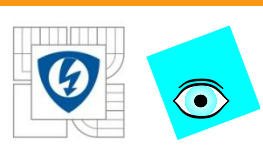
8 Digital In/Out

1 Counter

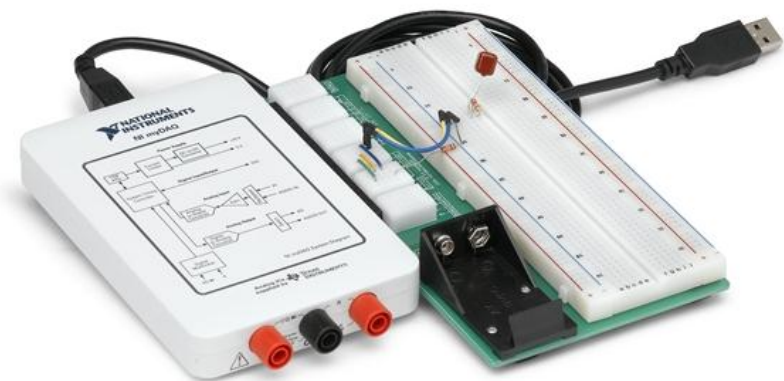
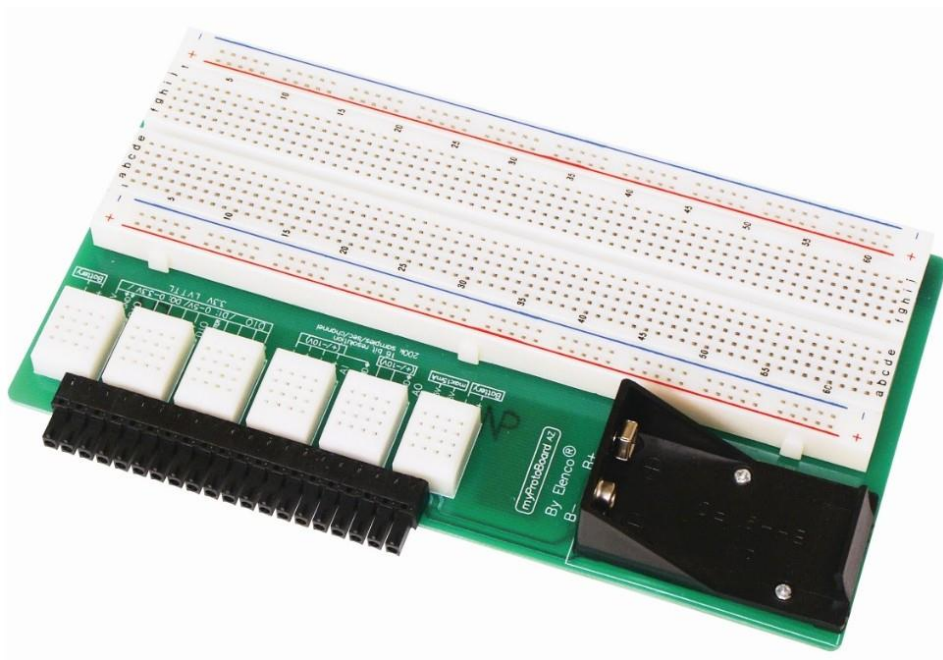
Analog In/Out
2 ch, 200ks/s

3.5mm
Audio In/Out

Integrated DMM
V, I, Ω , Diode



MyDAQ Prototyping Board

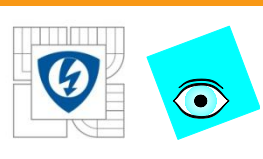


<https://decibel.ni.com/content/groups/mydaq>

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My DAQ connectivity board



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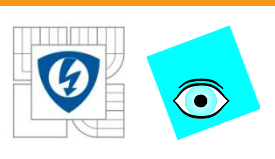
MyDAQ Agroengineering Farm plant



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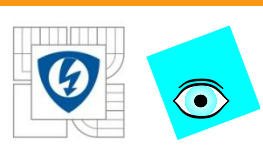
MyDAQ Dynamometer plant



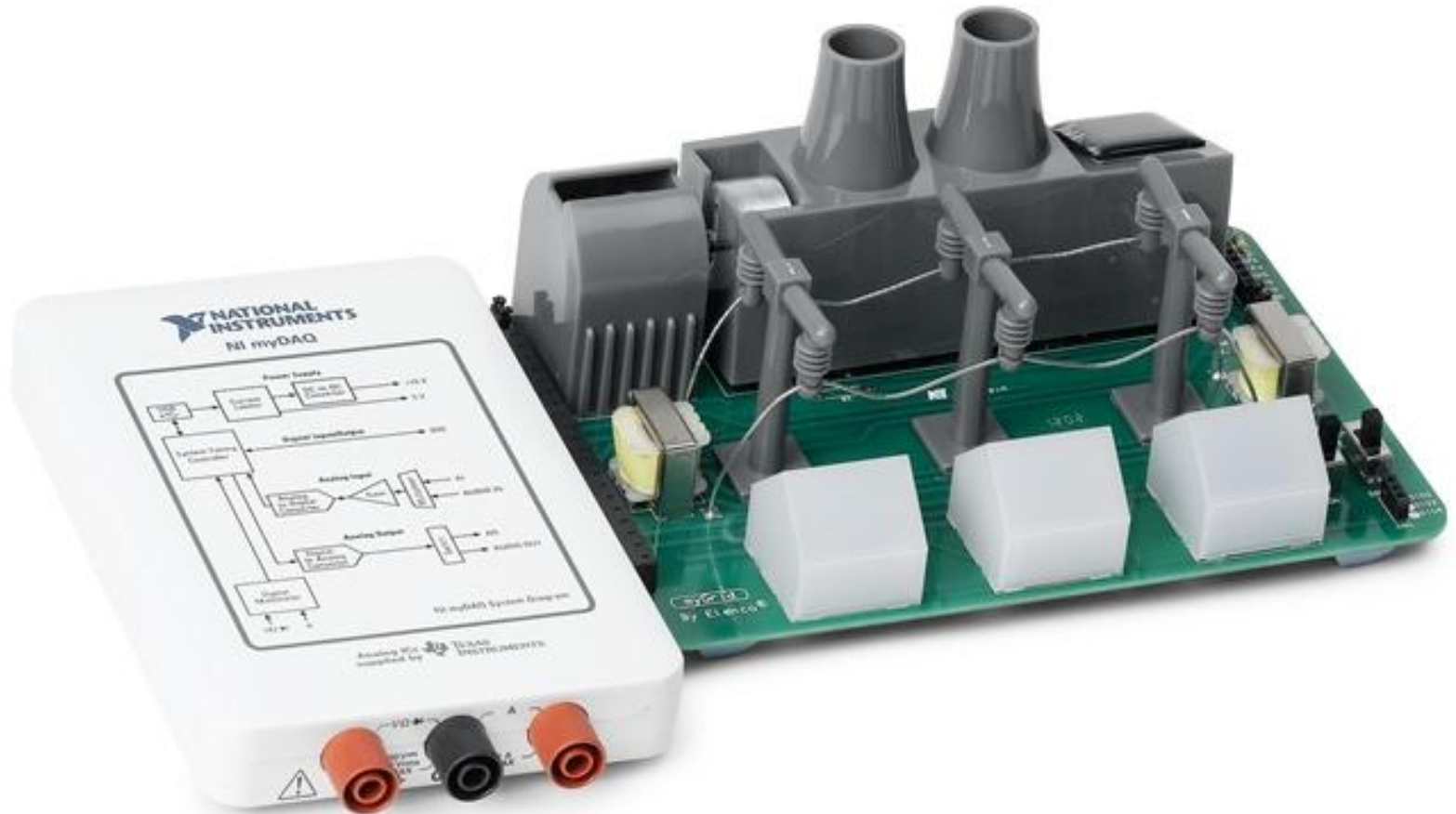
13. 4. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



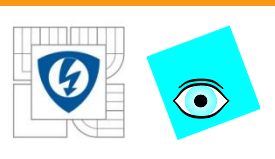


MyDAQ Smartgrid plant



13. 4. 2012

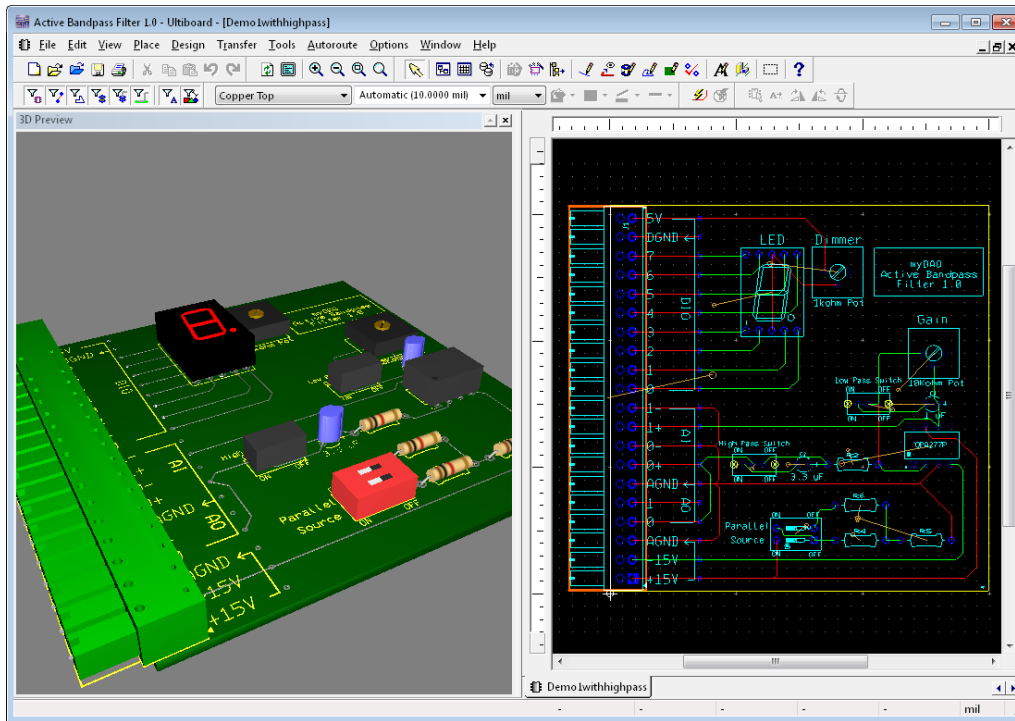
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



Endless Possibilities...

Extend learning with custom modules

- Custom signal conditioning
- Custom control plants
- Experiment kits
- Student design



Custom PCBs & Signal Conditioning



Low Cost Mini-System Experiments

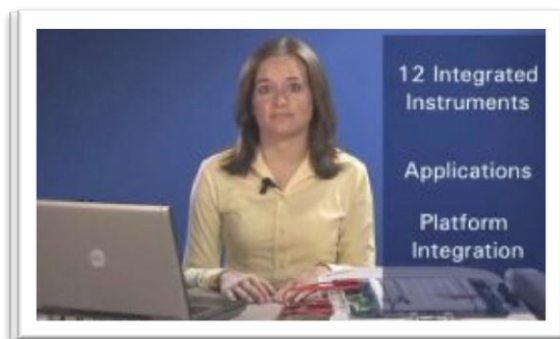
13. 4. 2012

INVESTICE DO ROZVOJE VZDELAVANI
(Custom PCB design templates available in ACM)



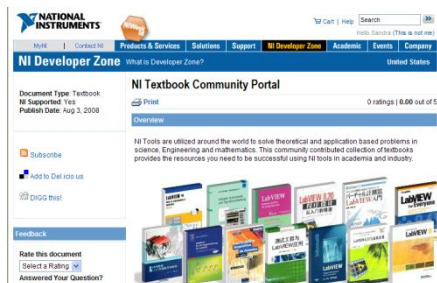


Online Resources

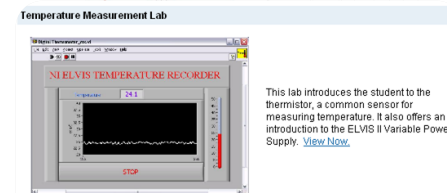


Webcasts

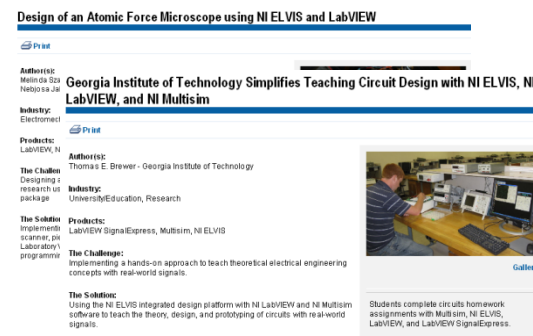
ni.com/academic
ni.com/nielvis



Textbook Resources



Labs & Curricula

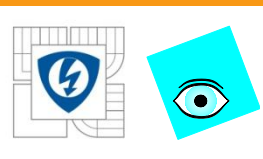


Case Studies & White Papers

13. 4. 2012

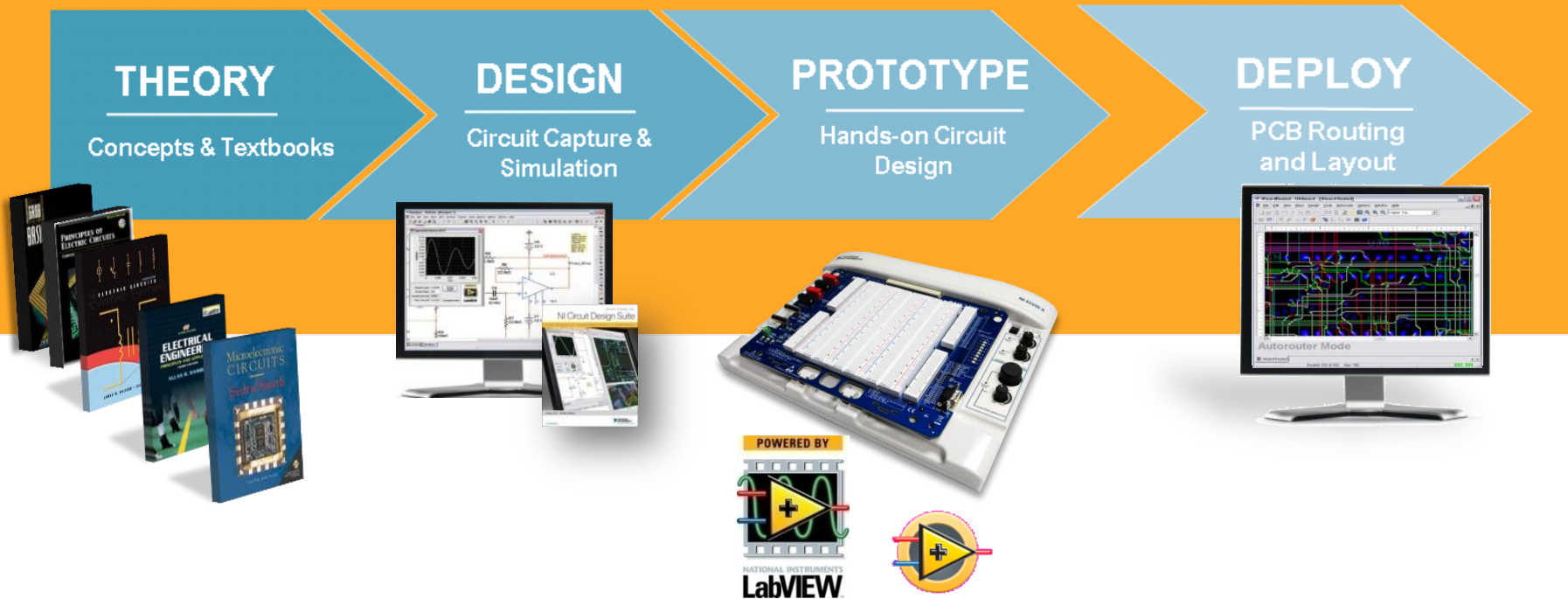
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





NI Electronics Education Platform

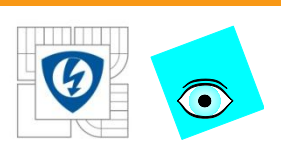
Electronics Education Platform



13. 4. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



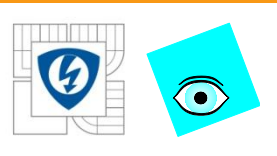


Multisim & Other SW Tools

13. 4. 2012

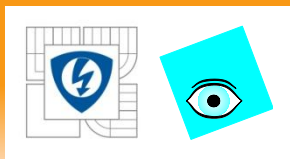
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Agenda

- A. Introduction to the NI Multisim
- B. Schematic Capture
- C. Simulation
- D. Prototyping
- E. Measurement and Comparison
- F. Multisim Addons
- G. other SW tools for co-simulation

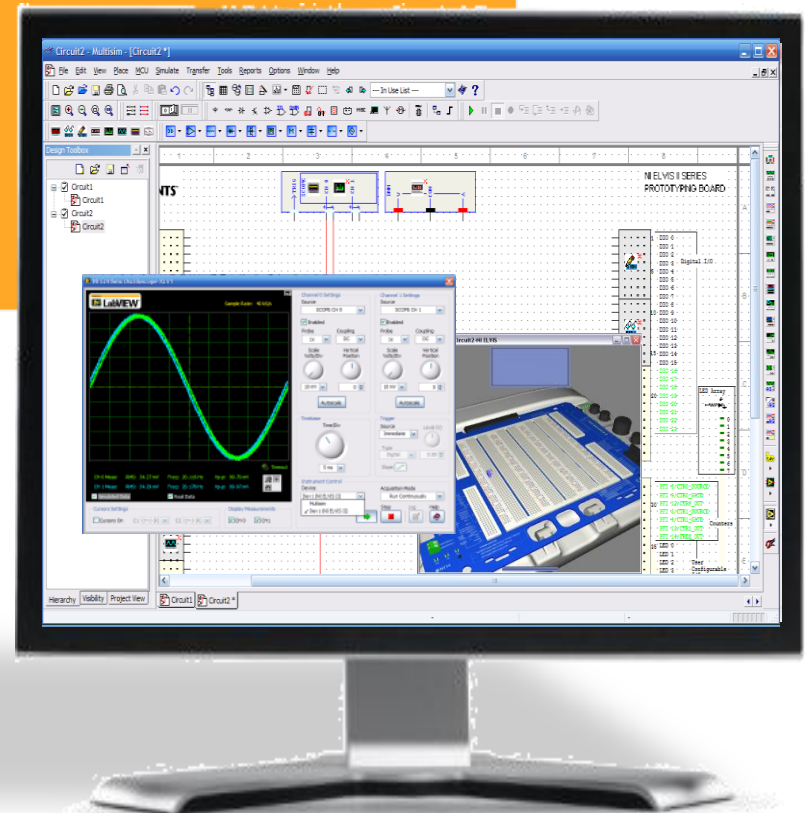


NI Multisim 12

NI Multisim

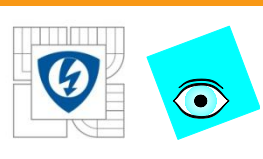
Unified environment for teaching circuit theory and design through capture and simulation

- SPICE-based simulation
- Interactive mixed-mode simulation
- NI ELVIS instruments inside Multisim
- 20 SPICE analyses
- 22 measurement instruments
- MCU simulation support
- Power and Machine components (motors..)
- PLD design tools
- Multisim and LabView Co-Simulation



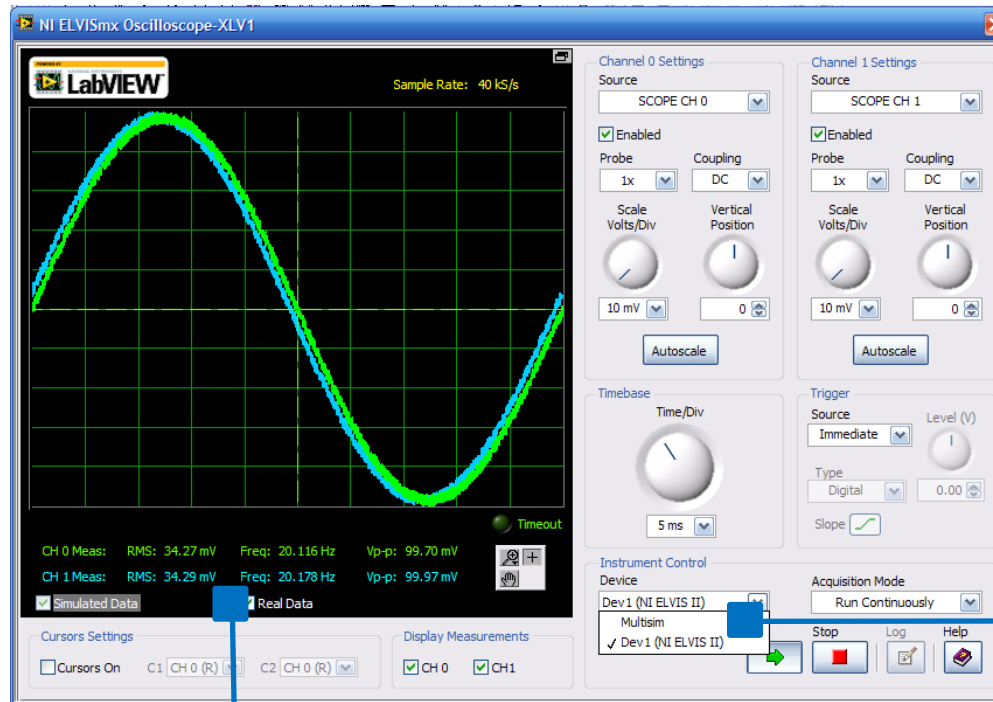
13. 4. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

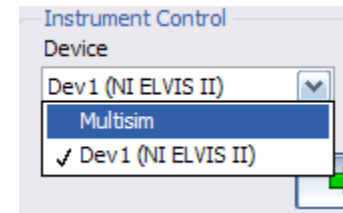


Theory and Measurement

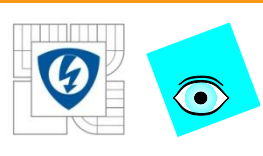
Compare simulated data and measured signal on the same instrument



Access NI ELVIS hardware With one click switch between simulated signals and acquiring signals from your NI ELVIS II hardware

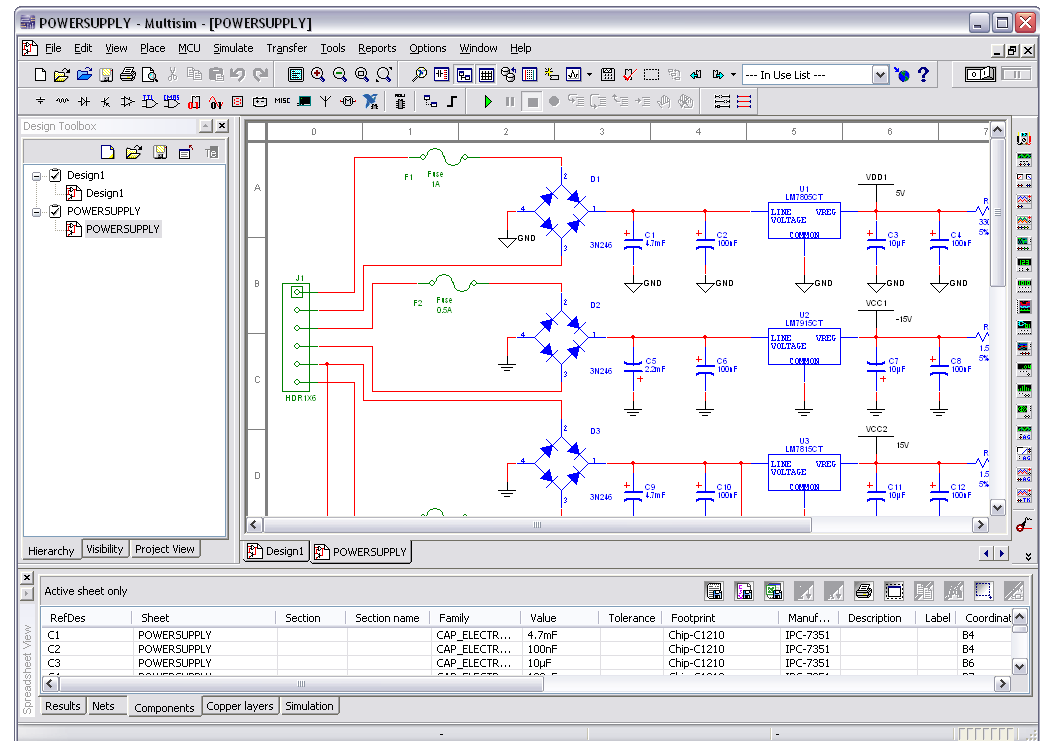


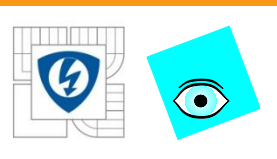
NI ELVIS II Instruments Compare simulated Multisim data with measured signals from NI ELVIS II within Multisim



What is Multisim?

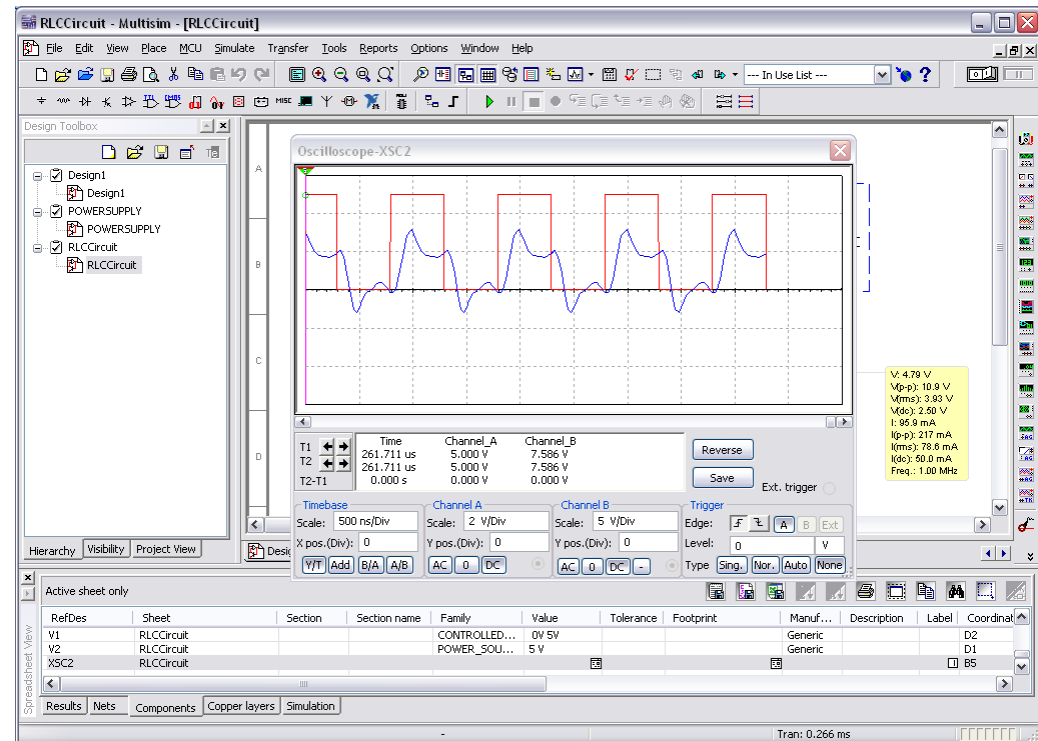
- General purpose EDA tool
- Schematic Capture
- Simulation
- Analyses
- Integrated Environment



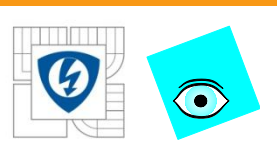


Benefits of Integrated Capture & Simulation

- Preparation for simulation is as simple as drawing a circuit
- Interactive Simulation
- Animated Parts
- Virtual Instruments
- Analyses and Graphs



Effective use of your time!



The Design Process

Where does Multisim fit in the design flow?

 **NI Multisim™**

 **NI Ultiboard™**

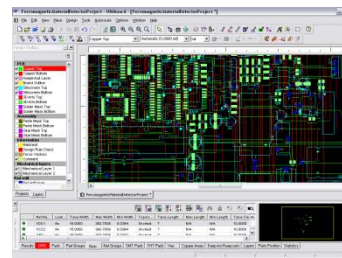
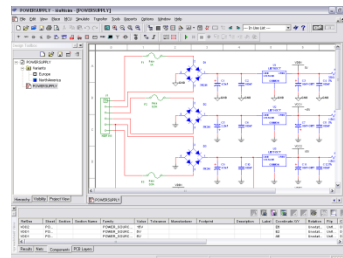
 **LabVIEW™**

Part Selection

Capture &
Simulation

Layout

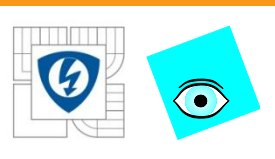
Verification



13. 4. 2012

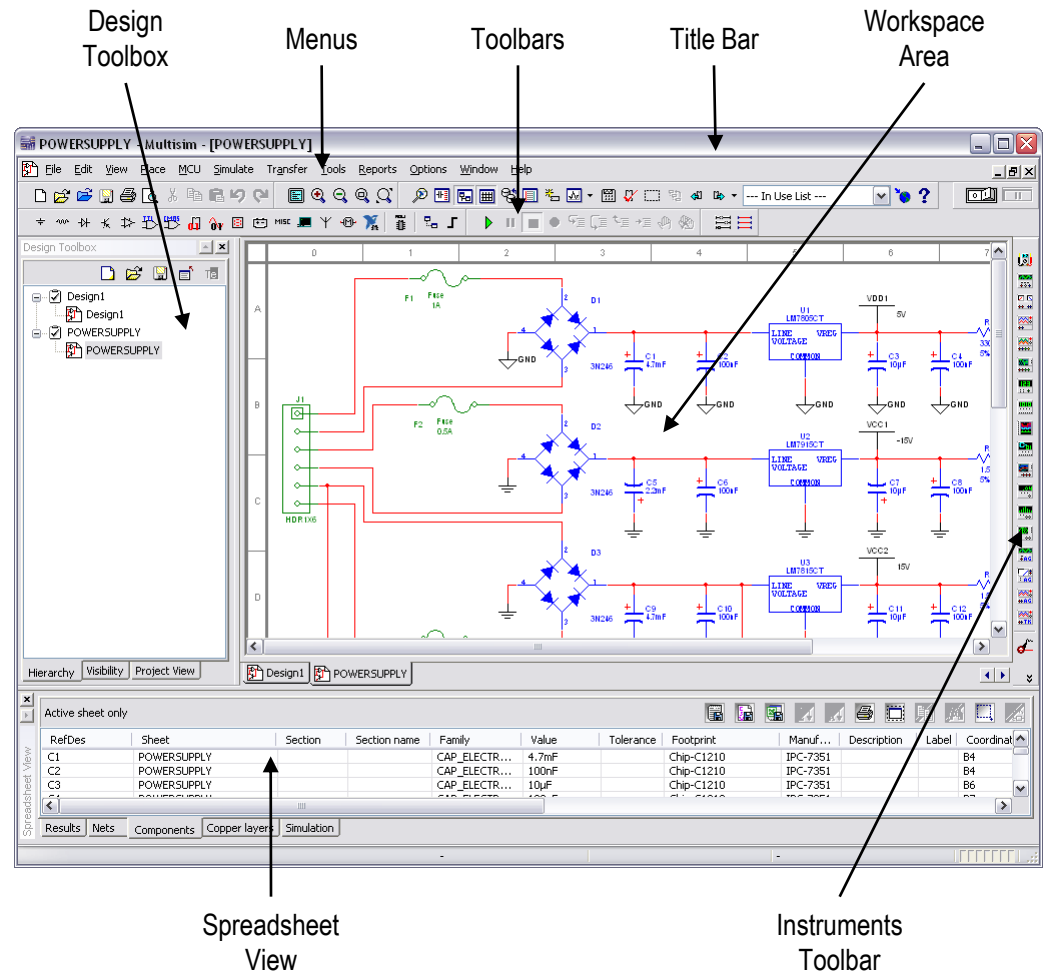
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





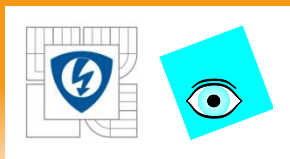
The Multisim GUI

Organized menus
Quick access toolbars
Design Toolbox
Spreadsheet View
Resizable Workspace



13. 4. 2012

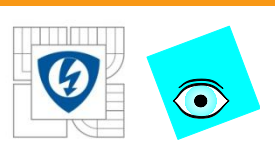
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



Global Preferences



- **Options»Global Preferences**
- Vary from computer to computer
- Stored in the User configuration file
 - Change config file and database paths
 - Save settings (security copy, backup, simulation data)
 - Component Placement mode, symbol standard
 - Rectangle behavior, mouse wheel behavior, bus wiring
 - Message prompts and general simulation settings

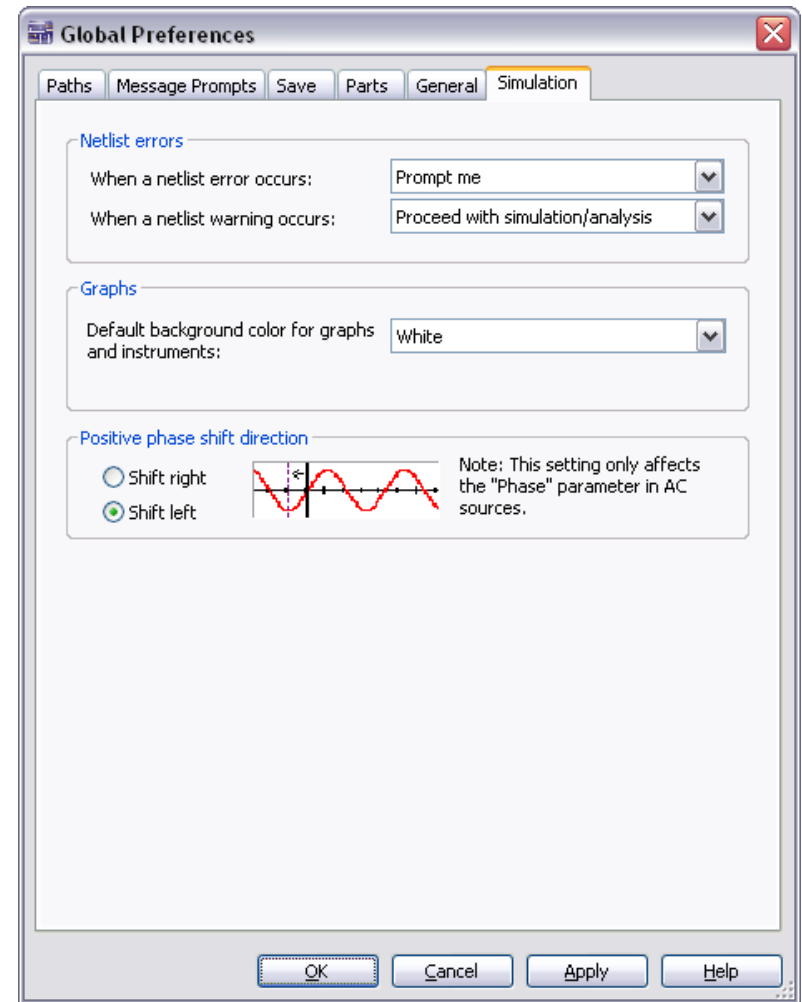


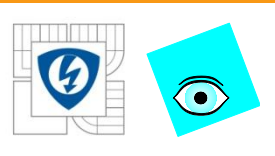
Global Preferences

Simulation tab



- Netlist errors action
- Default background
- Phase shift direction



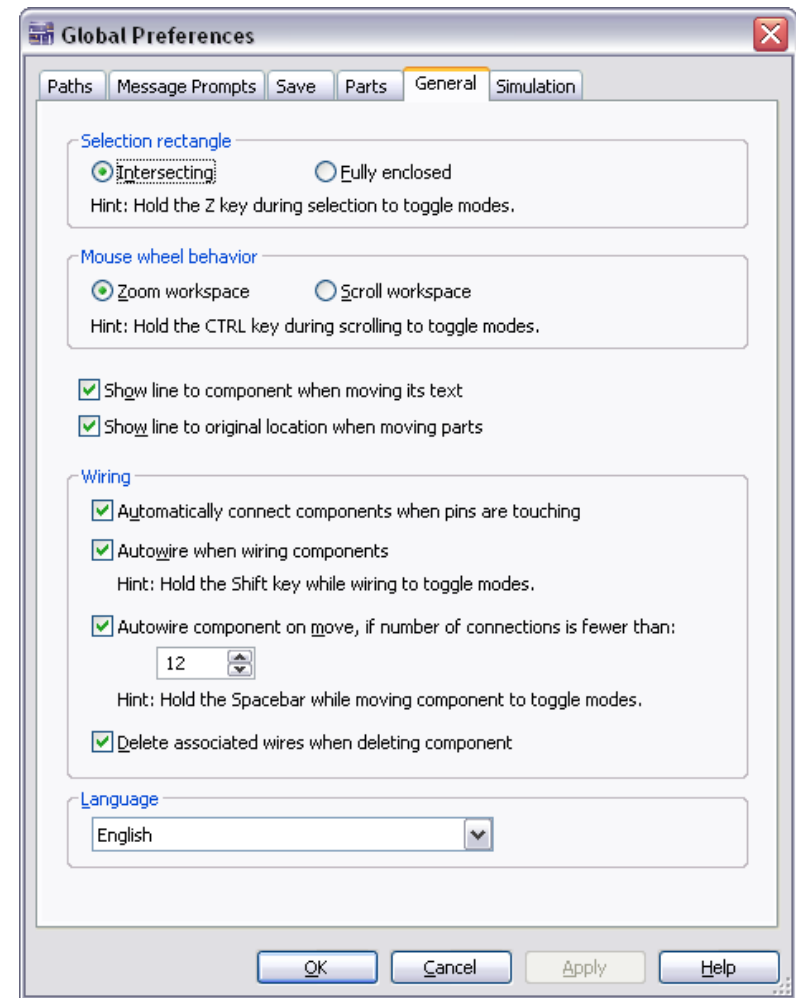


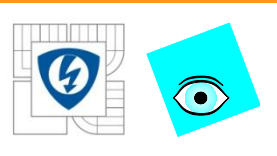
Global Preferences

General tab



- Selection rectangle
- Mouse-wheel behavior
- Wiring mode
- Localization





Sheet Properties

- **Options»Sheet Properties**
- Saved with the design file, if opened in another computer same settings will be used.
 - Color scheme and display properties
 - Sheet size
 - Wire and bus options
 - Font properties
 - PCB settings
 - Visibility status for annotation layers

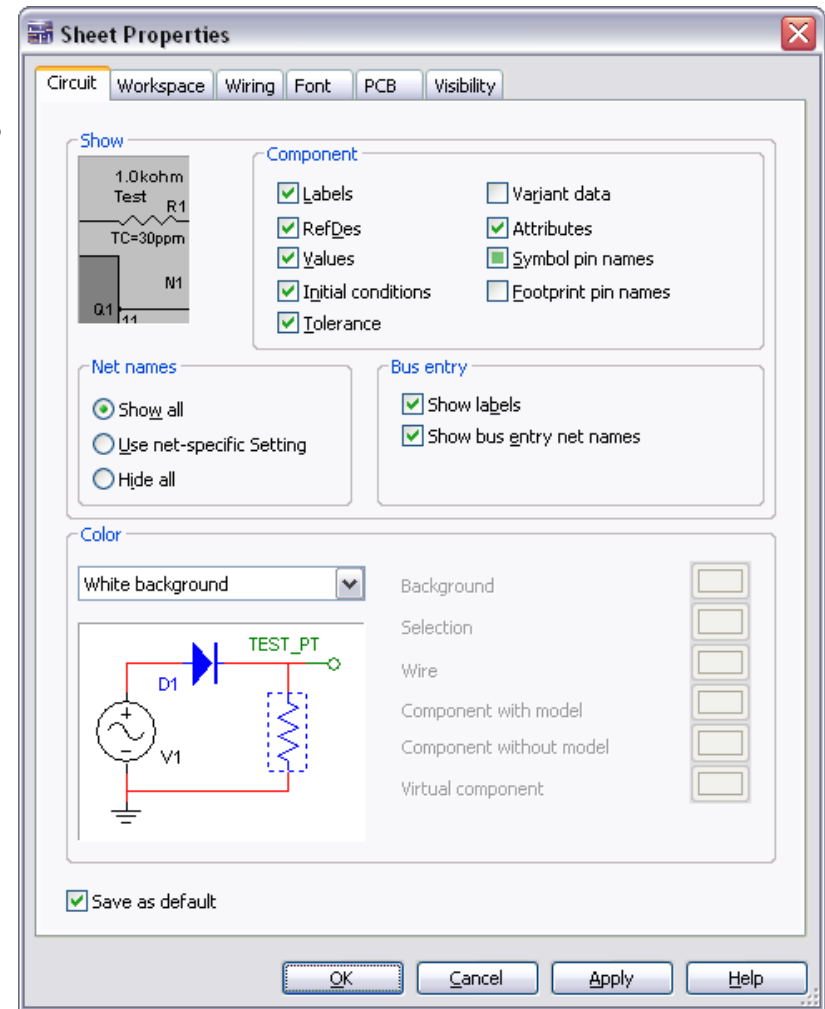


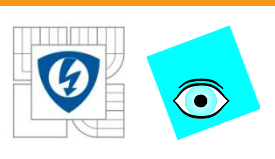
Sheet Properties – Circuits tab

- Component display properties
- Net names display properties
- Bus entry display properties
- Color scheme



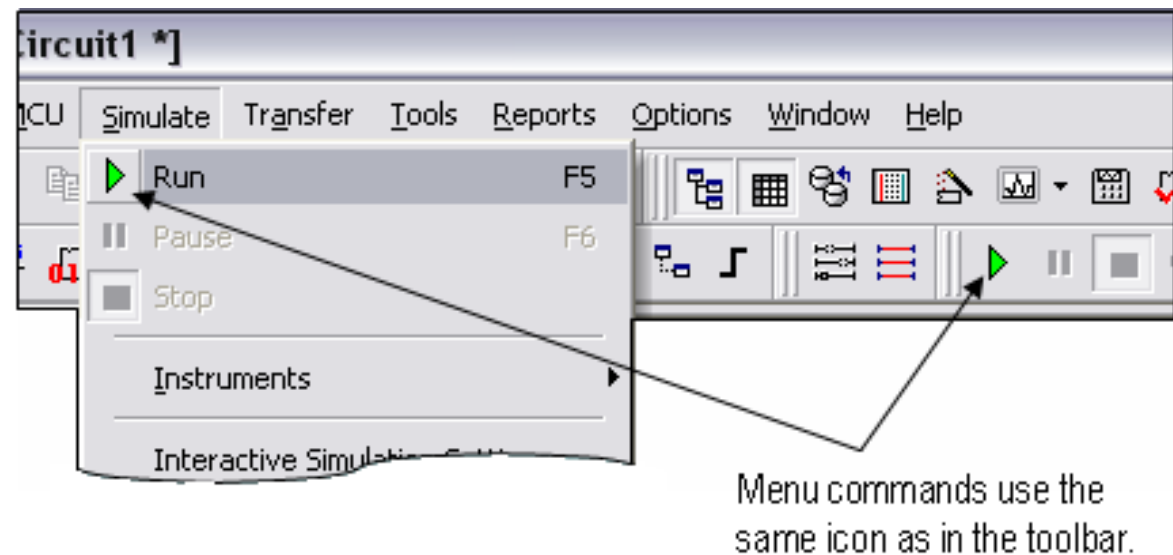
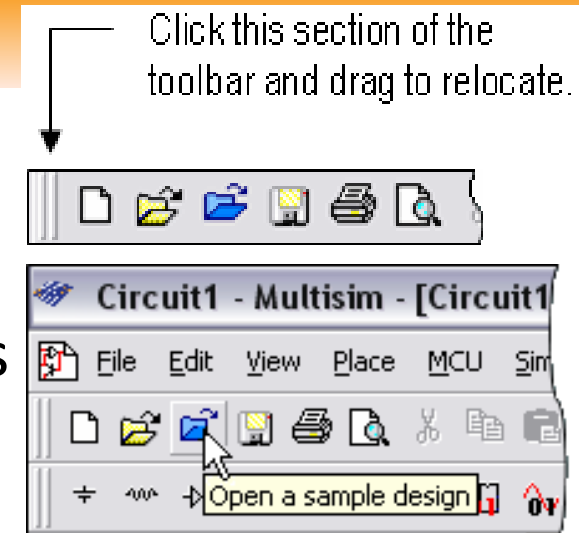
Tip: Experiment with changing the display properties of components, keep a balance between good visibility and optimum information display.

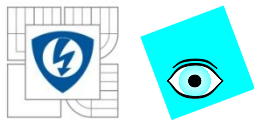




Toolbars and Menus

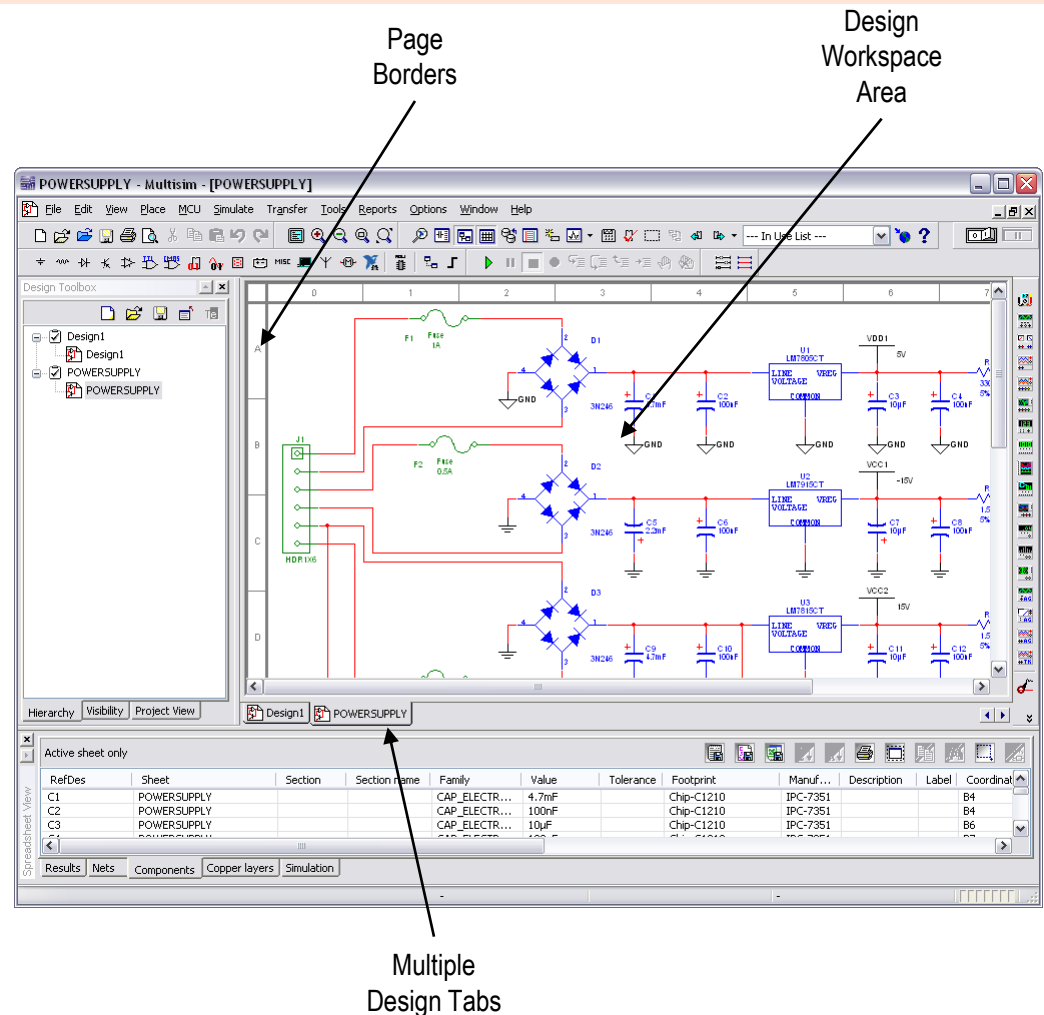
- Organized based in functionality
- All toolbar functions found in menus
- Right-click toolbar area and toggle toolbars
- Customizable (functions, location)
- ToolTips
- Lock toolbars

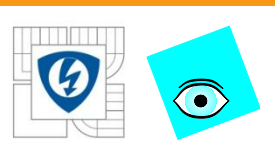




Workspace Area

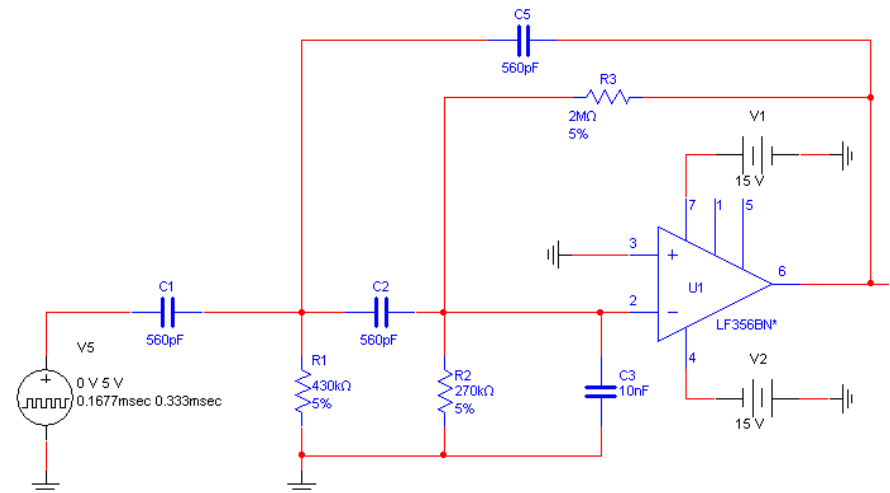
- Schematic area
- Multiple tabs
- Zoom in and out with the mouse wheel (default)
- Use **View** menu to show/hide Grid and Page Border





Schematic Capture

- Multisim offers click-and-place capture mode
- Integrated with simulation



Three step process:

Select

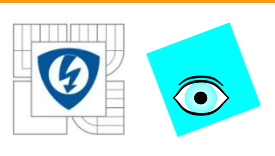
Component Database
In-Use List
Copy
Replace

Place

Rotate
Flip
Multi-section

Wire

Automatic
Touching-pins
Dropping

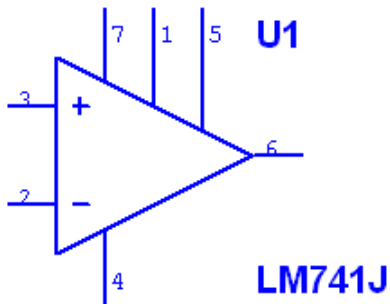


Components

- Symbolic representation of actual parts
- All components have a symbol
- Many components have a SPICE model and footprint

Capture Area

Symbol



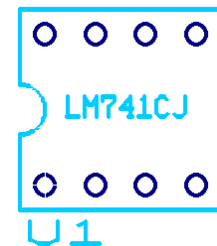
Simulation Engine

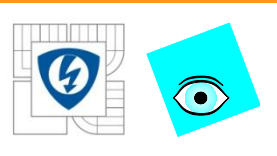
SPICE Model

```
.SUBCKT LM741 1 2 3
* 3 Terminal Op-amp Model
* A= 200000 RI= 2e+006 RO=
* Vos= 0.001 Ibs= 8e-008 I
* fu= 1.5e+006 fp2= 1e+032
Vos 4 1 DC 0.001V
Ib1 4 0 9e-008A
Ib2 2 0 7e-008A
G1 0 5 4 2 0.0584804
G2 0 6 5 0 0.779738
G3 0 3 6 0 0.779738
Ri 4 2 2e+006ohm
R1 5 0 1000ohm
R2 6 0 75ohm
R3 3 0 75ohm
C1 5 0 2.12207e-005
C2 6 0 2.12207e-035
Cc 5 0 3e-011
.ENDS
```

PCB Layout

Footprint



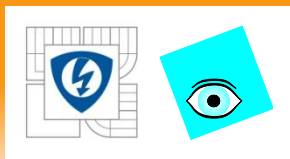


Components – Properties

- Double-click component to:
 - Change Label, RefDes
 - Display properties
 - Value
 - Faults
 - Check Pin assignment
 - Set Variant information
 - Modify User Field information

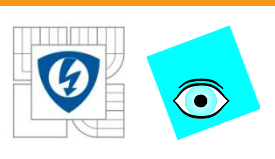
In the **Value** tab, click **Edit Component in DB** to customize the component.

(not for RLC components)



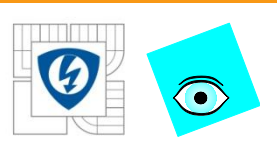
Components – Edit Component in DB

General	Component name, creation date, author, function.
Symbol	Number of pins, number of sections, symbol set, edit/copy symbol, pin mapping table.
Model	Model name, model data, add/edit/delete model, pin mapping table.
Pin Parameters	Component type, pin table.
Footprint	Footprint type, add/delete/change footprint, symbol pin to footprint pin mapping table, footprint preview.
Electronic Parameters	Common parameters, device specific parameters.
User Fields	User-defined fields.

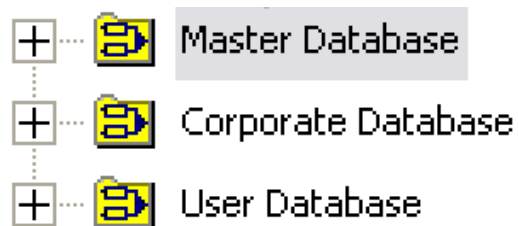


Components – Virtual, Real, Layout-only

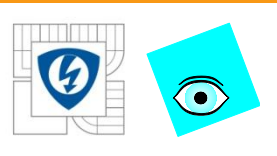
Component	Symbol	Model	Footprint	Default Color
Virtual (simulation only)	✓	✓	✗	
Real (simulation and layout)	✓	✓	✓	
Layout-only (layout only)	✓	✗	✓	



- **Tools»Database»Database Manager**
- Three levels:



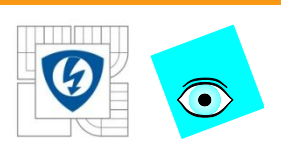
- Parts bin up to 17,500 parts (Power Pro edition)
- Master database cannot be edited
- Database utilities let you merge other user's database, or convert a database from a previous version



- **Corporate database**
 - Share components with colleagues
 - Located in local disk or network drive
- **User database**
 - Store your own custom components
- If you modify a Master database component, save it into the Corporate or the User database.



Caution: Always backup your Corporate or User database.

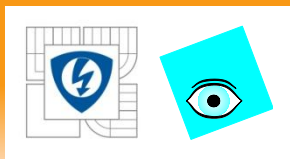


Component Browser

- **Place»Component**
- Most common tool to place components.
- You can select:
 - Database
 - Component
 - Model
 - Footprint
 - Search for components



Tip: Right-click anywhere in the workspace and select **Place Component** to access the **Component Browser**.

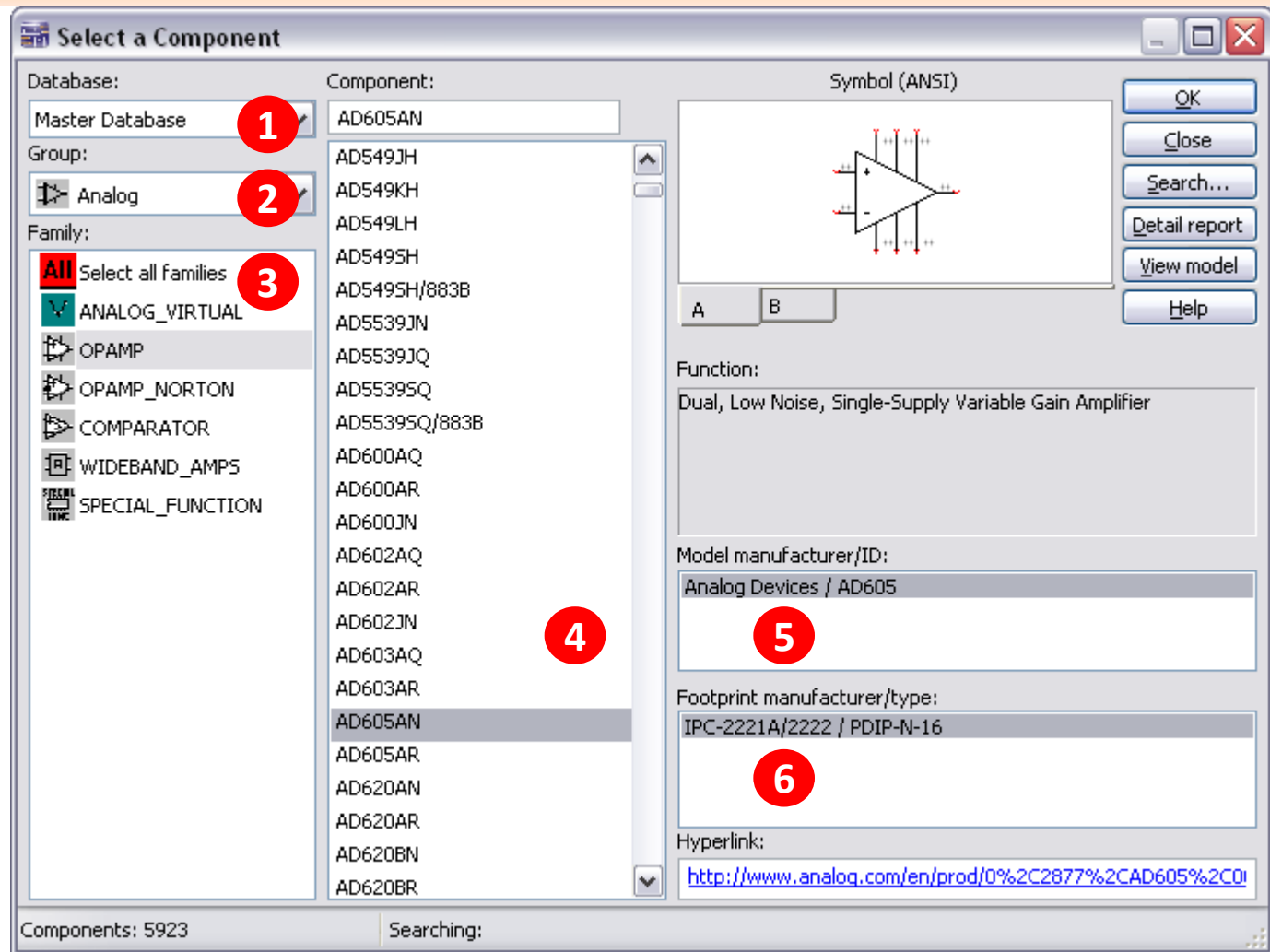


To place a part,
select:

1. Database
2. Group
3. Family
4. Part
5. Model
6. Footprint

You can also:

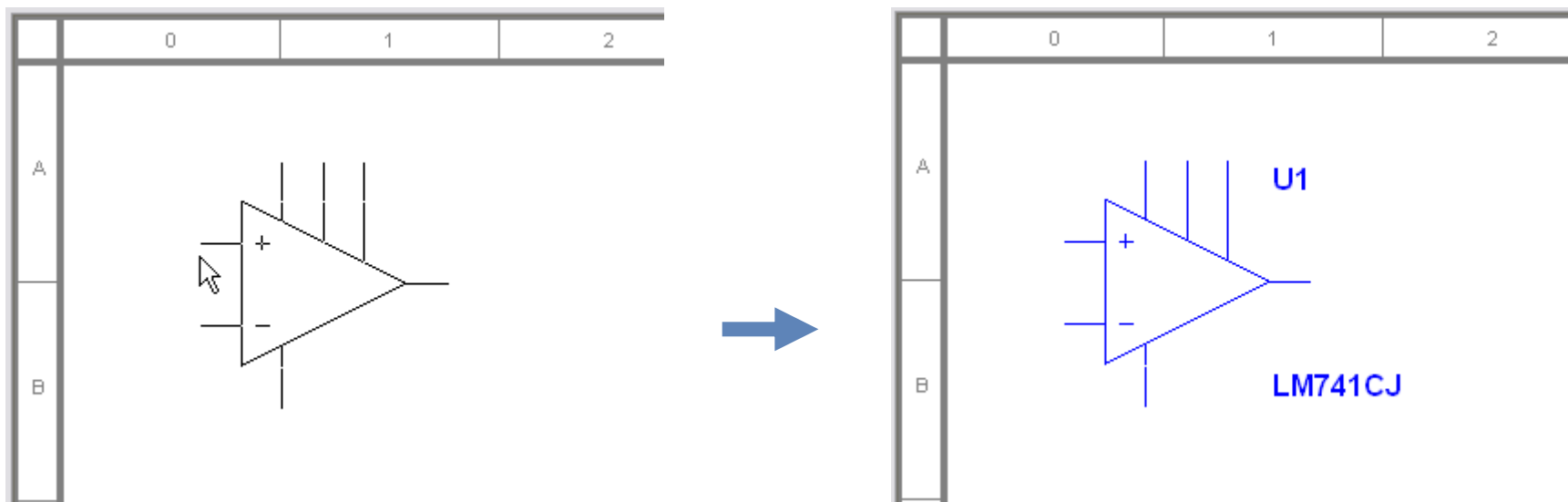
- Search
- Obtain datasheet
- Print a detail report
- View model

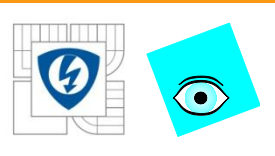




Placing a Component

- After selecting a component, a ghost image is attached to the mouse pointer
- Click to place
- Next RefDes is assigned

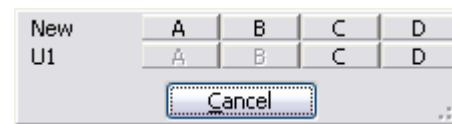




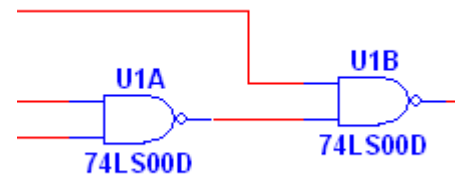
Placing Multi-section Components

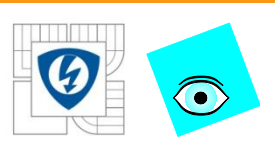
Select any section for
a new IC

Select C or D to place
unused sections of
U1



U1, section A and B are already
placed, therefore they are not
selectable



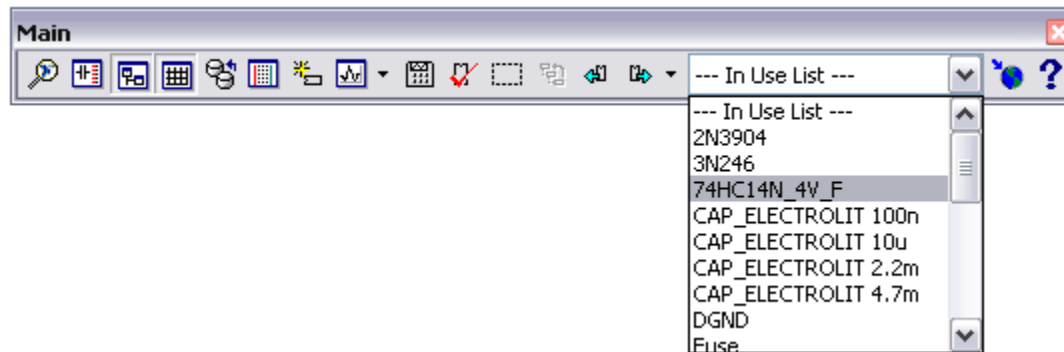


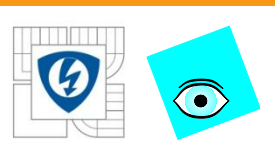
Component Toolbar and the In-Use List

- Access Master database **Groups** from the **Components** toolbar.



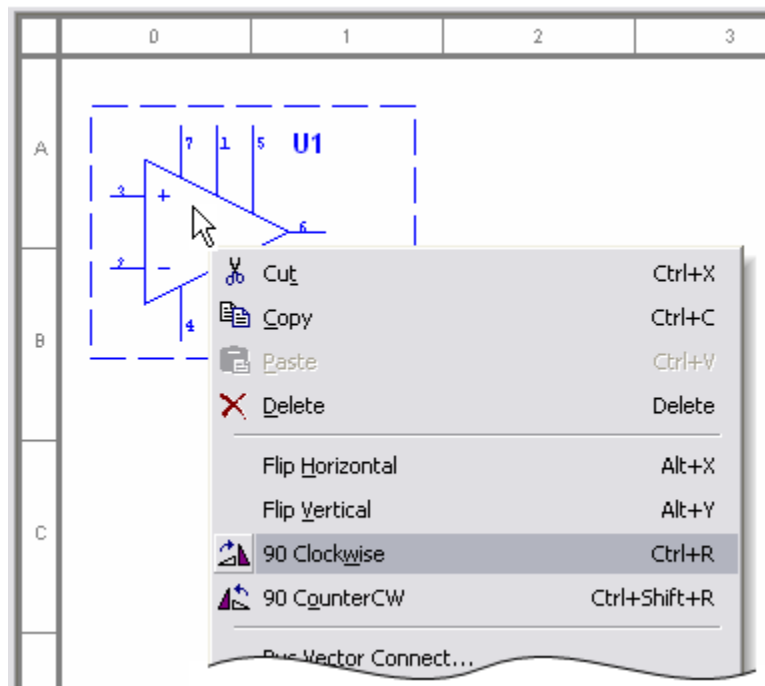
- Use the **In-Use List** to place another instance of an already placed component.





Rotating a Component

– If already placed



• While placing

While dragging the component...

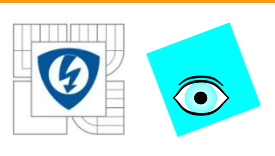


Press <Ctrl+R>...



Then click to place.

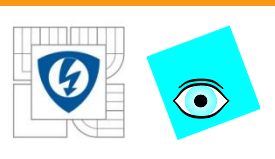




Component Search

- From the **Component Browser**, click **Search**
- Use ***** as a wildcard

Title	Value
Vendor	
Status	
Price	
Hyperlink	
Manufacturer	
Manufacturer Part No.	



Component Search – Results

Number of components matching search criteria

List of components matching search criteria

Search Results

Component(s) found: 127

Family: ALL

Component:

- 1N4741A
- 741
- 74100J
- 74100N
- 74107N
- 74109N
- 7410N
- 74116N
- 74125N
- 74126N
- 7412N
- 74132N

Function:

Model manufacturer/ID: IIT\1N4741A

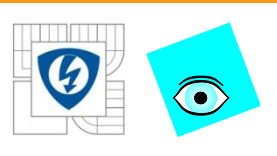
Footprint manufacturer/ID: IPC-2221A/2222\DO-41

Buttons: Refine search, < Back, OK, Cancel, Help

Title	Value
Vendor	
Status	
Price	
Hyperlink	
Manufacturer	

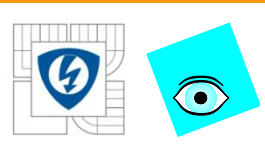
OK will take you to the exact database location

Details of component selected



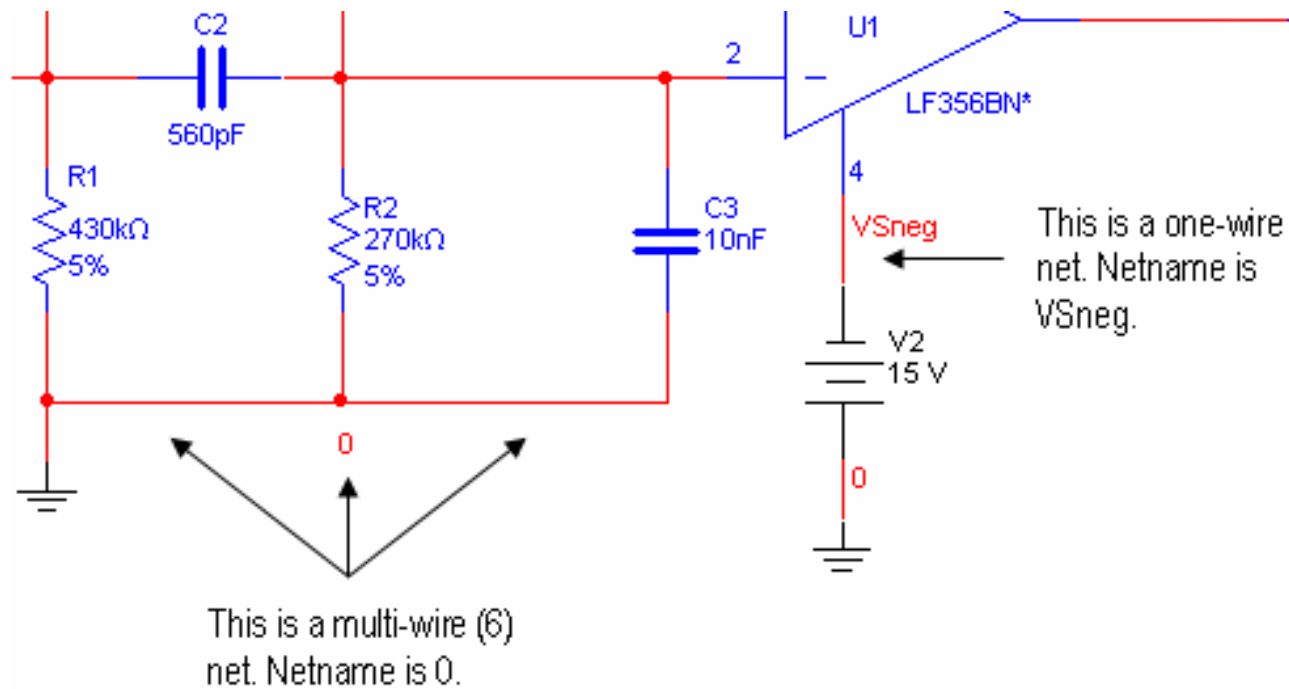
Nets

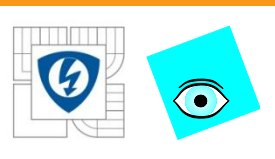
- Wires are the graphical representation of nets
- Modeless (*no placing vs. wiring mode*)
- Mid-air wiring is allowed
- Real-time netlist is updated behind the scenes
- Easy to change wire connections once placed



Nets

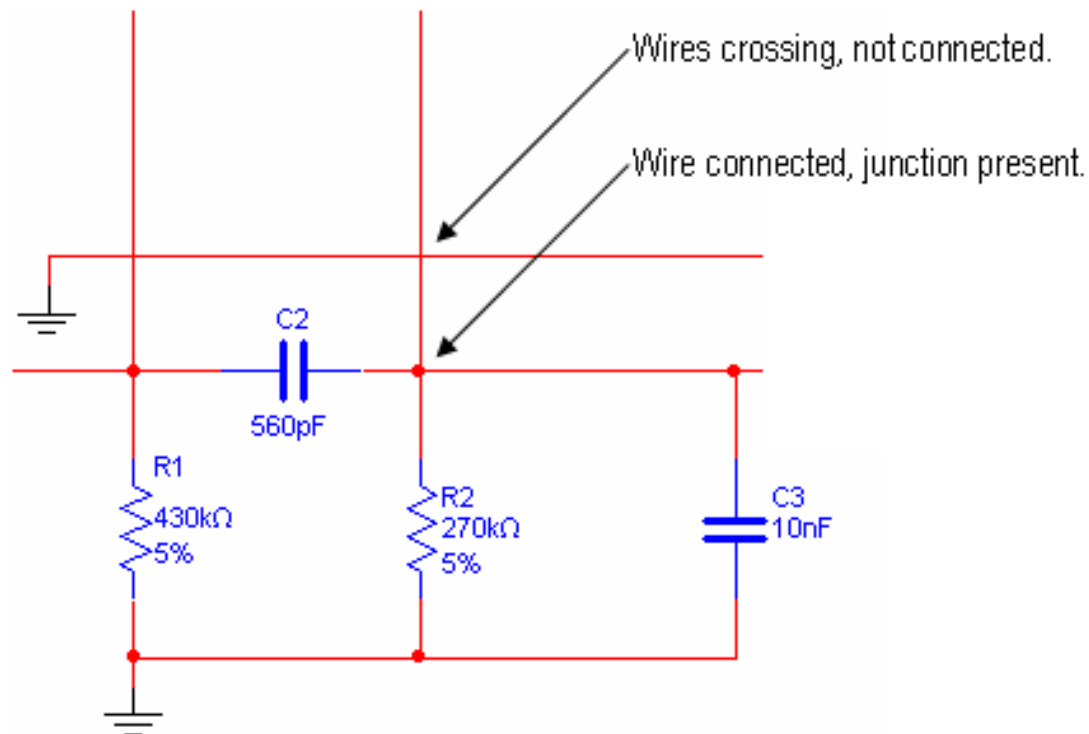
- Multiple wires can make one net or node

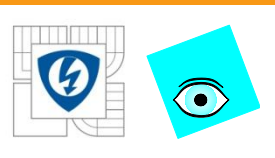




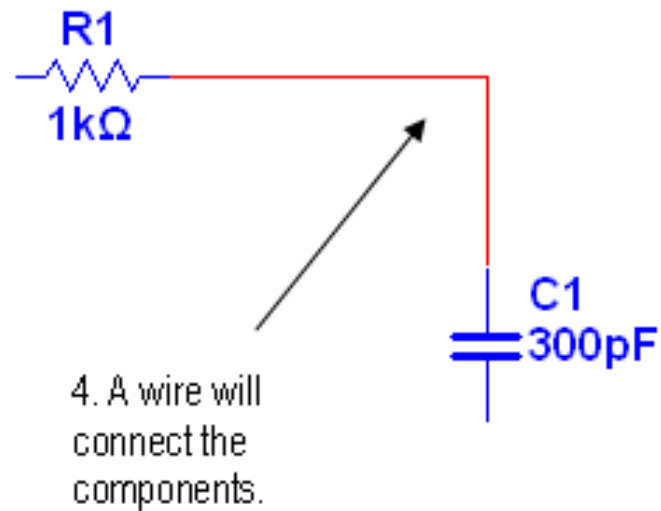
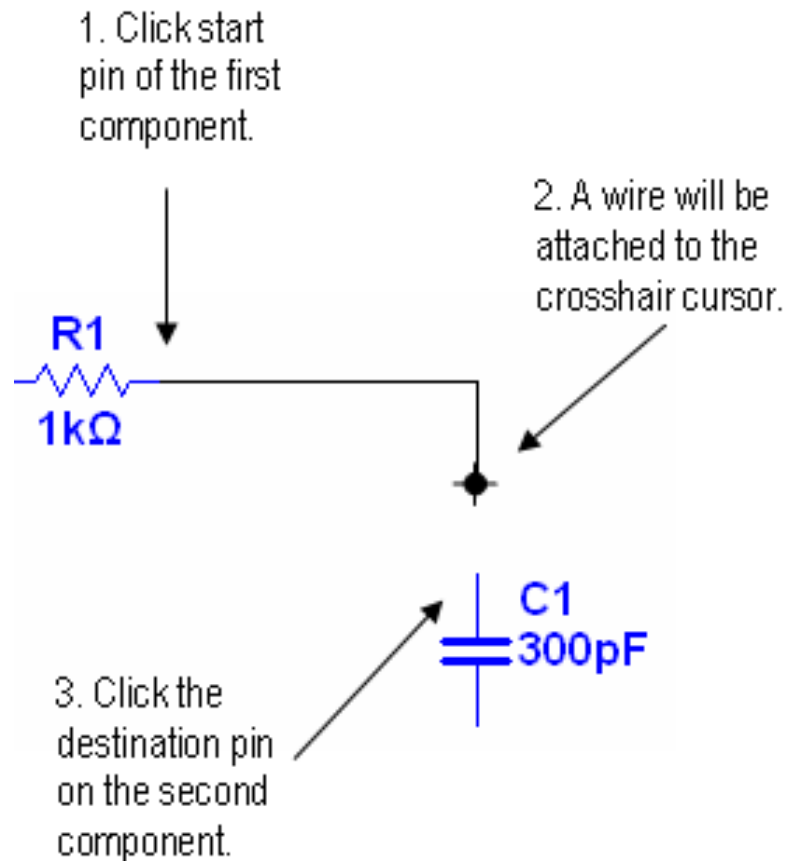
Junction Dots

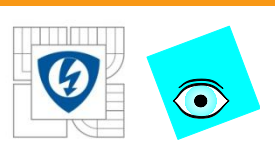
- Junction dots represent a wire connection





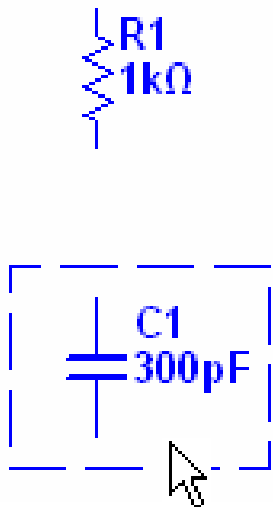
Methods for Wiring – Automatic



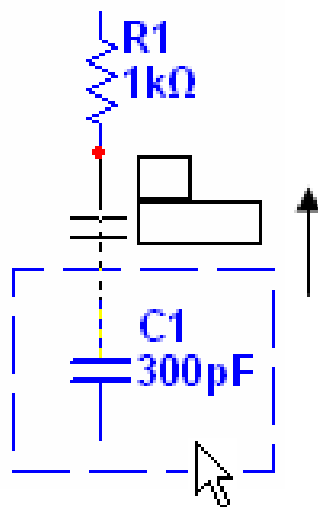


Methods for Wiring – Touching Pins

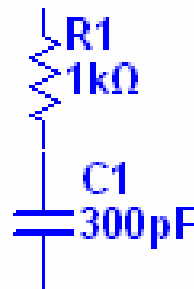
1. Select the component to wire.



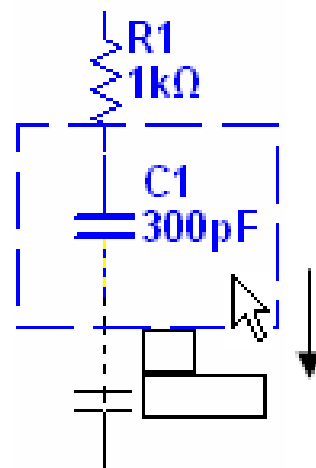
2. Move component and touch pins to be wired. Notice red dot.



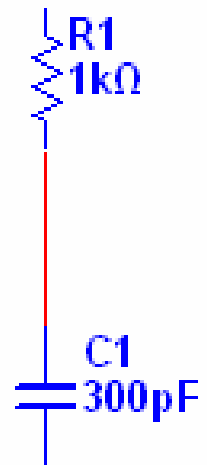
3. Drop the component. Connection is made.

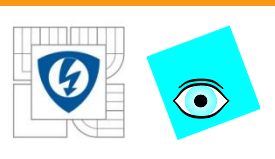


4. Drag the component away.



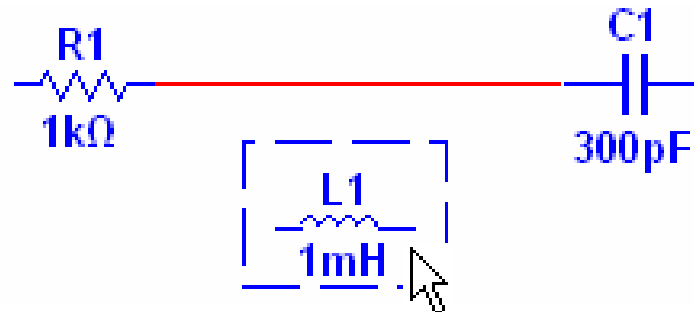
5. Drop the component. Wire is ready.



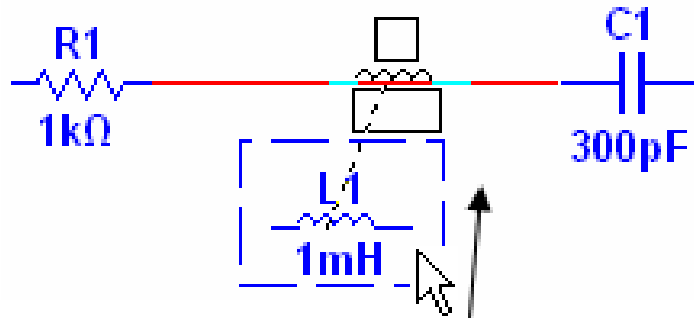


Methods for Wiring – Dropping

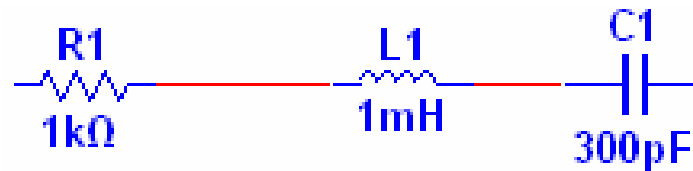
1. Select component to wire.

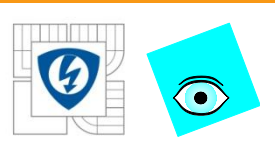


2. Move the component and place it over the wire to be connected in series.



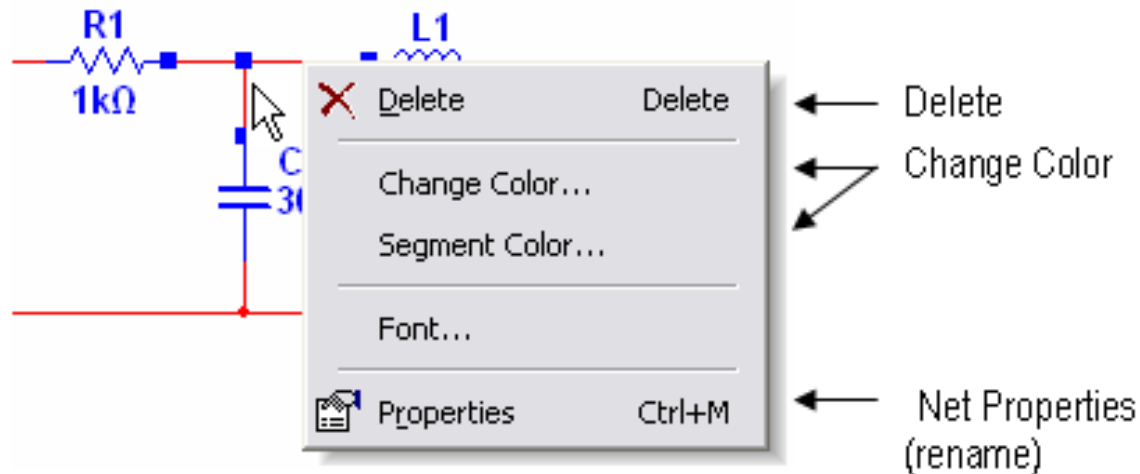
3. Drop the component. The connection is made.

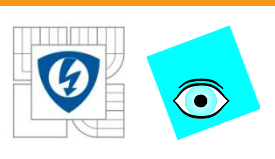




Changing Wire Properties

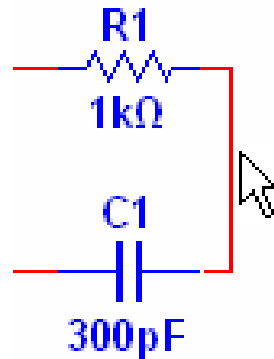
- Right-click the wire to access the run-time menu
- Change colors, net name font and properties



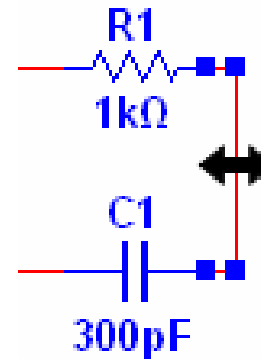


Moving Wires

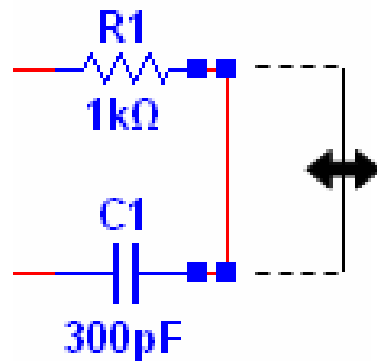
1. Click the segment of interest.



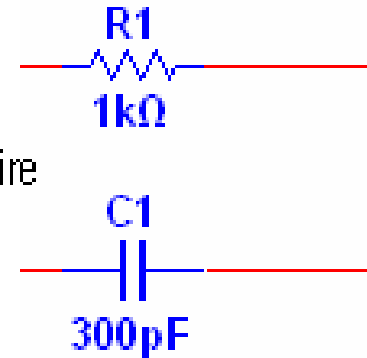
2. Notice the drag points and double arrow cursor.

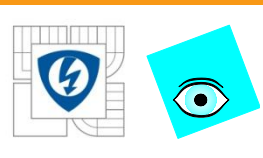


3. Drag the line to the new position.



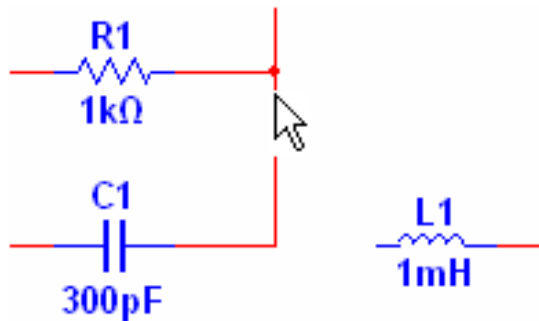
4. Click to drop the wire and finish.



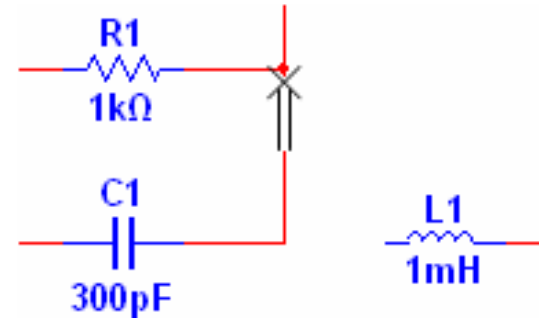


Re-wiring a Net

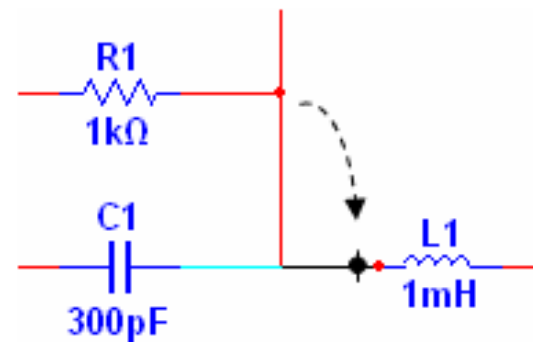
1. Move cursor close to pin or junction.



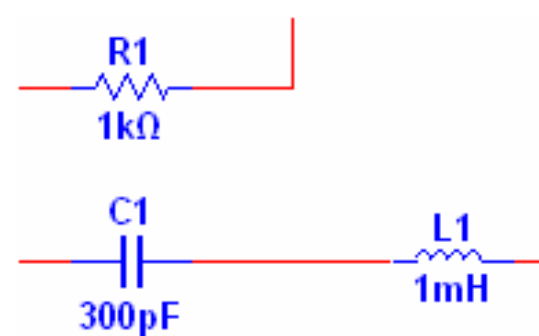
2. When cursor changes click to attach wire to cursor.

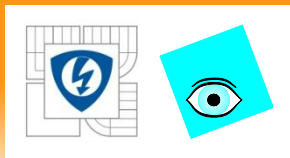


3. Click on new location to connect.



4. New connection is ready.





Virtual Wiring

- Useful in large designs
- Avoids unnecessary wires crossing the schematic
- Give a net a name that already exists to create the virtual connection
- Use Global or On-page connectors



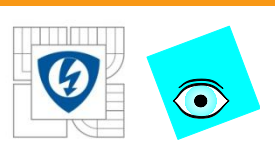
Global connectors are visible to the whole design



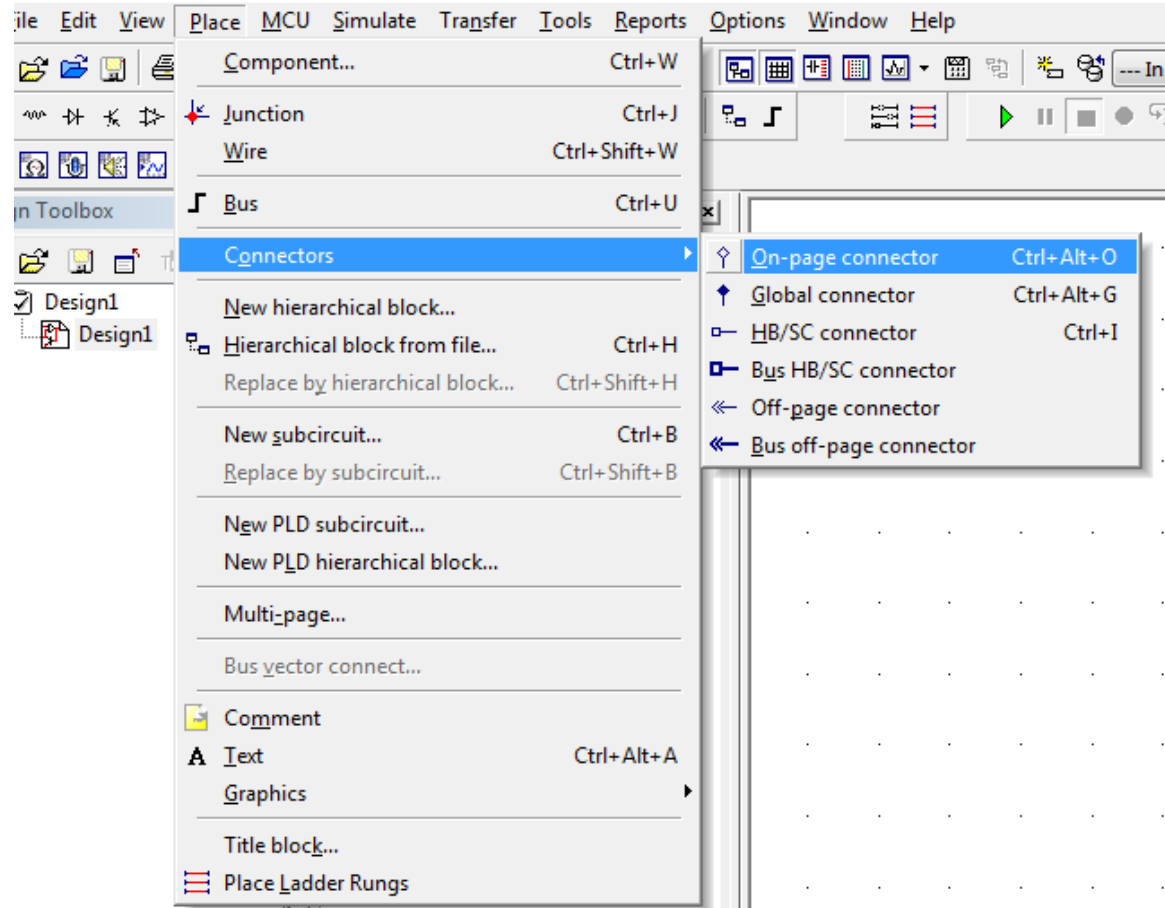
On-page connectors are visible to the sheet



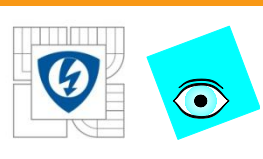
On-page connectors may connect to Global connectors



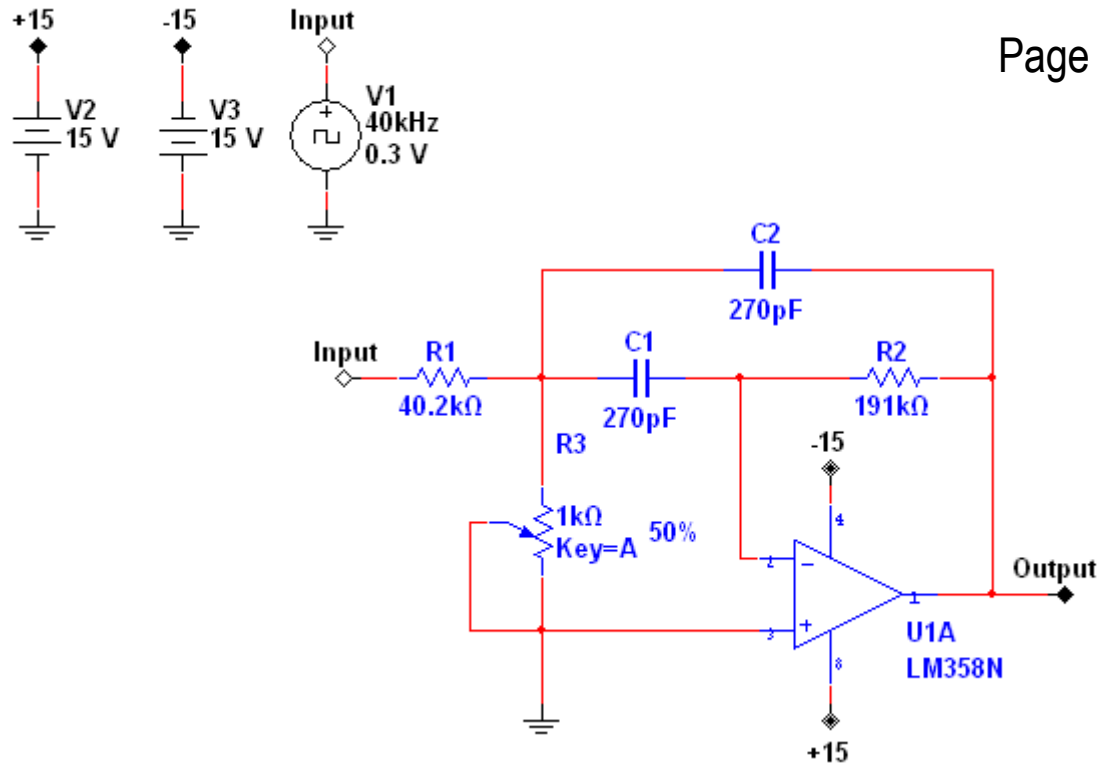
Virtual Wiring



Place/connectors/..



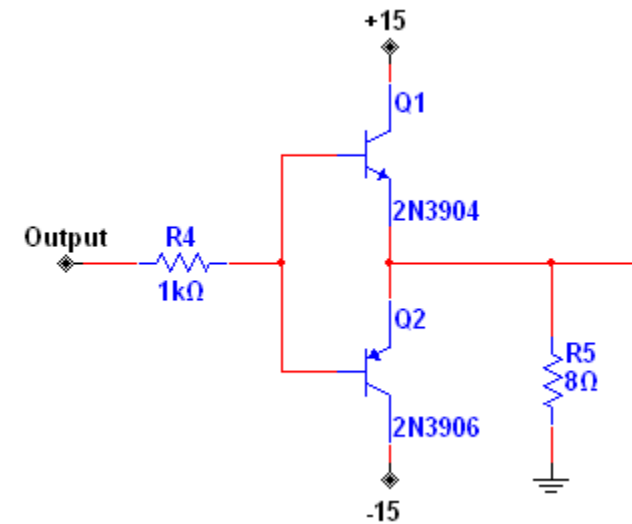
Virtual Wiring



My Design

Page X

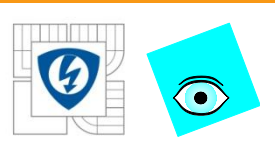
Page Y



13. 4. 2012

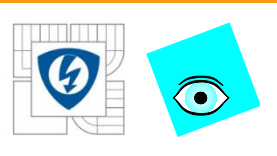
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Analyses in Multisim

- Multisim provides analyses for examining circuit behavior
- Analyses require a circuit ready for simulation
- Custom expression can be added
- Grapher View helps to take precise measurements



Analyses in Multisim

- The following analyses are available:

DC Operating Point

Distortion Analysis

Transfer Function

AC Analysis

DC Sweep

Worst Case

Single Frequency AC Analysis

Sensitivity

Monte Carlo

Transient Analysis

Parameter Sweep

Trace Width Analysis

Fourier Analysis

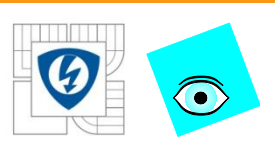
Temperature Sweep

Batched Analysis

Noise Analysis

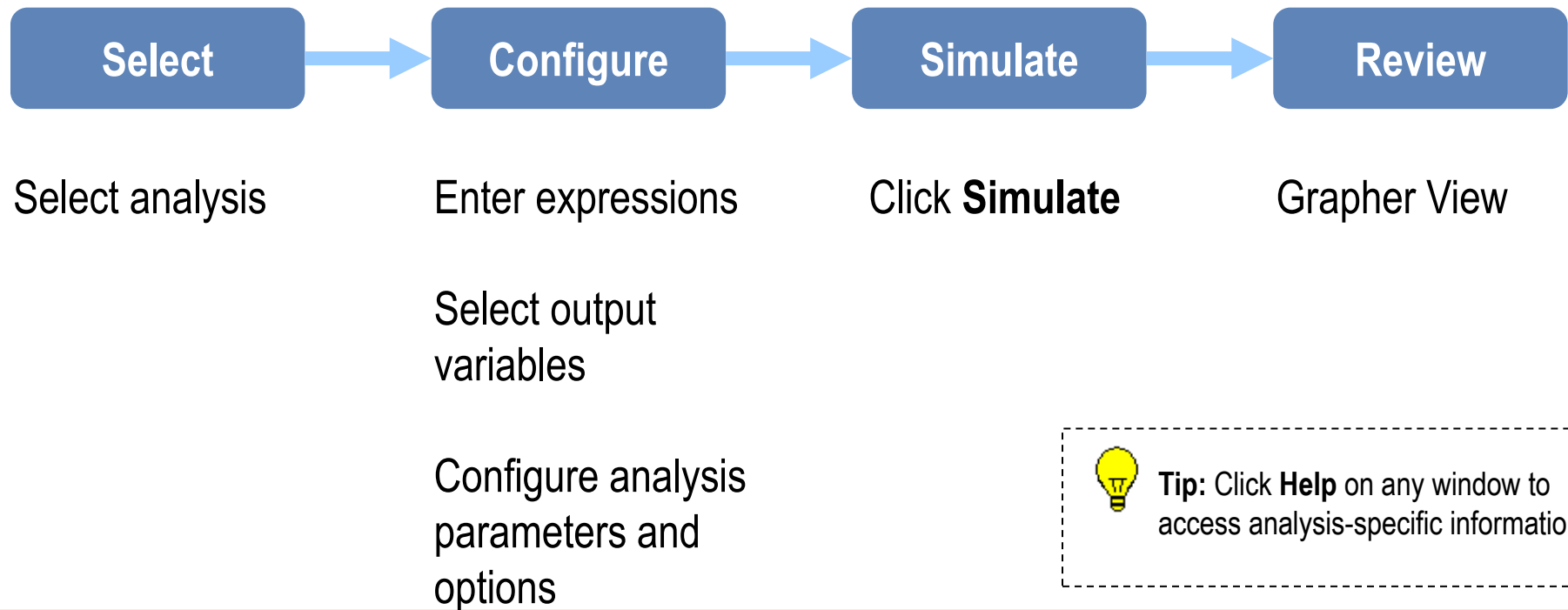
Pole Zero

User Defined Analysis

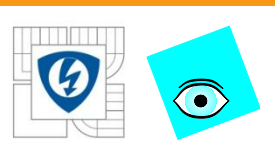


Using Analyses

- **Simulate»Analyses»...**
- Four step process:

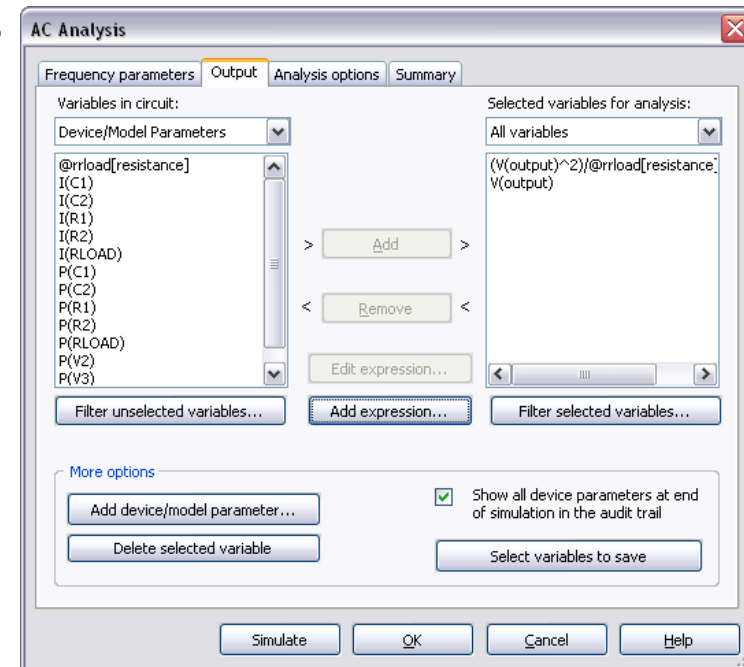


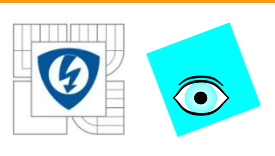
Tip: Click **Help** on any window to access analysis-specific information.



Selecting Output Variables

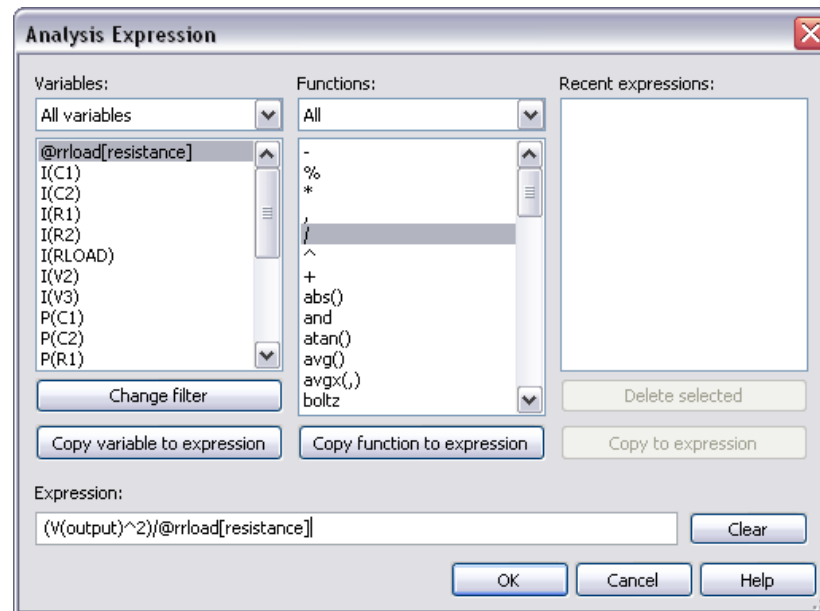
- Choose output variables from the list
- Voltages and currents per node (net) are listed as well as current and power per component
- Add model or device parameters
 - Resistance
 - Capacitance, and so on
- Add expressions

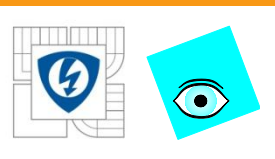




Adding Custom Expressions

- Double-click variable or operand to add it to the expression
- Type expression manually
- Use built-in functions to help create custom analysis outputs

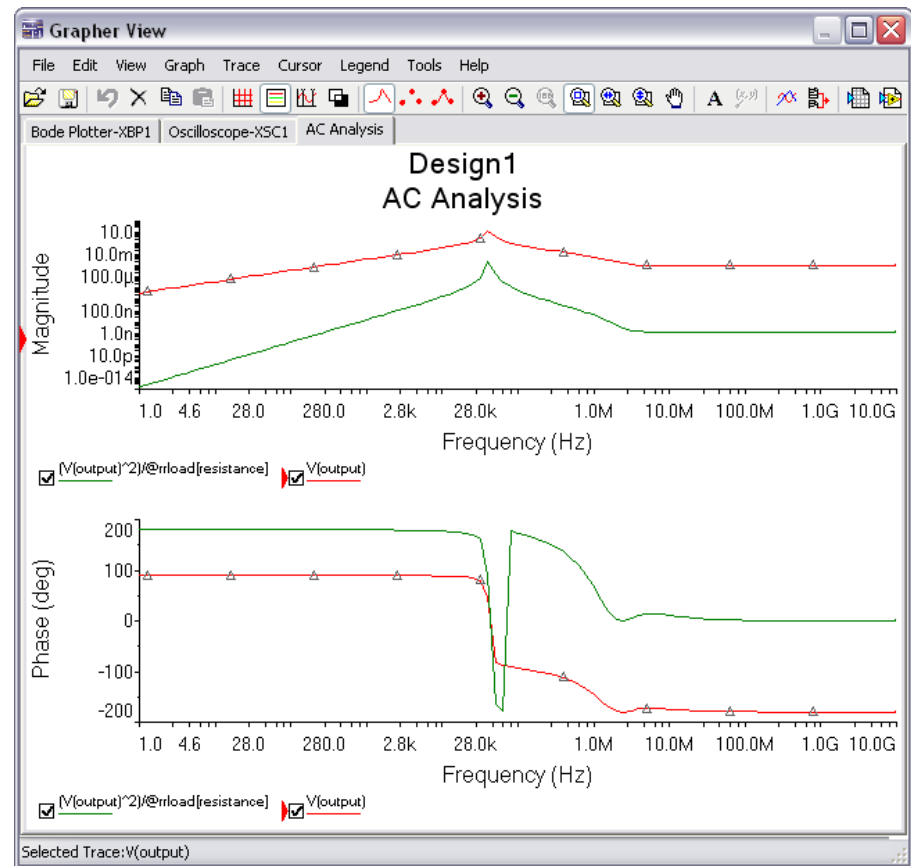


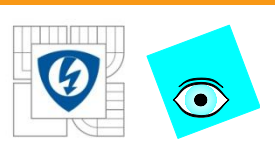


The Grapher



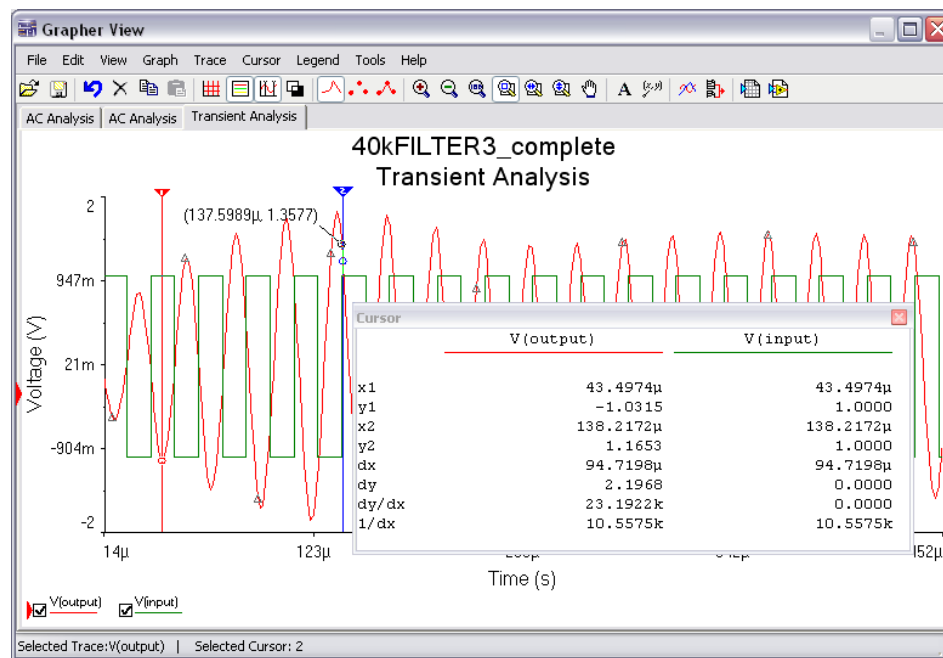
- Displays simulation results from:
 - Virtual Instruments
 - Analyses
- View, adjust, save, print export data
- Precise cursor measurements
- Overlay different results to compare
- Make annotations and place data labels





The Grapher – Cursors

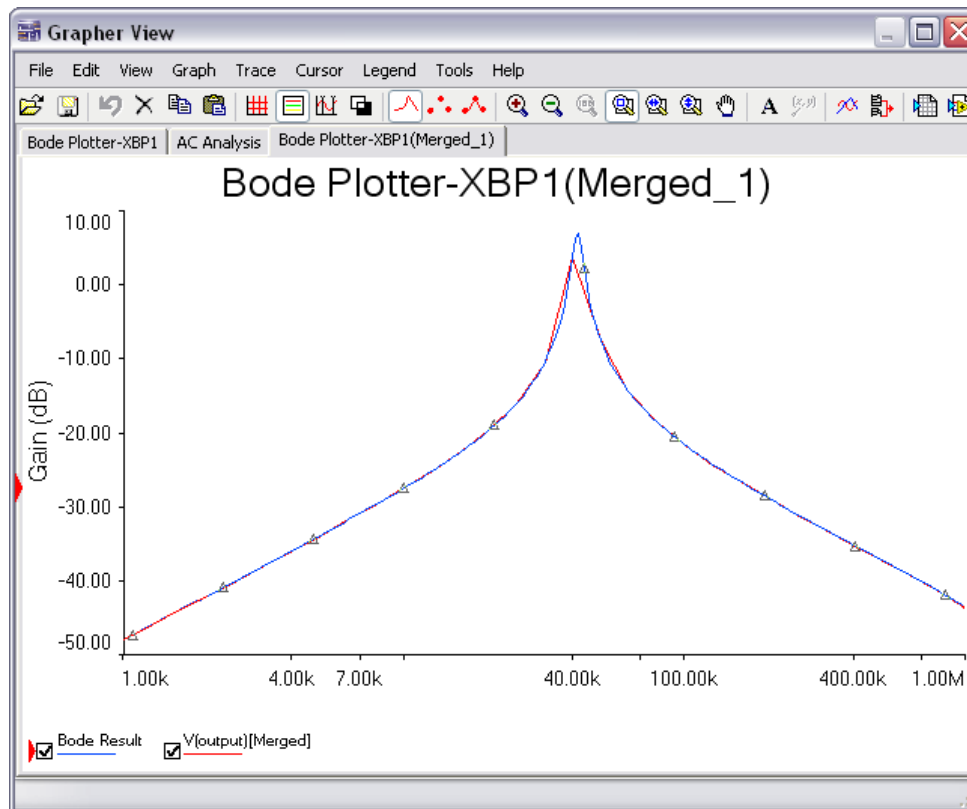
- Take precise measurements with the cursors
- Right-click cursor to access functions for positioning and data labels

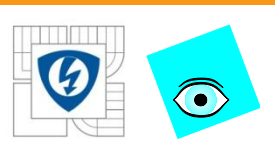




The Grapher – Overlay Traces

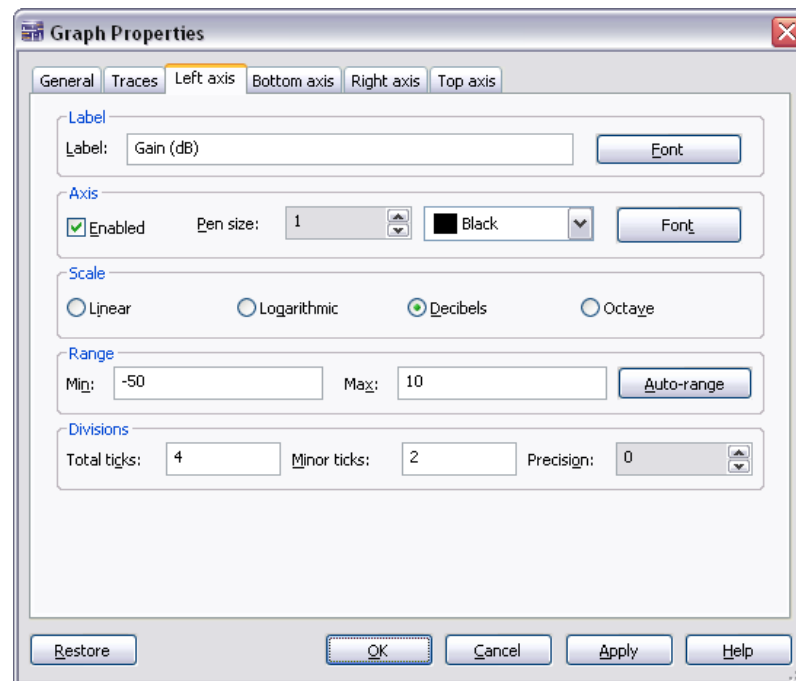
- Compare different graphs

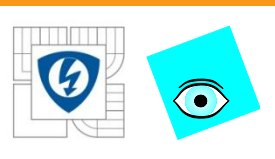




The Grapher – Properties

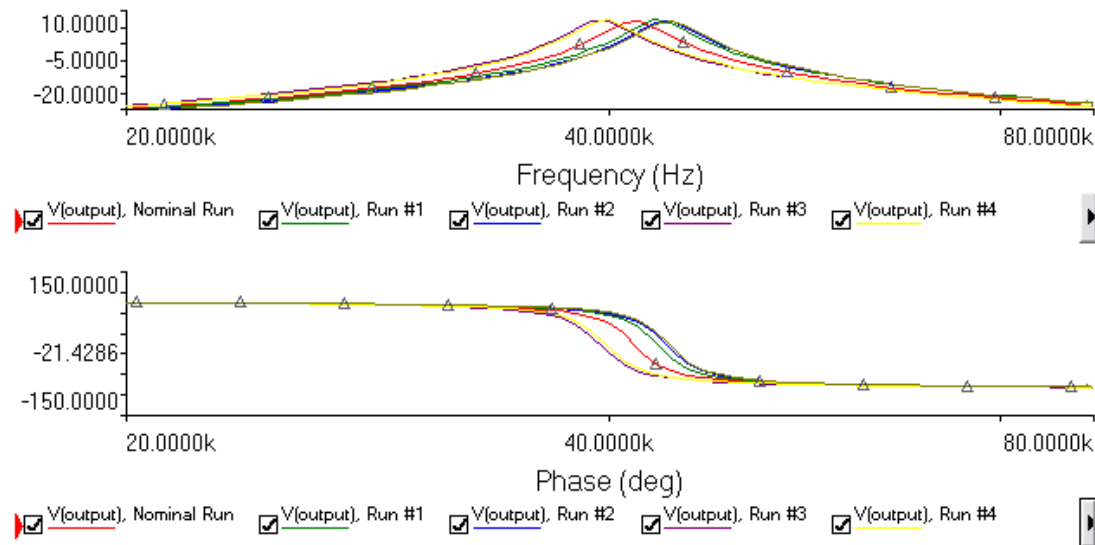
- Set custom properties for pages and graphs
- Modify the appearance of traces and axes





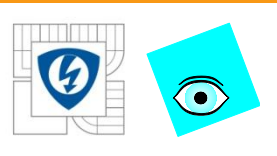
The Grapher – Mixed Displays

- Some analyses output table data instead of plot data



Run Log Descriptions

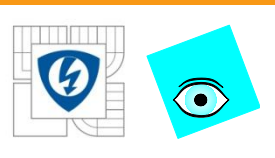
	# of run	time [sec]	output value
1	Nominal Run (Mean Frequency: 2.23926 Standard Deviation Frequency: 0.045)		2.20422 (same as nominal, lower than mean by -0.0350466)
2			
3	Run #1		2.32573 (5.51293% higher than
4			
5	Run #2		2.19695 (0.329613% lower than



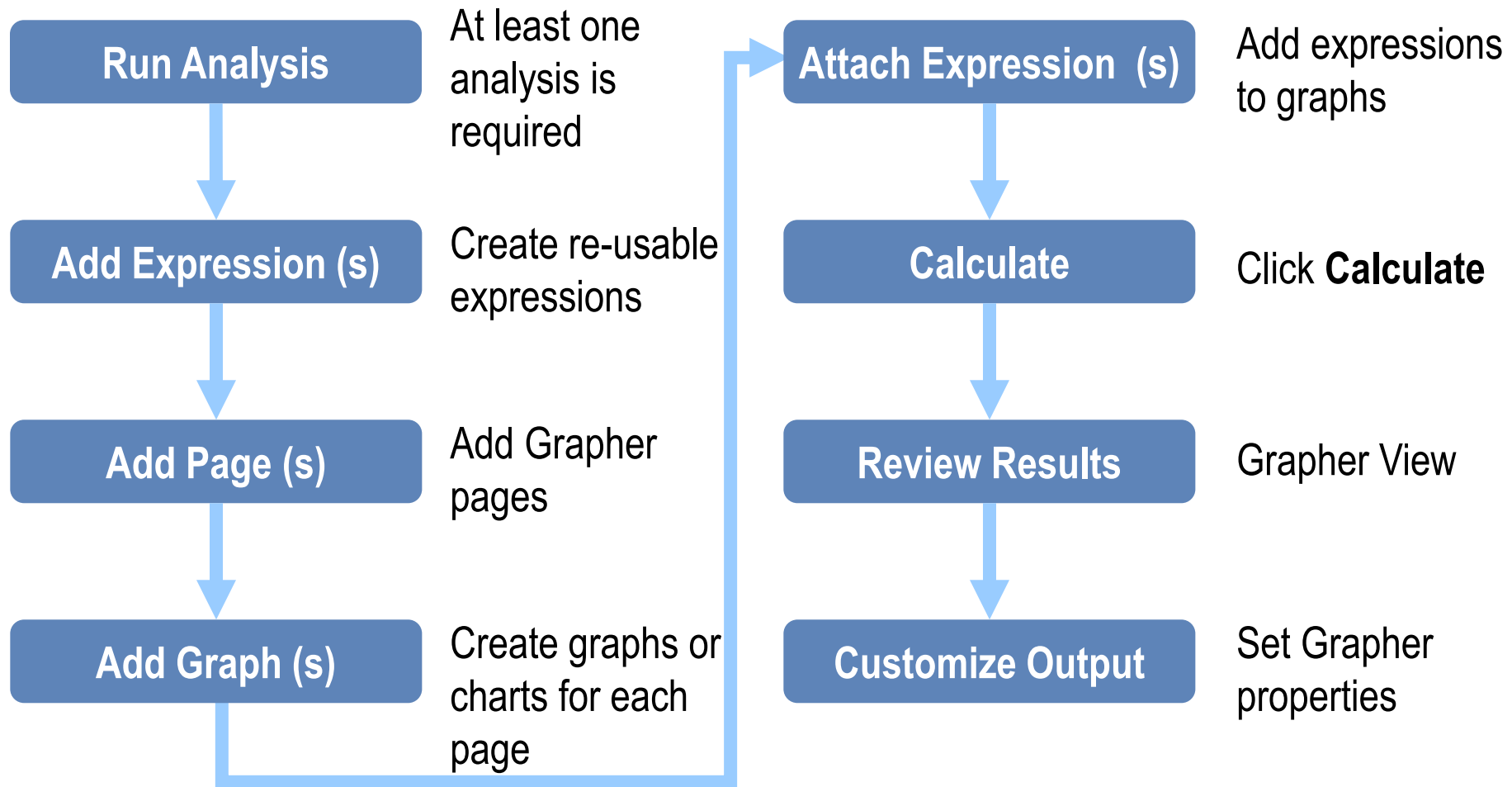
The Postprocessor

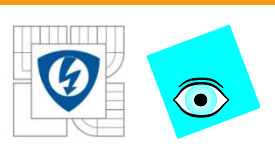


- Use the Postprocessor to:
 - Mathematically manipulate analyses results
 - Plot results in a graph or chart
 - Customize results output
- At least one analysis run is required
- **Simulate»Postprocessor**
- Examples:
 - Add voltages
 - Calculate power from voltage and current



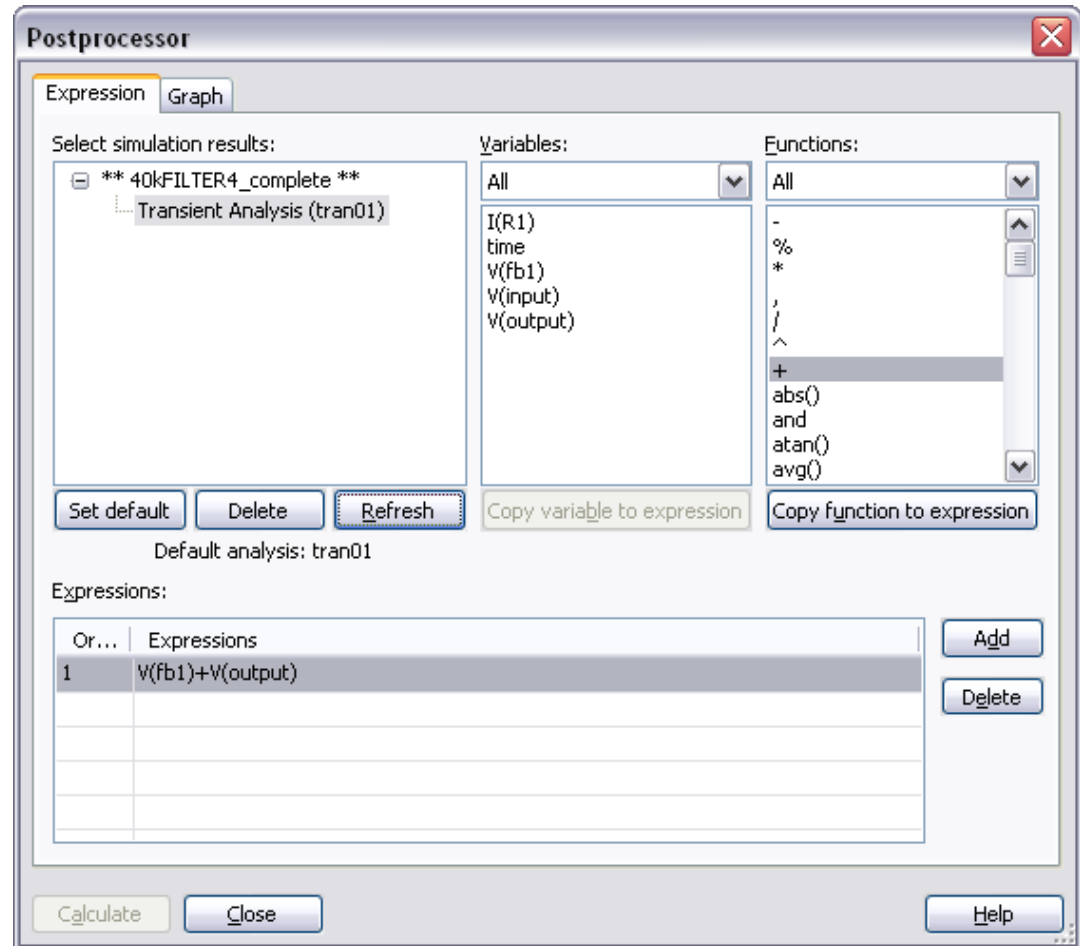
Using the Postprocessor

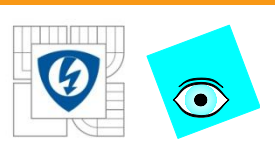




Using the Postprocessor – Expression Tab

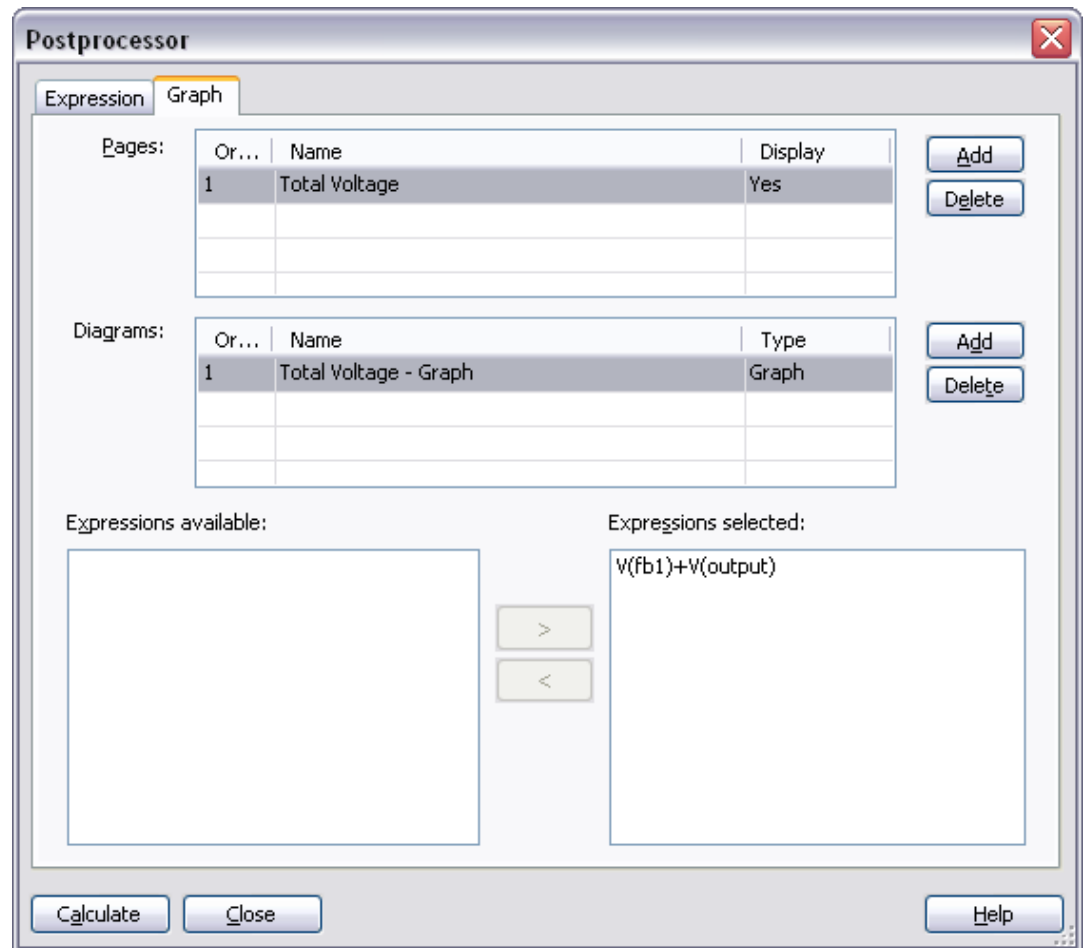
- Select from available results
- Select from available variables
- Build expressions

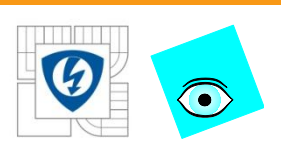




Using the Postprocessor – Graph Tab

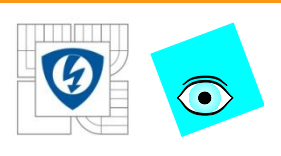
- Add Pages
- Add Graphs or Charts to Pages
- Assign Expressions
- Click **Calculate**





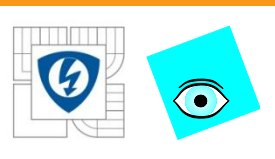
Viewing Results from the Postprocessor

- The Grapher displays Postprocessor results like any other instrument or analysis
- Use the cursors to make precise measurements
- Set the graph properties to fit your results
- Save, print or export results to external applications

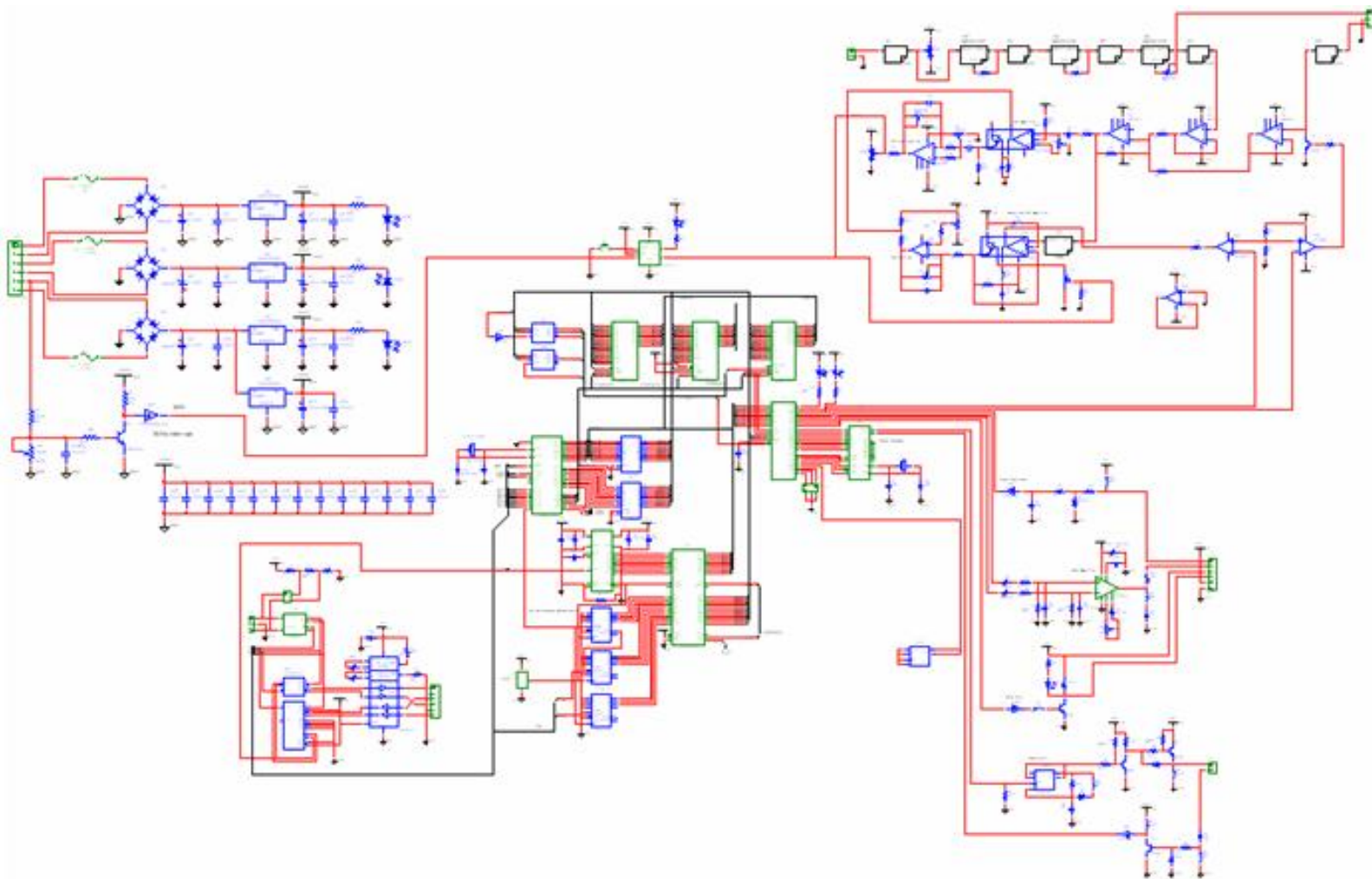


Design Blocks

- Build a library of commonly used circuits
- Reuse circuit models
- Changes propagate
- Cleaner, modularized architecture
- Use the Design Toolbox to browse through the hierarchy
- Three options:
 - Hierarchical Blocks
 - Subcircuits
 - Multi-page



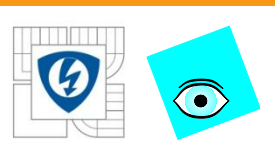
Design Blocks – Before



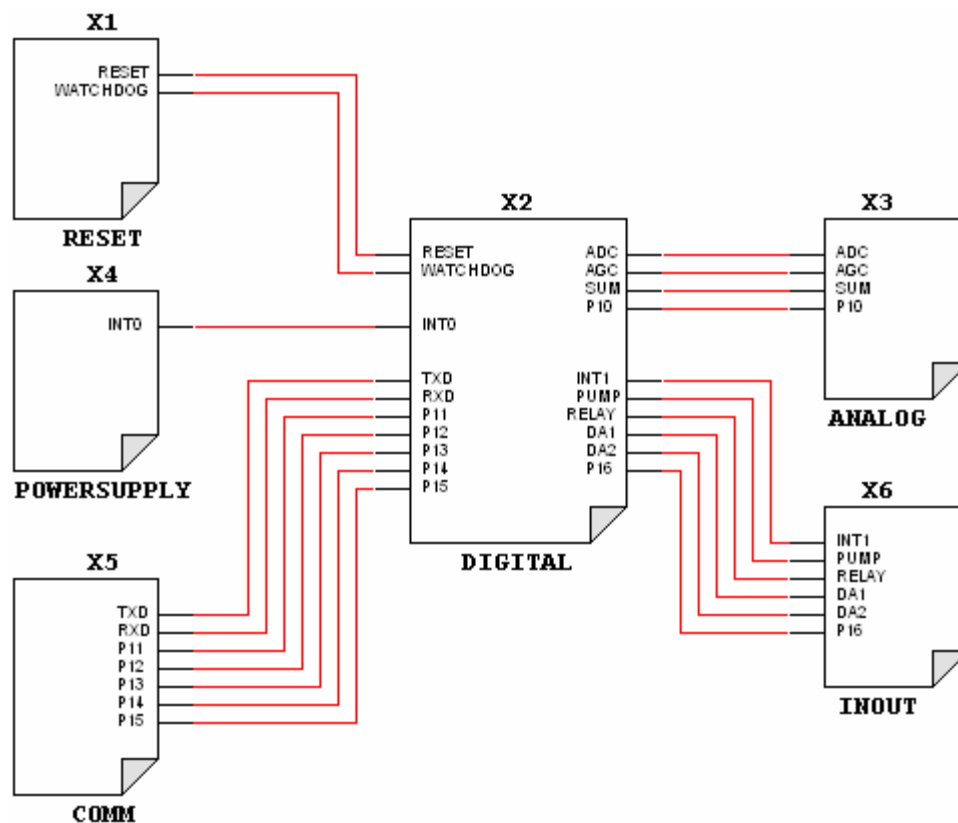
13. 4. 2012

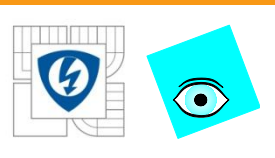
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





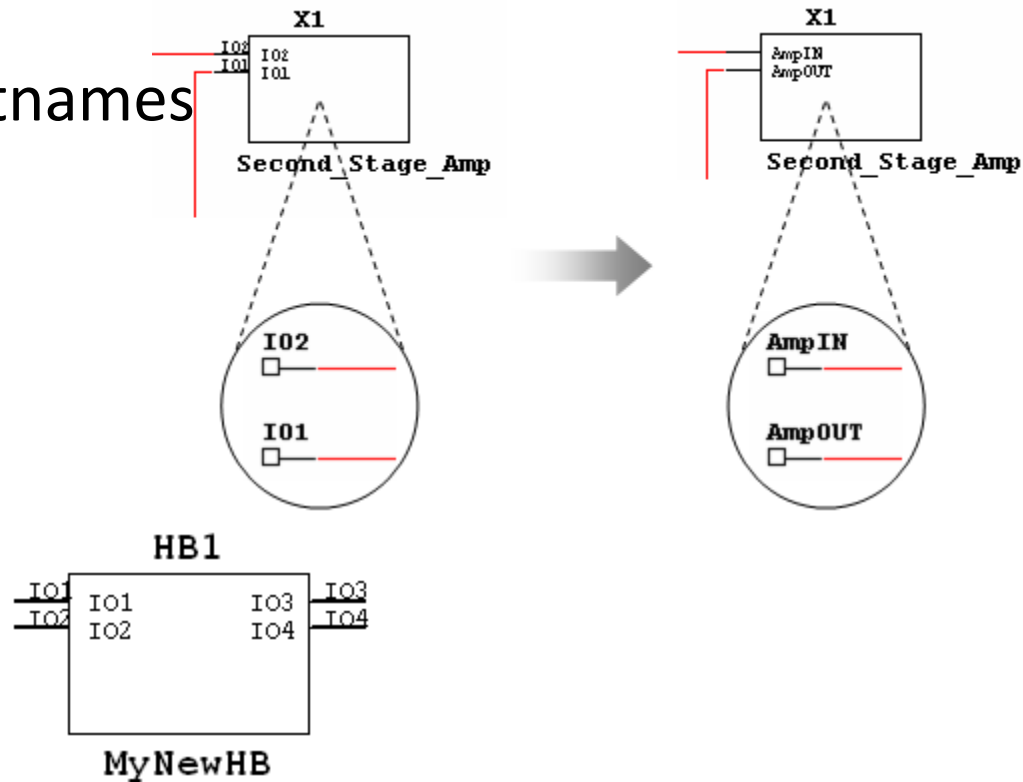
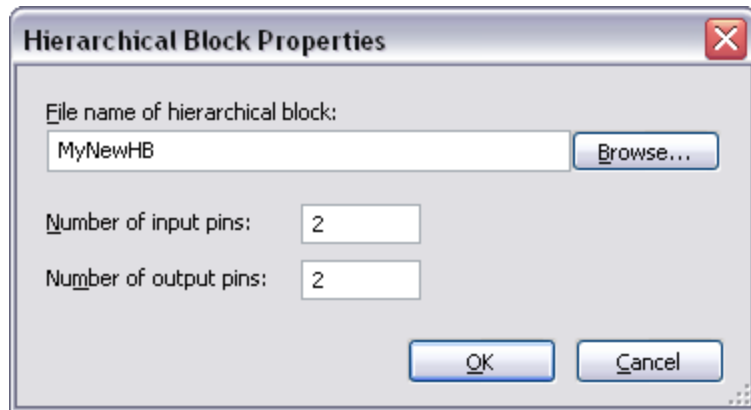
Design Blocks – After

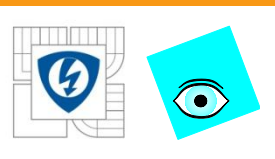




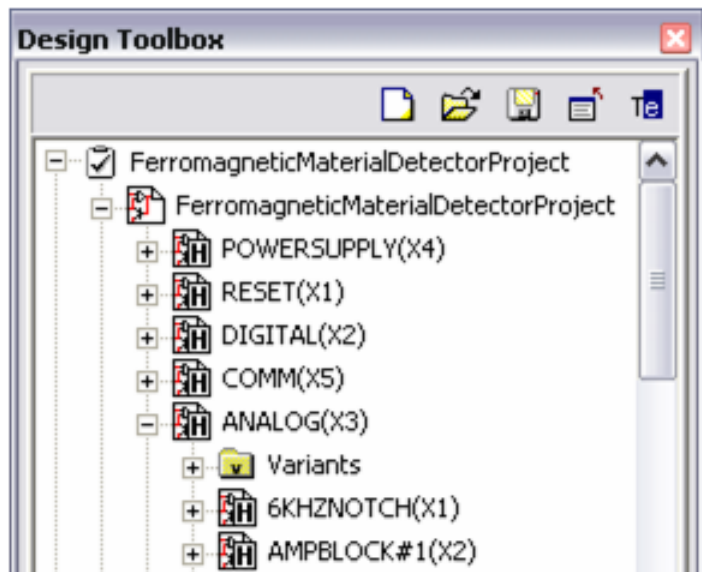
Design Blocks – Connectors

- Interconnect circuits with HB or SC connectors
- Rename connectors
- Connector name = netnames





Nested Circuits



→ Design Name



→ Top Level Circuit Page



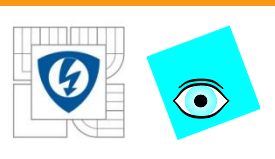
→ Hierarchical Block



→ Subcircuit

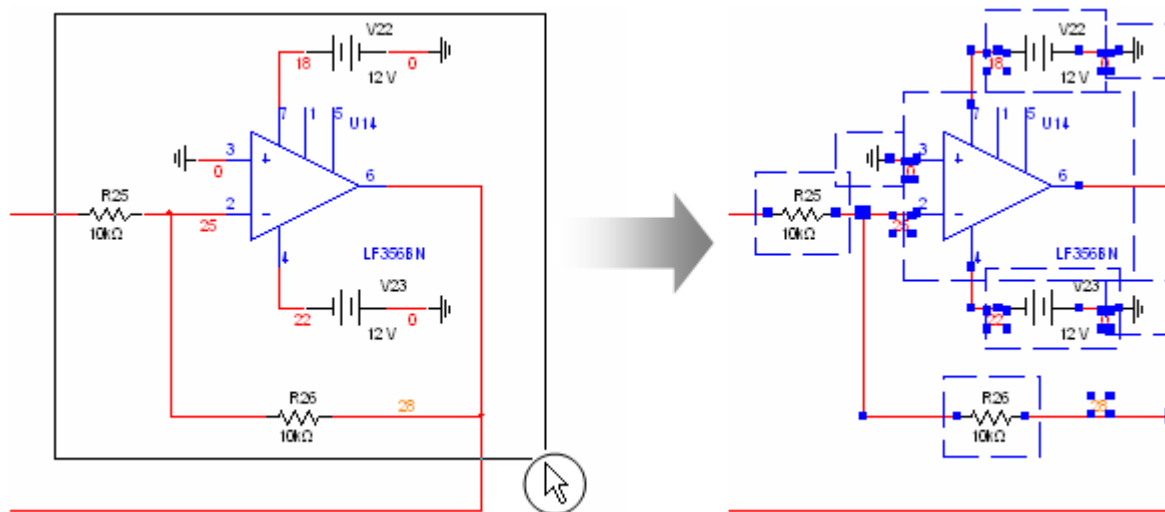
↑
↑
↑
↑
2nd Child Nested Circuit (HB/SC)
1st Child Nested Circuit (HB/SC)
Page Level (Single or Multi-Page design)
Design Level (Main filename)

- Hierarchy tree organization
- Use Design Toolbox



Creating Design Blocks

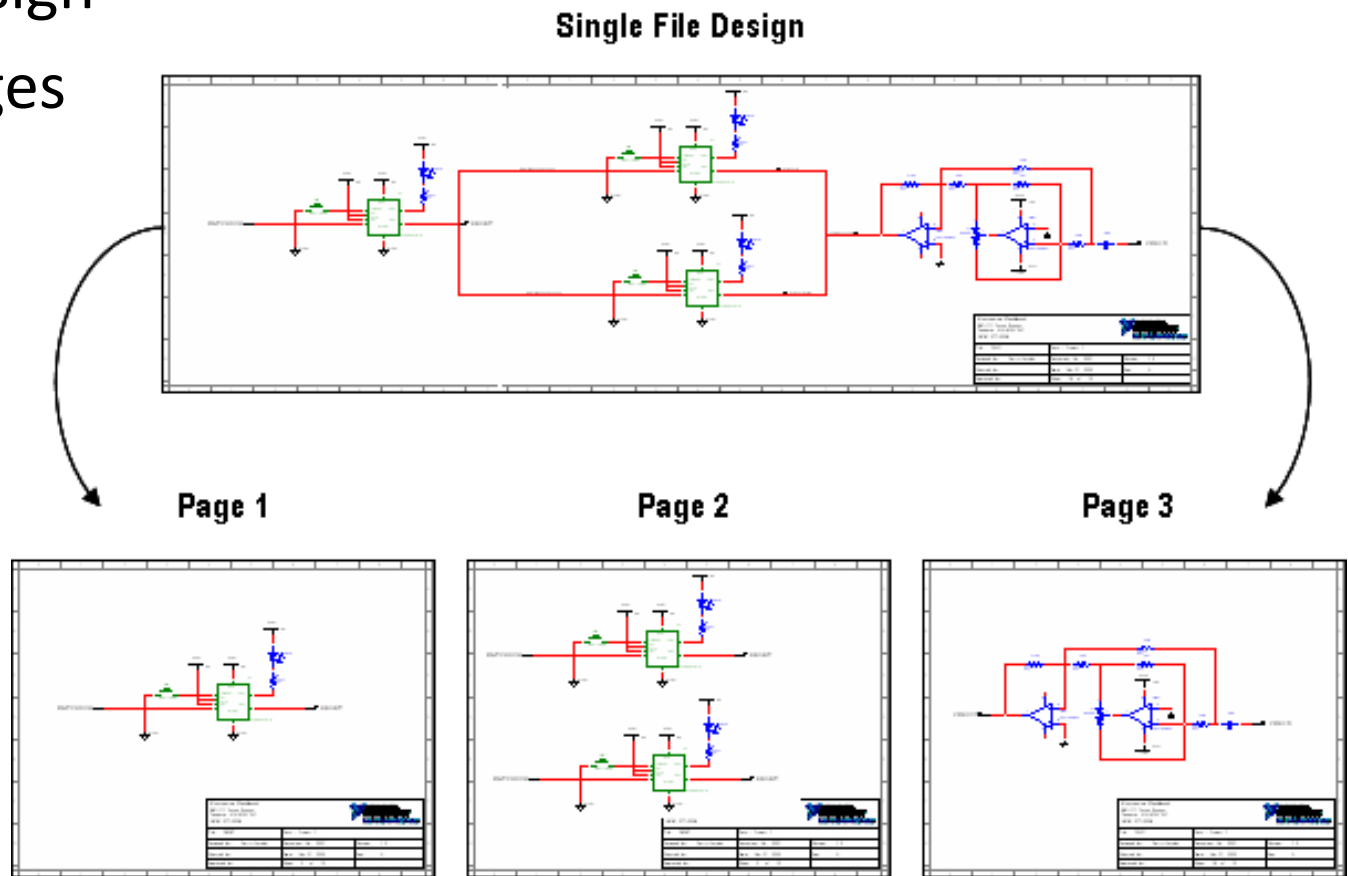
- Multiple options to create or use blocks
 - Place»New Subcircuit (or Hierarchical Block)
 - Place»Hierarchical Block from File
 - Place»Replace by Subcircuit (or Hierarchical Block)

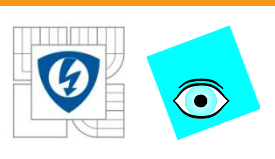




Multi-page Design

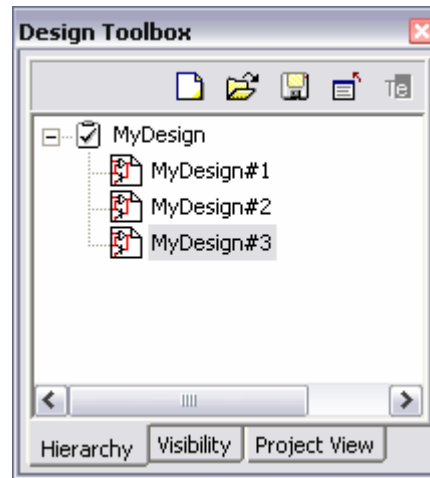
- For flat design
- Split in pages



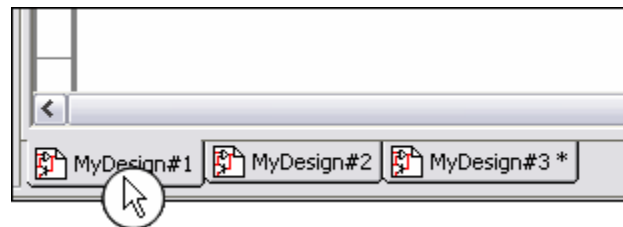


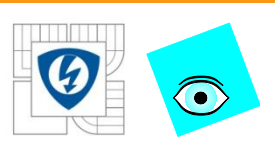
Multi-page Design

- Same hierarchy level as top-level page



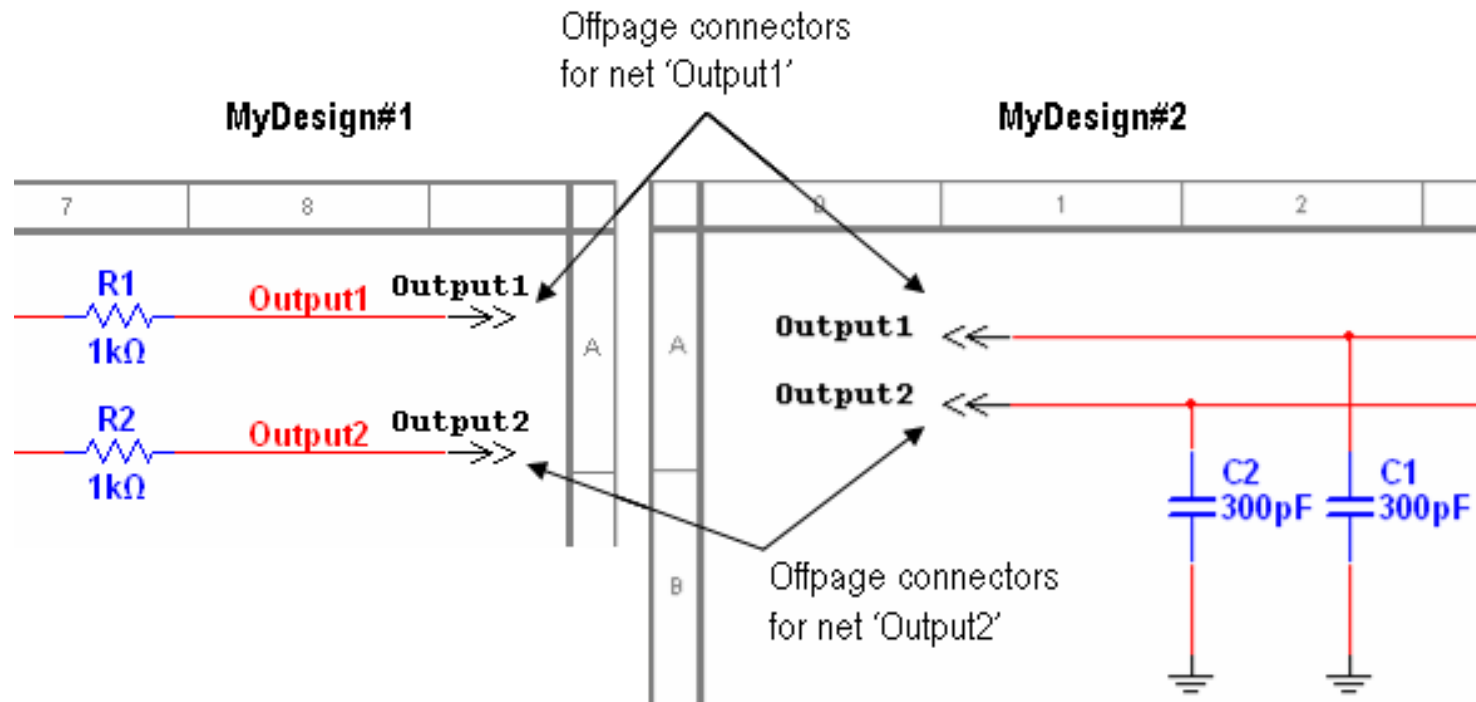
- Workspace tabs per page (reorder in Design Toolbox)

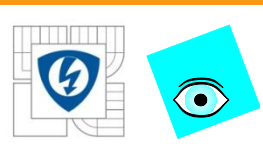




Multi-page Design

- Interconnect pages with Off-page connectors.
- Alternatively, you could use Global with On-page connectors.





Modular Design Summary – Pros & Cons

Multi-page

Pros

- Good for flat designs
- Every page saved in the same circuit file
- Organized horizontal view of design

Cons

- Not for reusing blocks in a later project
- Not recommended for non-flat designs
- File size is bigger
- Updating a section requires the complete circuit to be open

Subcircuits (SC)

- Every page saved in the same circuit file
- Symbol is editable
- Easy to visualize functional blocks

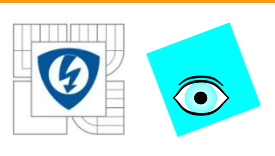
- Not for reusing blocks in a later project
- File size is bigger
- Updating a section requires the complete circuit to be open

Hierarchical Blocks (HB)

- Best option to reuse circuit blocks
- Symbol is editable
- Smaller file size
- Easy to visualize functional blocks
- Updating the HB updates all designs where it is used

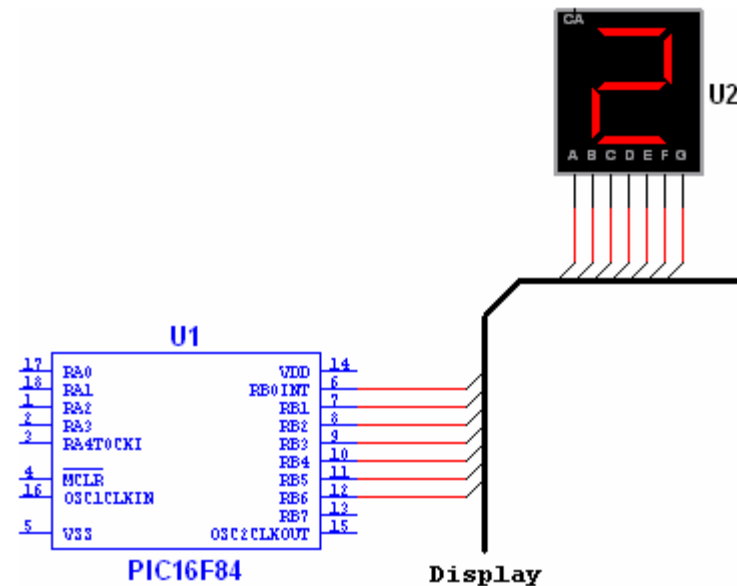
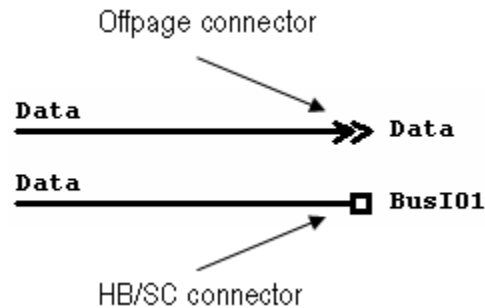
- HBs need to accompany the main design file every time you move it

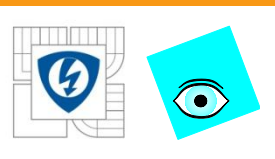
Recommended



Buses

- Buses simplify wiring
- Carry multiple nets
- Used within:
 - a page
 - across pages
 - across design blocks

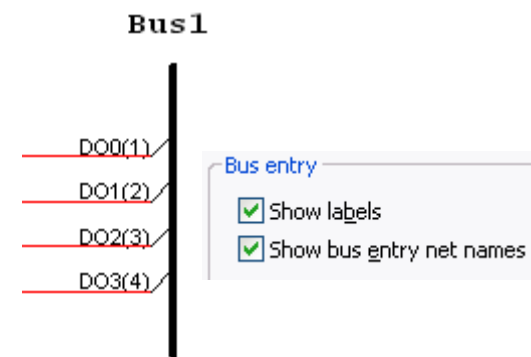
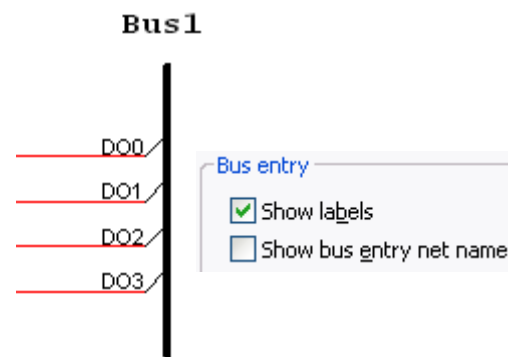
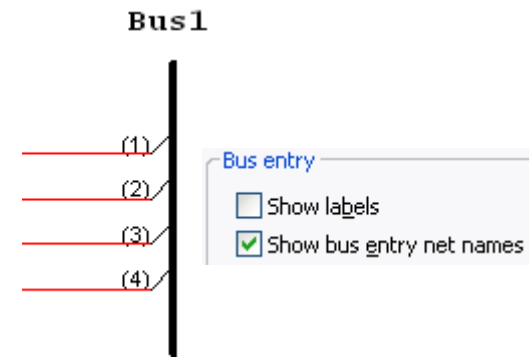
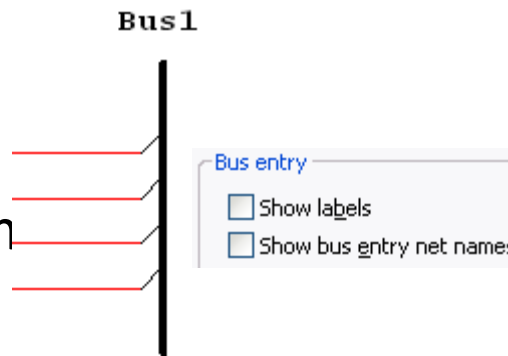


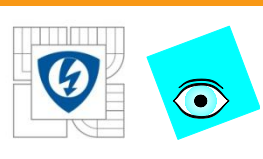


Bus Wiring Modes

- Set mode in **Options»Sheet Properties»Circuit** tab
- Bus wiring modes:

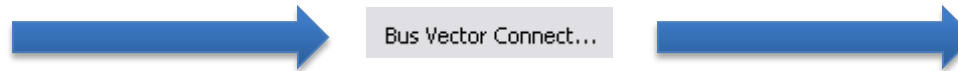
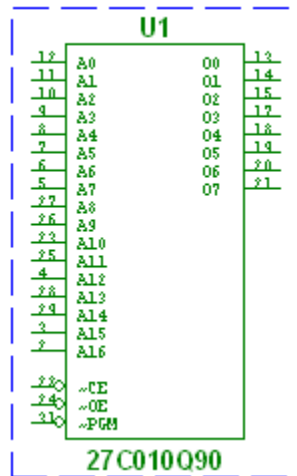
- no labels,
- net names,
- busline nam





Bus Vector Connect

Data



Bus Vector Connect

Select which component pins to connect to which bus lines or nets

Component

Name:

Pins:

03
04
05
06
07

Up
Down

Bus

Name:

Bus lines:

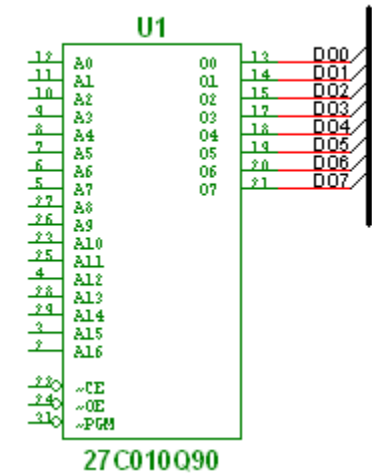
DO0 (<Unconnected>)
DO1 (<Unconnected>)
DO2 (<Unconnected>)
DO3 (<Unconnected>)
DO4 (<Unconnected>)

Add bus lines

Auto-assign
Up
Down

OK Cancel Help

Data



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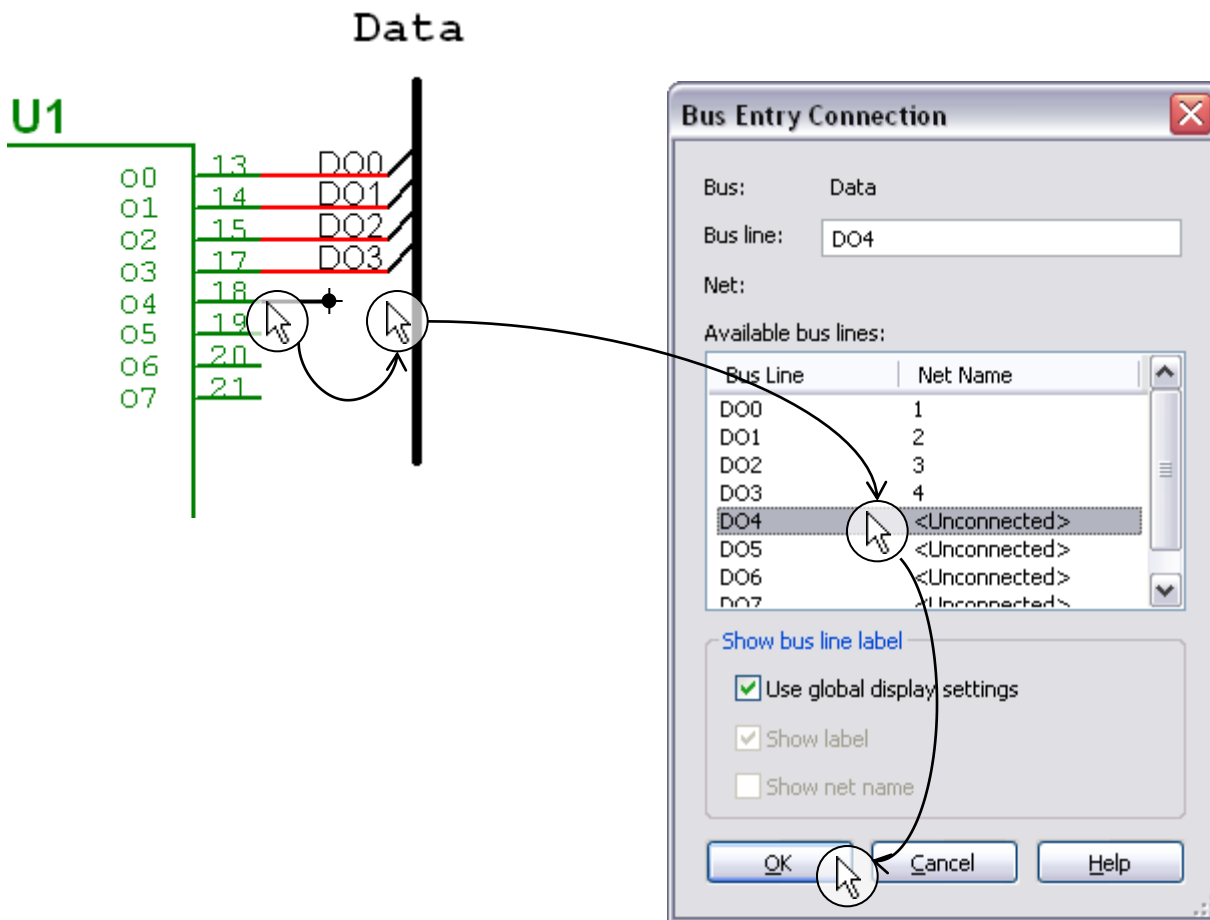
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

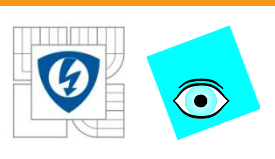


125

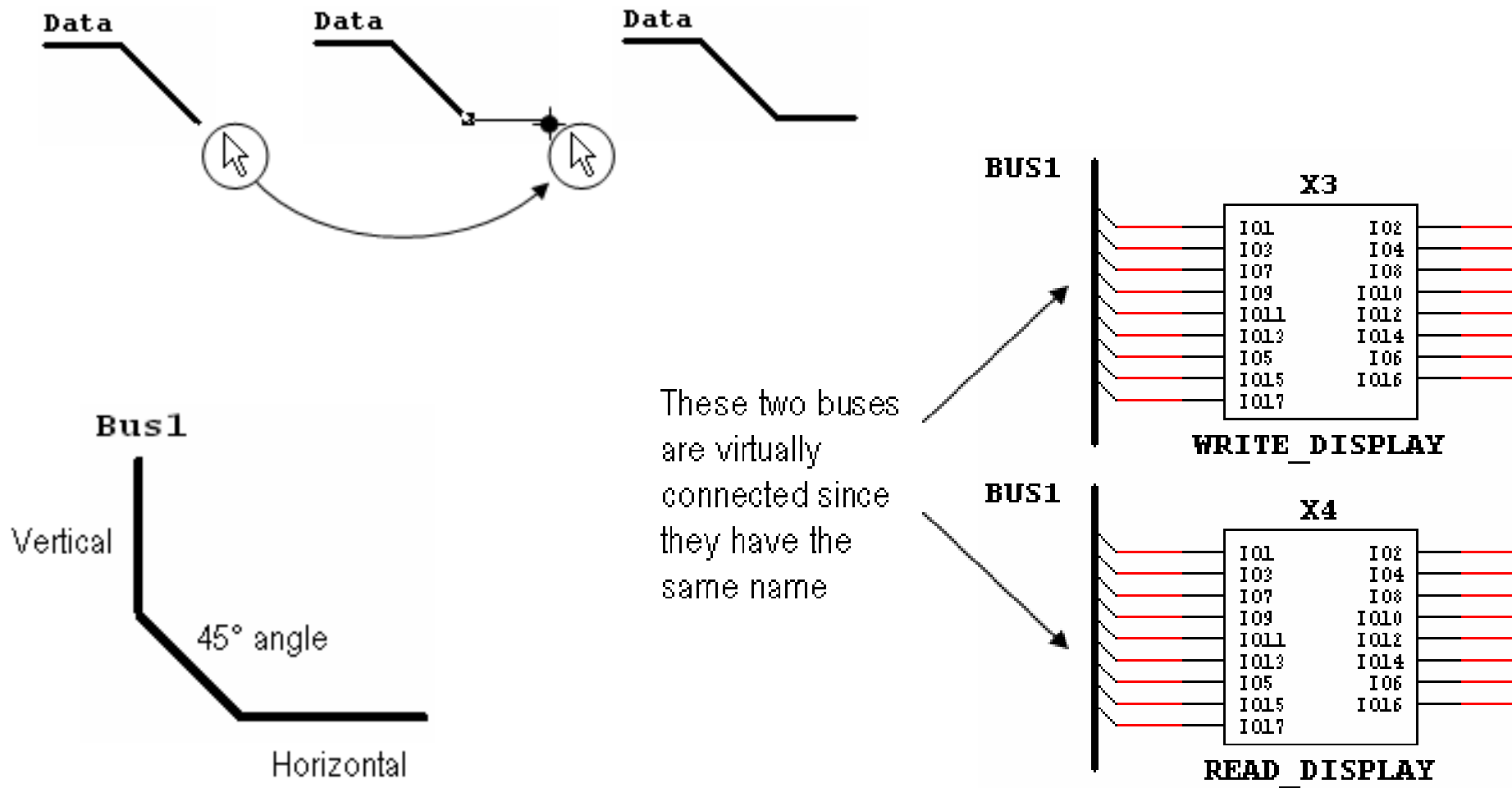


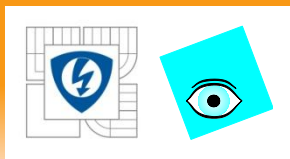
Bus Entry Connect





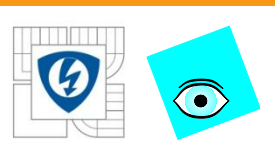
Bus Manipulation





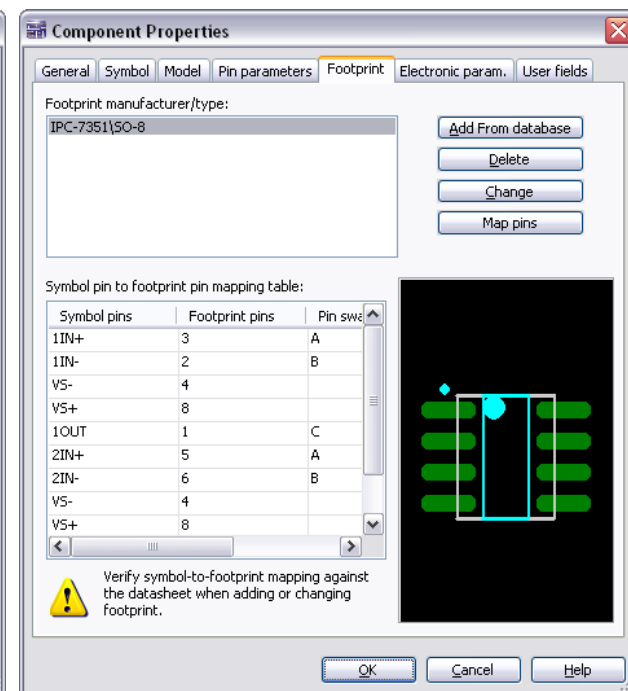
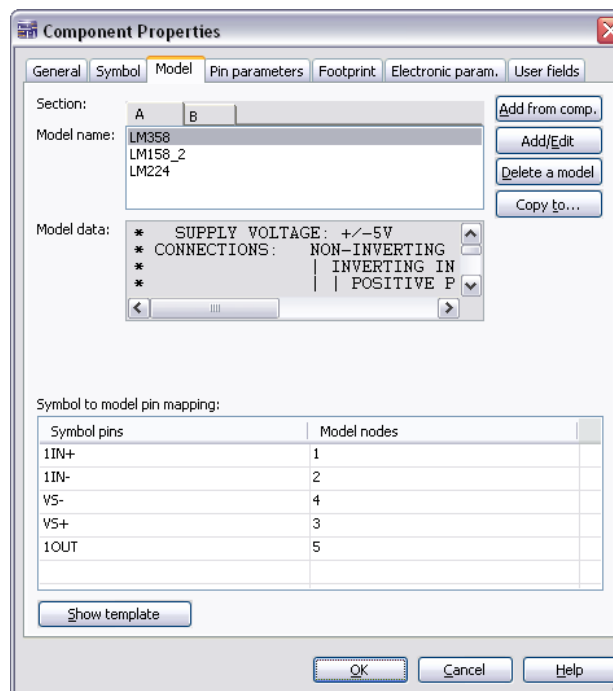
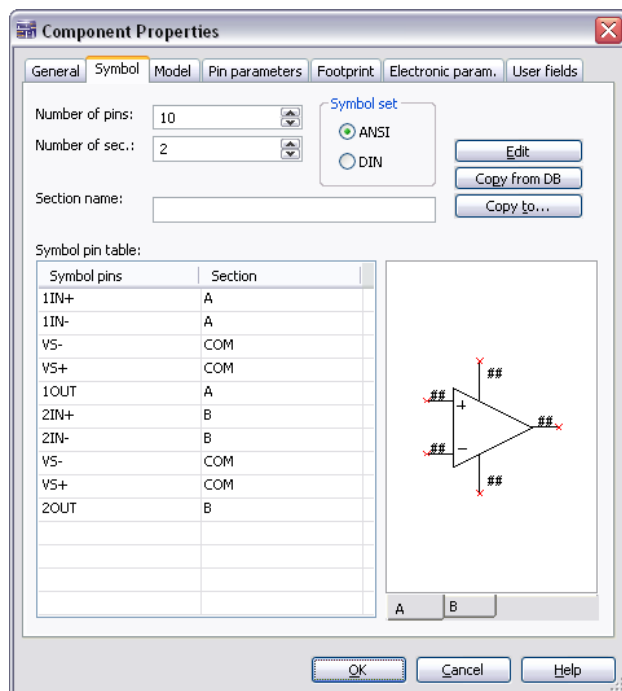
Tools Available to Customize Components

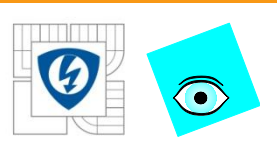
- Component Properties – edit components
- Corporate/User DB – save custom components
- The Component Wizard – create new components
- Model Makers – create new SPICE models
- The Symbol Editor – create new symbols
- Database Manager – manage custom components



Component Properties

- Double-click a component to access the Properties window
- Click **Edit component in DB** to edit the component
- Use the tabs to modify component information or configuration

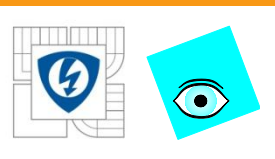




The Component Wizard



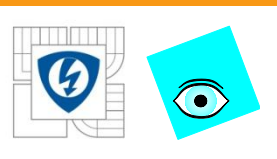
- Step by step assistant guides you in the new component creation
- Store the new component in the User or Corporate database
- Number of steps depend on intended use of component:
 - Simulation and Layout (*model and footprint*)
 - Simulation only (*model*)
 - Layout only (*footprint*)
- **Tools»Component Wizard**



- **Step 1: Enter Component Information**
- Name, author, function
- Component type:
 - *Analog* for most components
 - *Digital* if you have XSPICE
- Select use of component

The screenshot shows the 'Component Wizard - Step 1 of 8' dialog box. It contains the following fields and options:

- Enter component information**
- Component name:** LT1078
- Function:** Micropower Dual Opamp
- Author name:** Your Username
- Use of component:**
 - ☒ Simulation and layout (model and footprint)
 - ☐ Simulation only (model)
 - ☐ Layout only (footprint)
 - ☐ Simulation and PLD export (model and VHDL export)
- Component type:** Analog
- Buttons:** Next >, Cancel, Help



- **Step 2: Enter Footprint Information**
 - Select footprint from database
 - Use custom footprints from Ultiboard
 - Define number of sections
 - Define number of pins per section

Component Wizard - Step 2 of 8

Enter footprint information

Footprint manufacturer: IPC-2221A/2222 [Select a footprint](#)

Footprint type: PDIP-8

☐ Single section component ☒ Multi-section component

Number of sections: 2 Total number of pins: 10

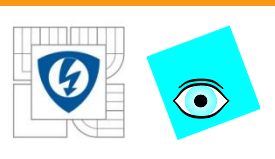
Section details:

A B

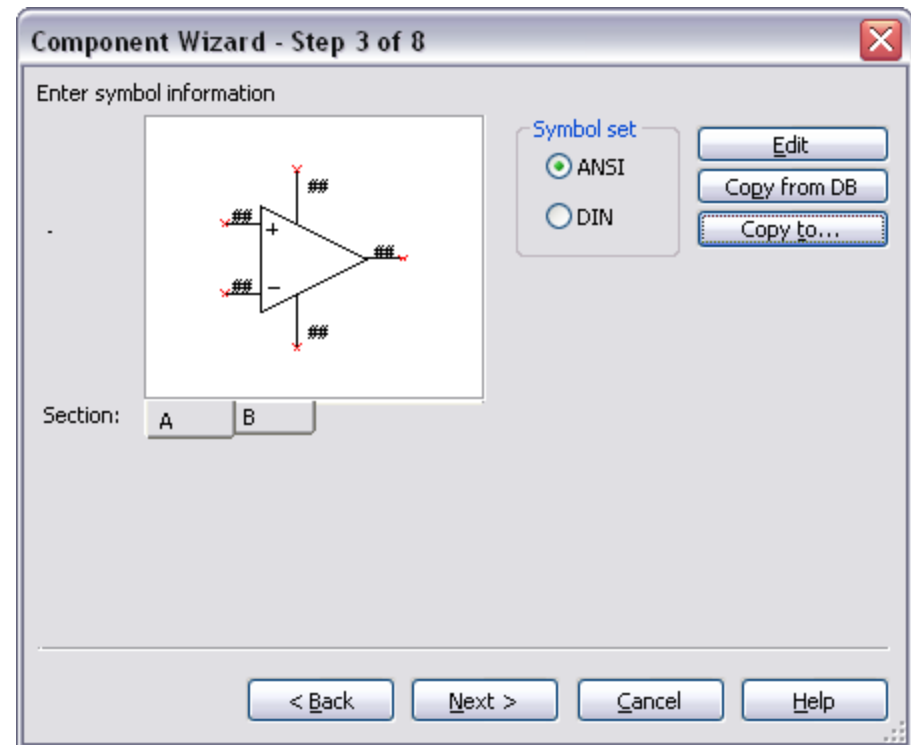
Name: A

Number of pins: 5

< Back Next > Cancel Help



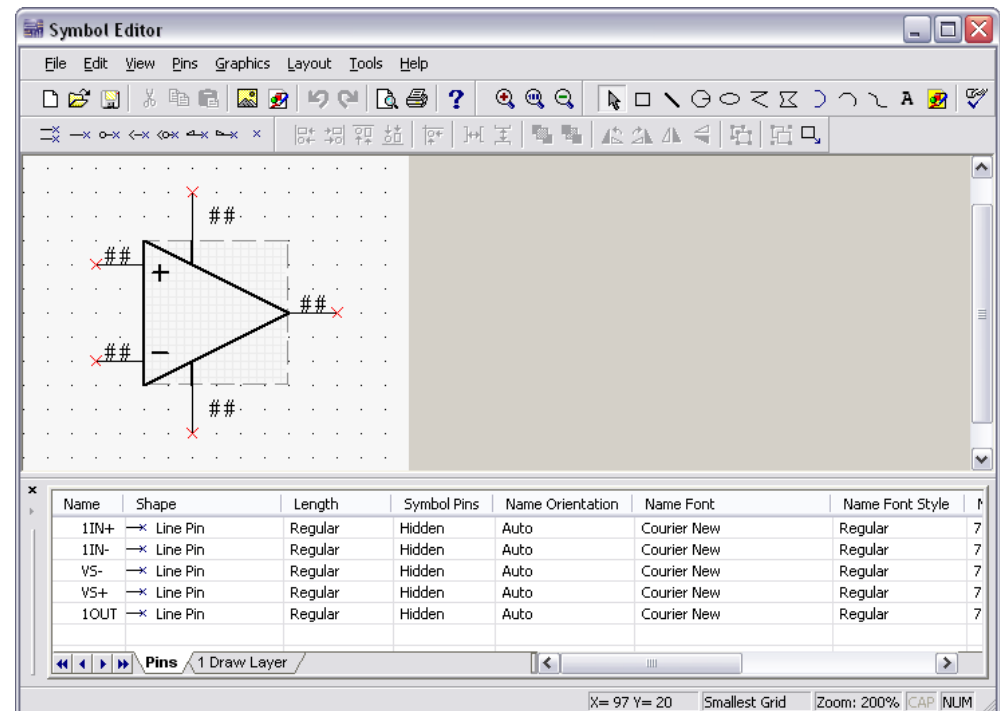
- **Step 3: Enter Symbol Information**
 - Copy symbol from database components
 - Copy symbol to DIN
 - Create symbol per section
 - Click **Edit** to launch **Symbol Editor**

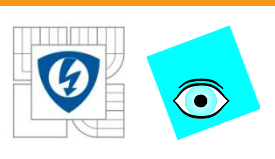




The Symbol Editor

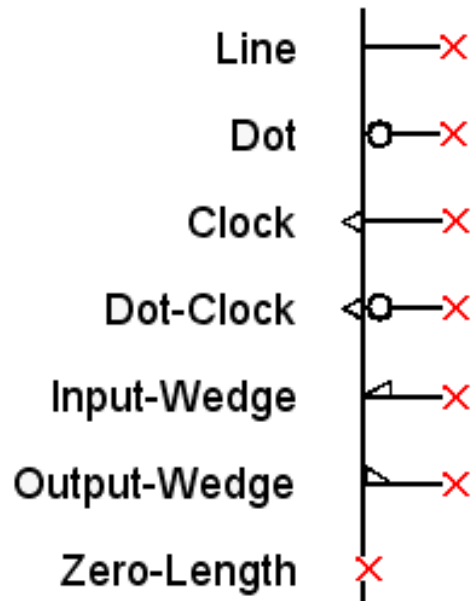
- Specialized graphics editor
- Create / modify symbols
- Save symbol files
- Also access from:
 - **Tools»Symbol Editor**





The Symbol Editor

- Define pin shapes

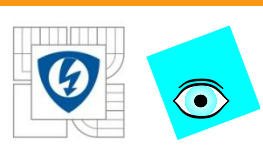


- Define pin names and properties using the Spreadsheet View*

Spreadsheet

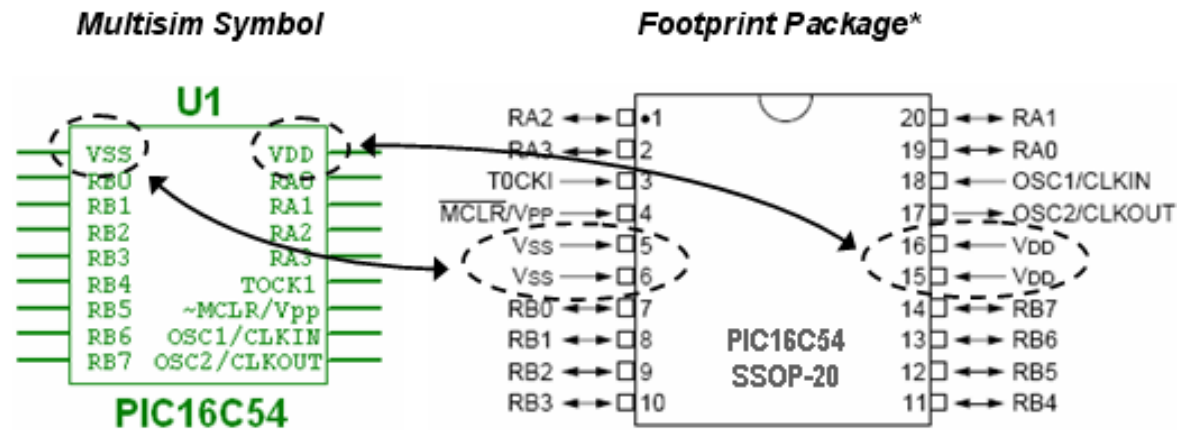
Name	Shape	Length	Symbol Pins	Name Orientation	Name Font
VIN-	Line Pin	Short	Visible	Auto	Courier New
VCC+	Line Pin	Short	Visible	Auto	Courier New
VCC-	Line Pin	Short	Visible	Auto	Courier New
REF	Line Pin	Short	Visible	Auto	Courier New
SHDN	Line Pin	Short	Visible	Auto	Courier New
G0	Line Pin	Short	Visible	Auto	Courier New
G1	Line Pin	Short	Visible	Auto	Courier New
G2	Line Pin	Short	Visible	Auto	Courier New

Pins 1 Draw Layer



The Symbol Editor – Repeated Pins

- **Method 1:** One single pin representing multiple pins

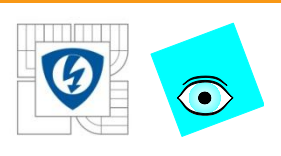


* Microchip® PIC16C54 Datasheet

Symbol Pin to Footprint Pin Mapping Table:

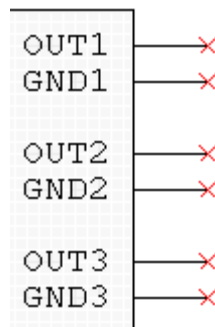
Symbol Pins	Footprint Pins	Pin Swa
VSS	5,6	
RB0	7	
RB1	8	
RB2	9	
RB3	10	
RB4	11	
RB5	12	
RB6	13	
RB7	14	
VDD	15,16	
RA0	19	

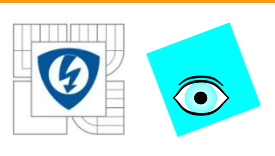
Duplicated footprint pins mapped to one single symbol pin



The Symbol Editor – Repeated Pins

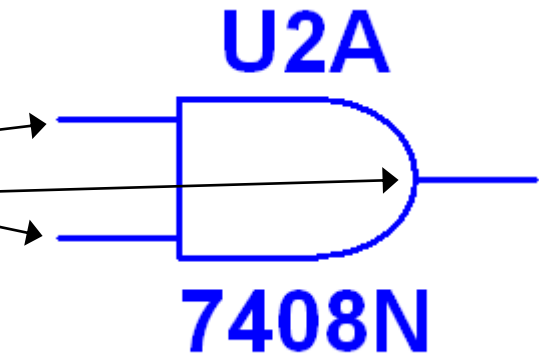
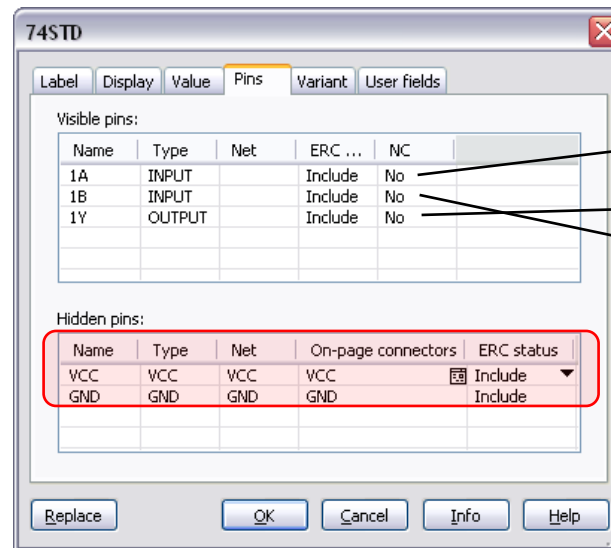
- **Method 2:** One pin with an appended suffix

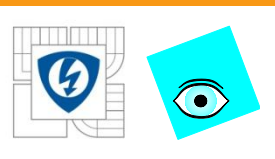




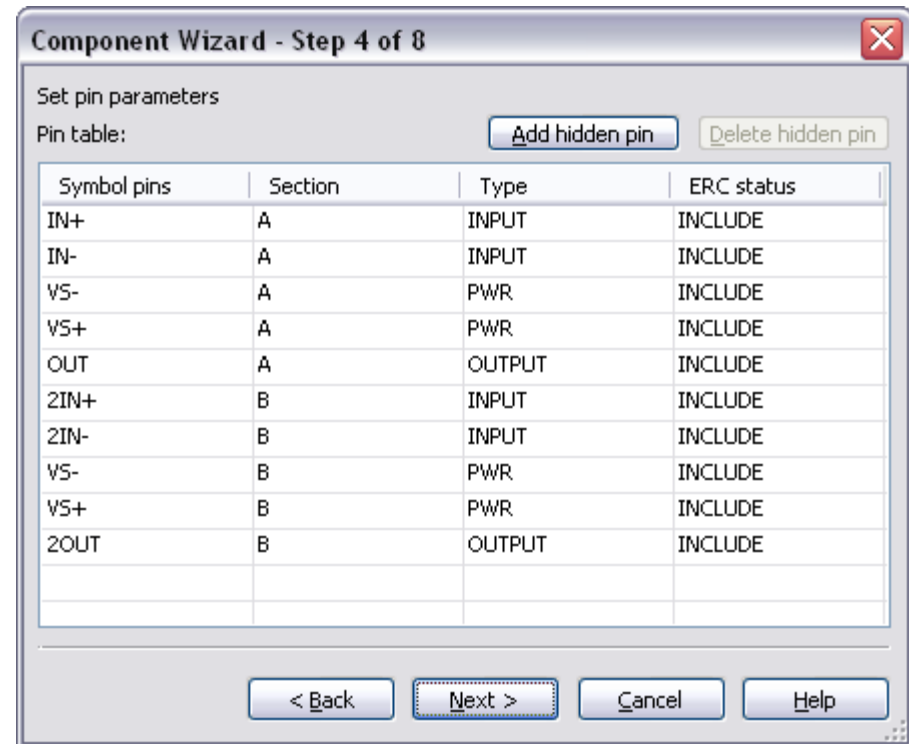
The Symbol Editor – One Shared Pin

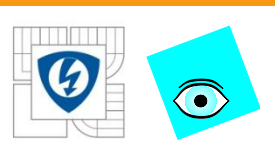
- If a component shares one single pin across multiple sections, such as a GND connection:
 - Create a duplicate pin per section
 - In **Step 5** assign the same footprint pin to every instance of that pin in each symbol
- The other option is to add that pin as a *hidden pin*, which is part of the model and/or footprint but does not show in the schematic.





- **Step 4: Set Pin Parameters**
- Set sections:
 - A, COM, Power, ...
- Set pin types for ERC
- Set ERC status
- Add hidden pins (not in the symbol but needed for model and/or footprint)

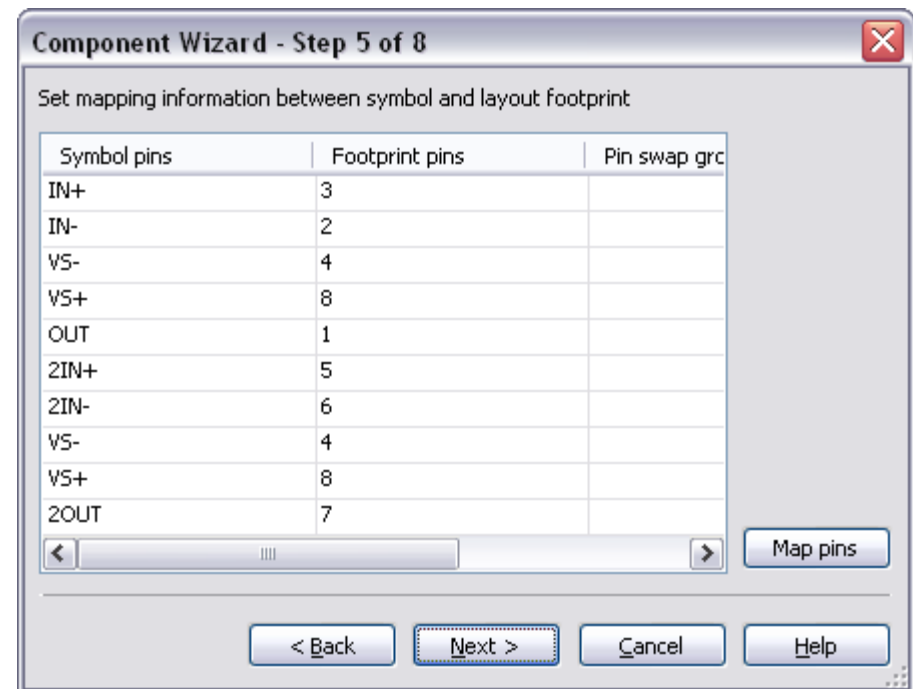


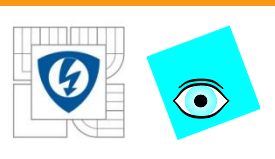


- **Step 5: Set Mapping Information Between Symbol and Layout Footprint**
 - Multiple footprint pins can be mapped to a single symbol
 - Set Pin and Gate Swap Group Information



Caution: The accuracy of this mapping will impact the PCB layout design.



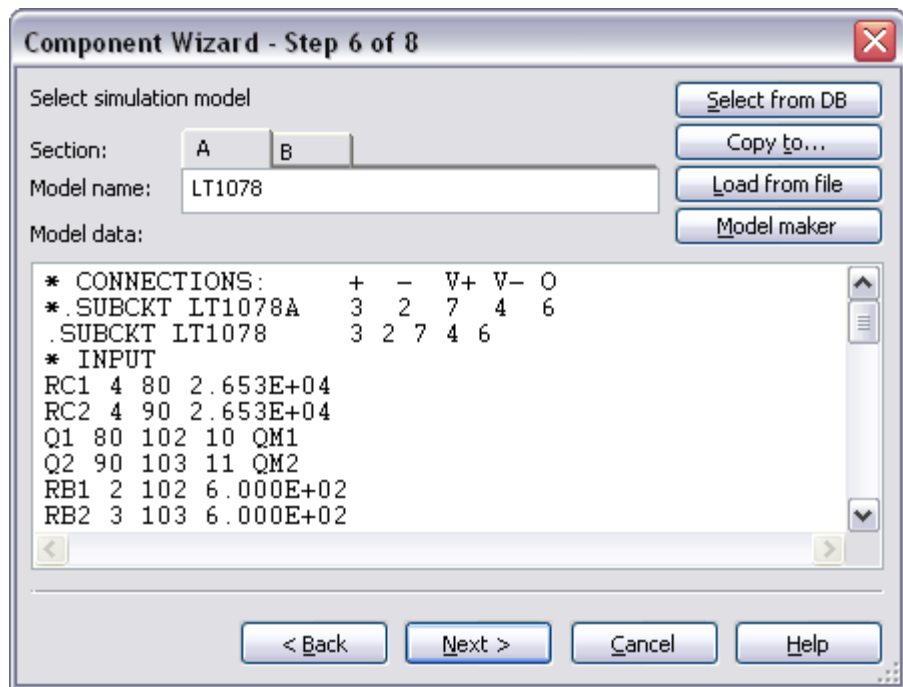


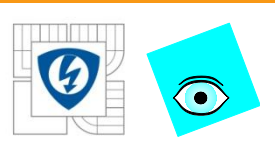
- **Step 6: Select Simulation Model**

- Define model per section
- Copy model from database
- Load model from file
- Use the Model Maker



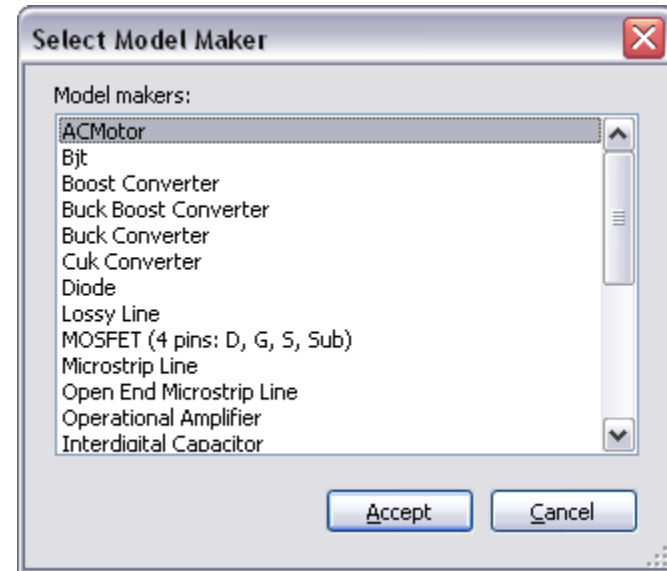
Note: The quality and sophistication of a SPICE model directly impacts the ability to simulate that component correctly and accurately.



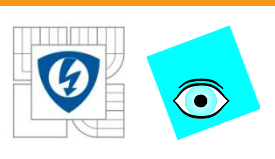


Model Maker

- Automatically generate simulation models
- Use datasheet parameters
- Preset values provided



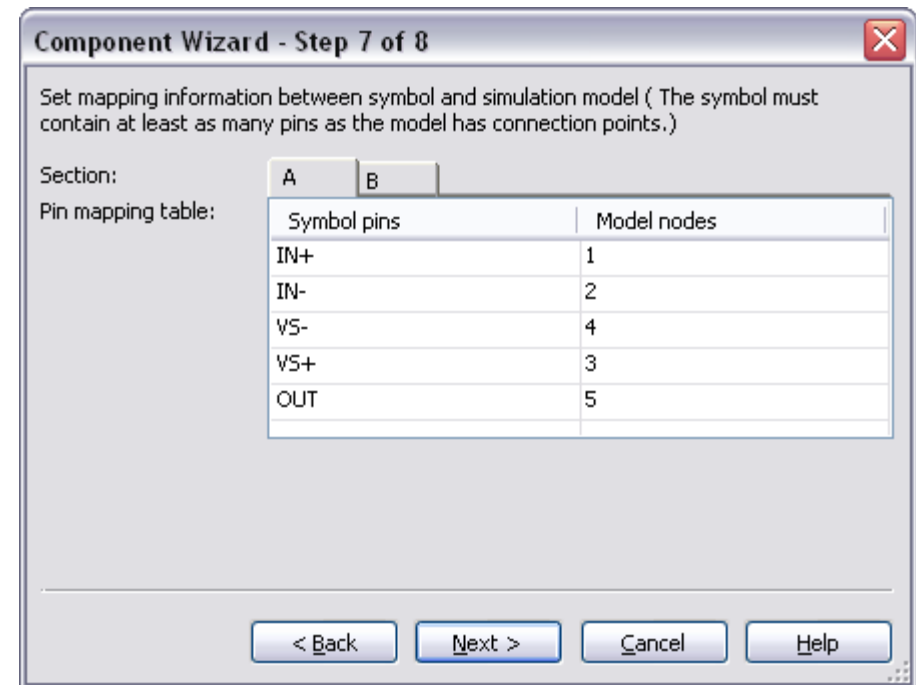
Caution: Model accuracy can only be guaranteed by the component manufacturer.

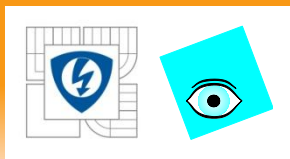


- **Step 7: Set Mapping Information Between Symbol and Simulation Model**
 - Model nodes are in order of appearance
 - Set model node per pin
 - Set model nodes per section



Caution: The accuracy of this mapping will impact the simulation results.





SPICE Model Node
Pin Mapping Table
Model Node Number

Example 1

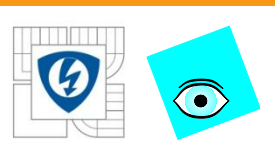
.SUBCKT MUR1605CT A1 K A2 — { A1 → 1
K → 2
A2 → 3

Example 2

.SUBCKT 741 1 2 3 4 5 — { 1 → 1
2 → 2
3 → 3
4 → 4
5 → 5

Example 3

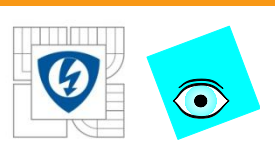
.SUBCKT OP193 51 52 99 50 32 — { 51 → 1
52 → 2
99 → 3
50 → 4
32 → 5



- **Step 8: Save Component to Database**

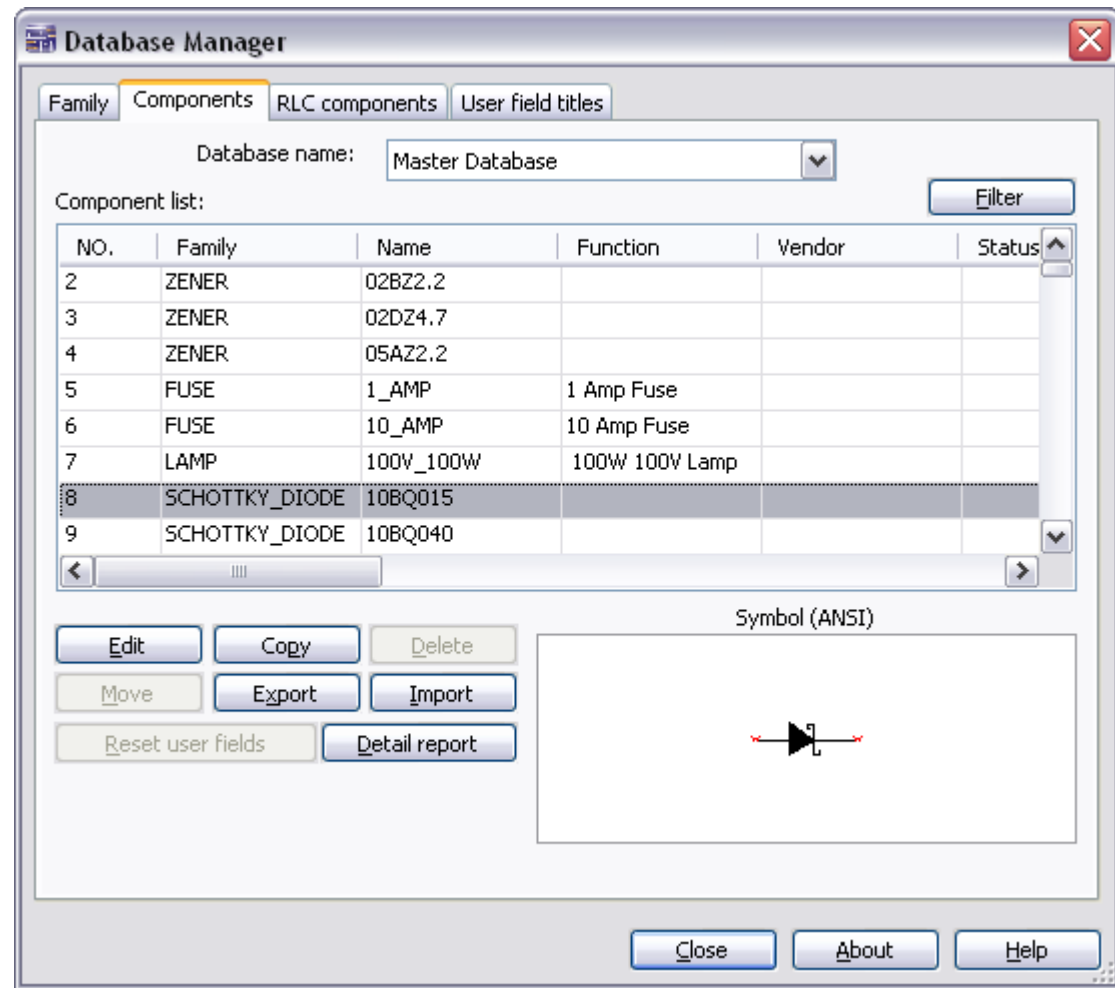
- Select User or Corporate Database
- Select Group and Family
- Modify Family icon from the Database Manager

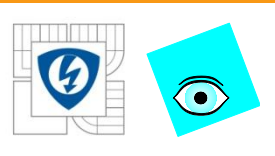




Database Manager

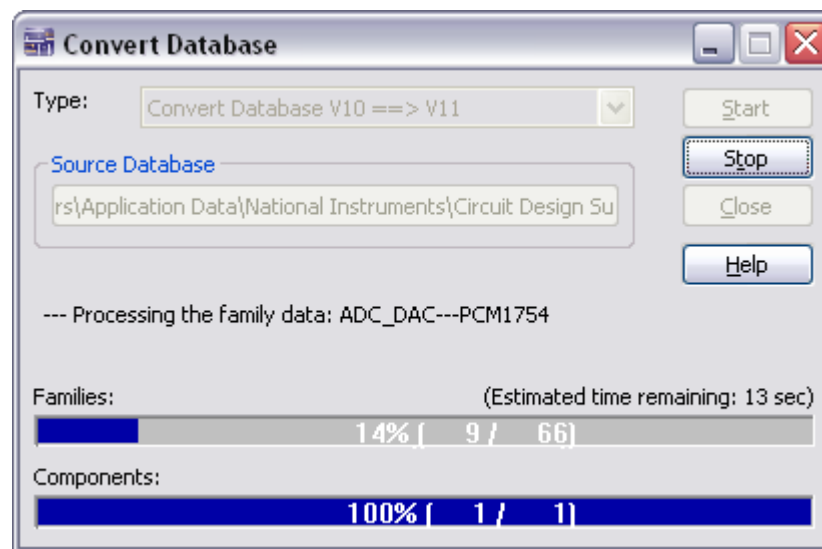
- Manage Master, Corporate and User database
- Edit, copy, delete and move parts
- Import and export components
- Filter allows you to browse quickly
- Create and modify new Families
- Set User Fields



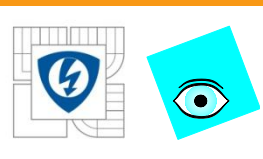


Converting and Merging Databases

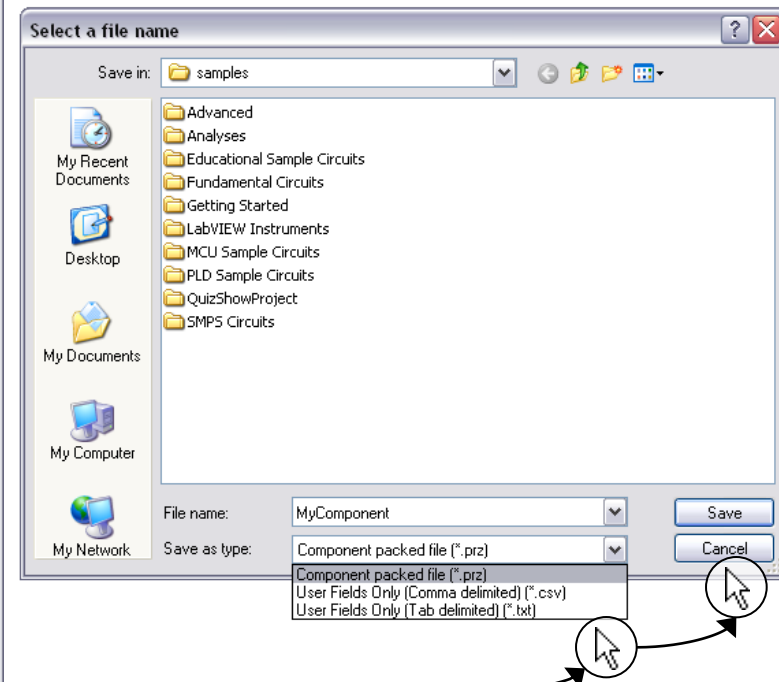
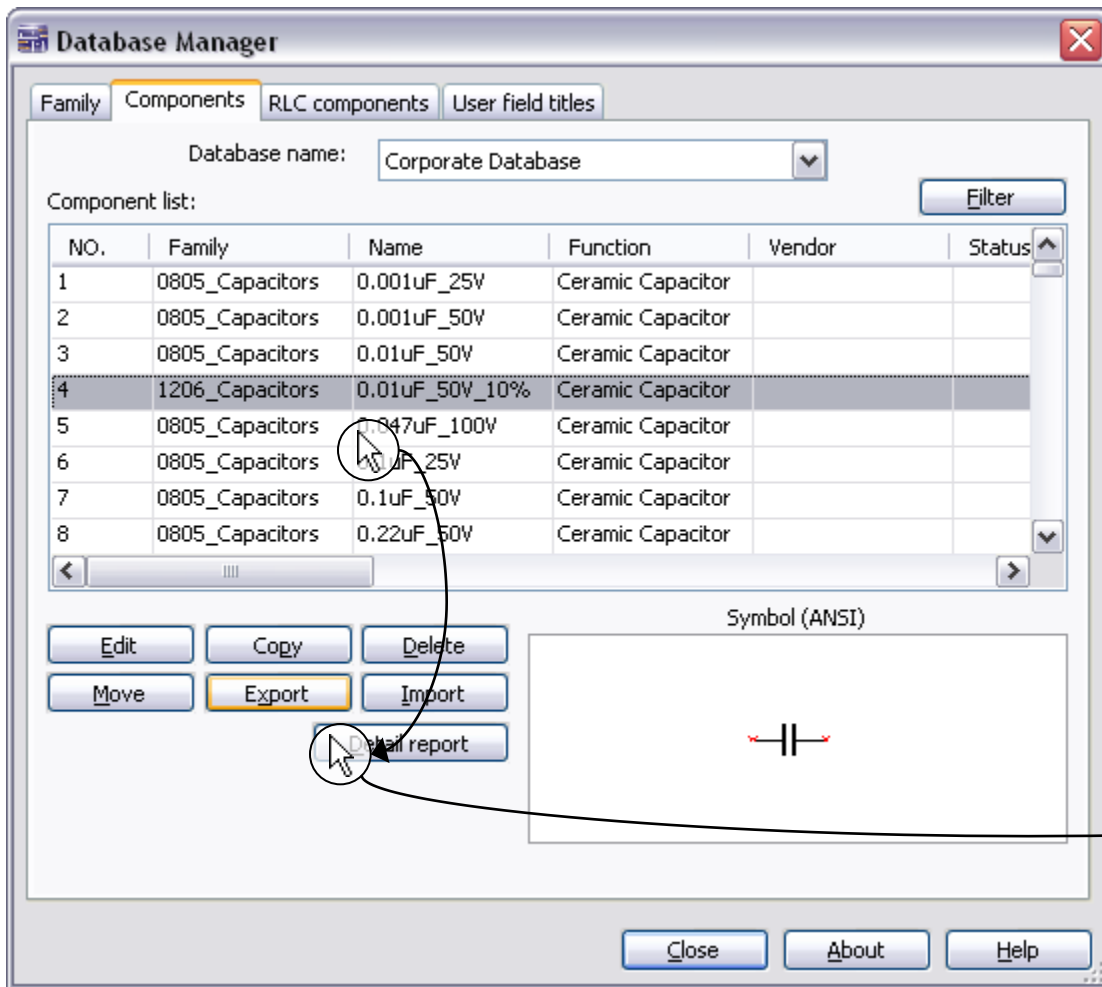
- **Tools»Database»Convert Database**
 - Convert an older version (2001, 7, 8, 9 or 10) database to 11



- **Tools»Database»Merge Database**
 - Merge an existing version 11 database

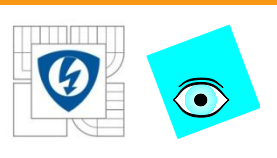


Importing and Exporting Components



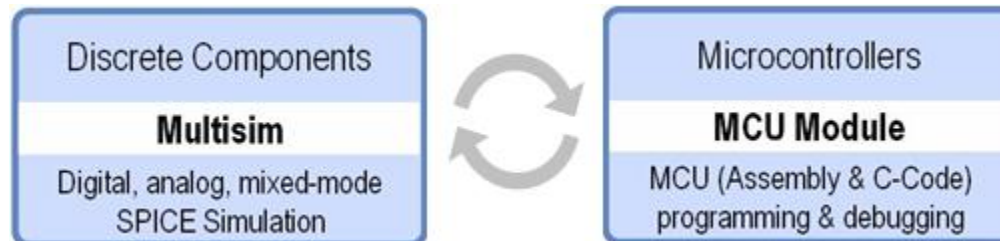
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MCU Co-simulation

- Adds co-simulation capabilities
 - C or assembly with SPICE components
- Simulate like any other circuit

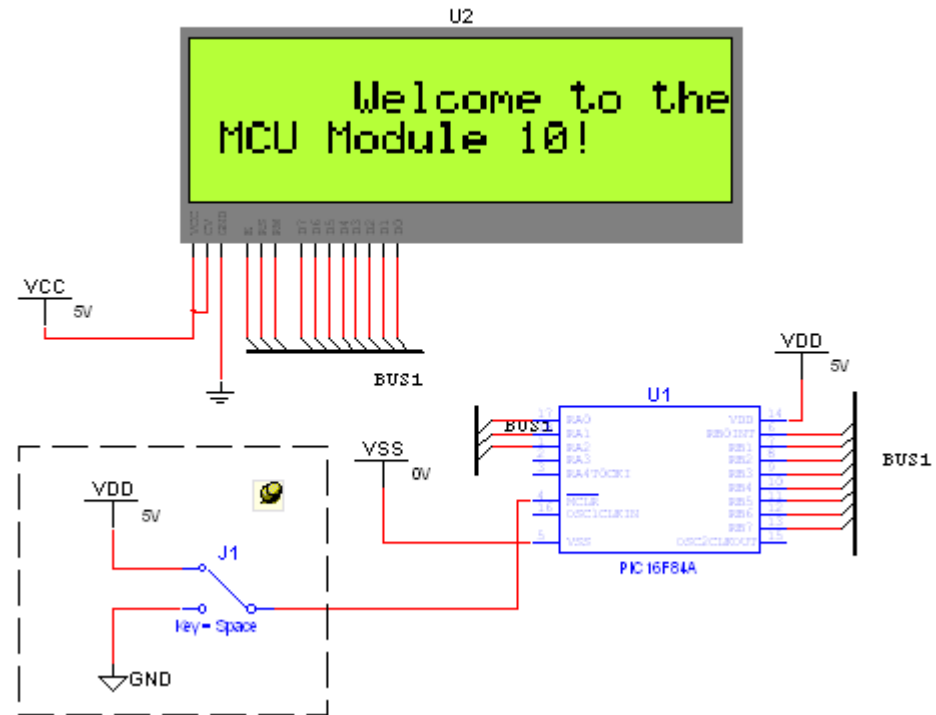


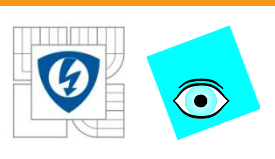


MCU Co-simulation

- Supports:
 - 8051, 8052
 - PIC16F84, PIC16F84A
- Includes peripherals like ROM and RAM
- Advanced peripherals:
 - Keypads
 - LCD Displays
 - VTERM terminal

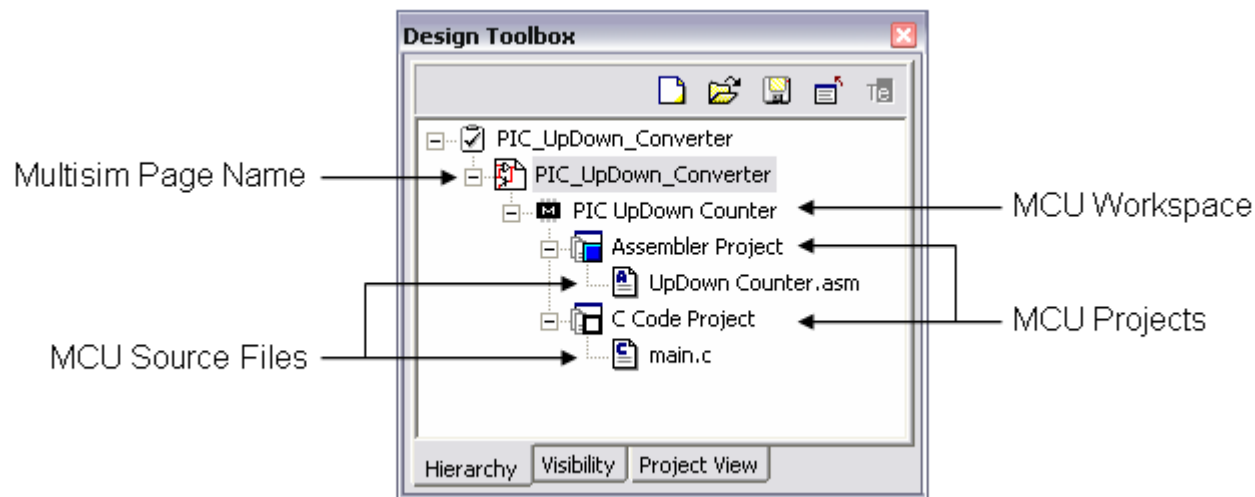
PIC Driven LCD Display

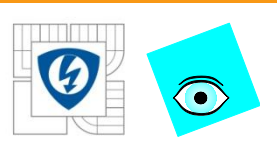




MCU Workspace

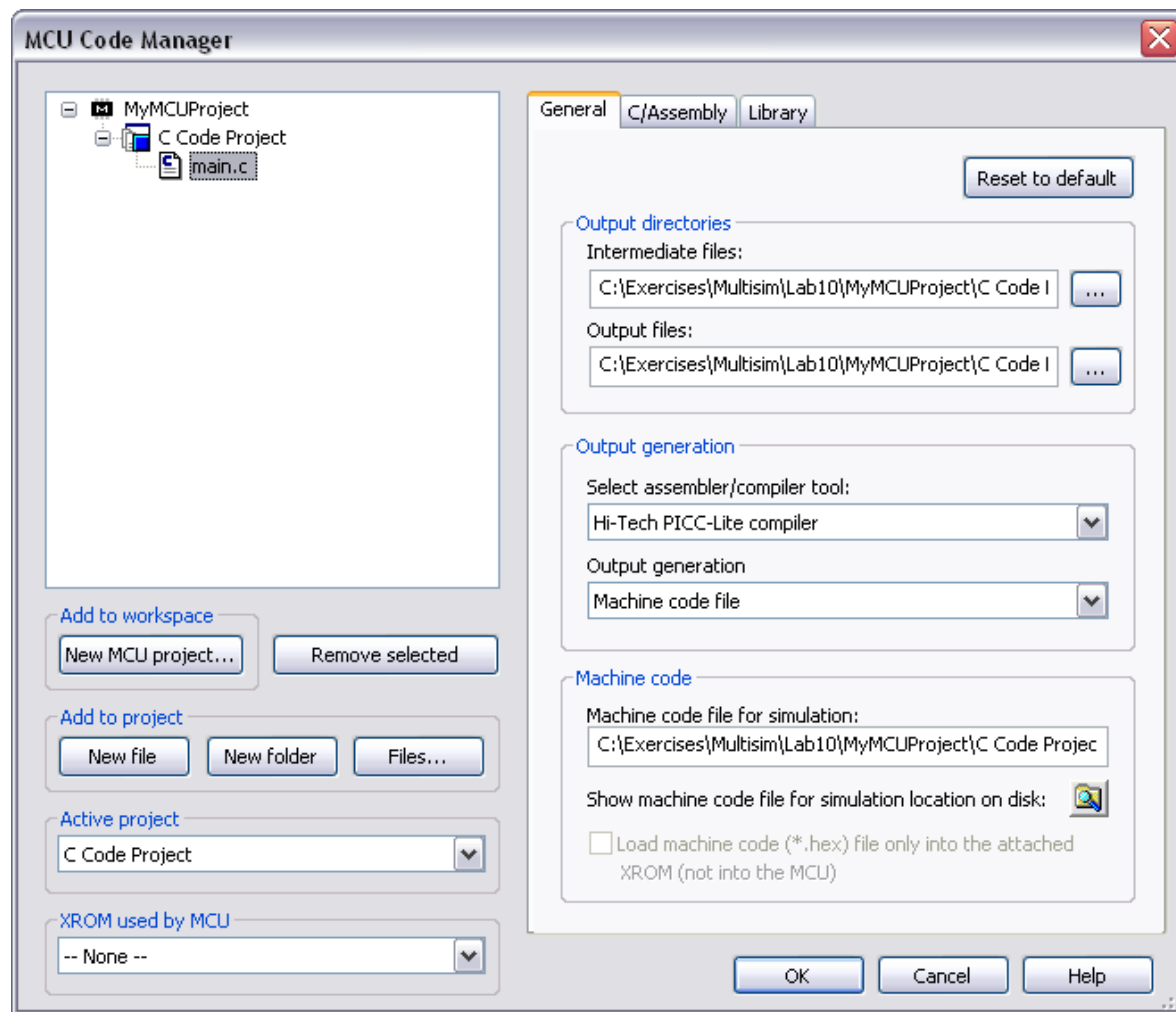
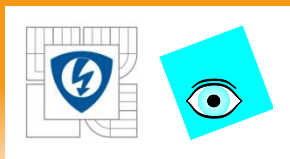
- Dedicated hierarchy in the Design Toolbox
- Organized in projects

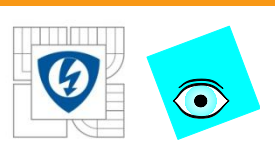




Code Manager

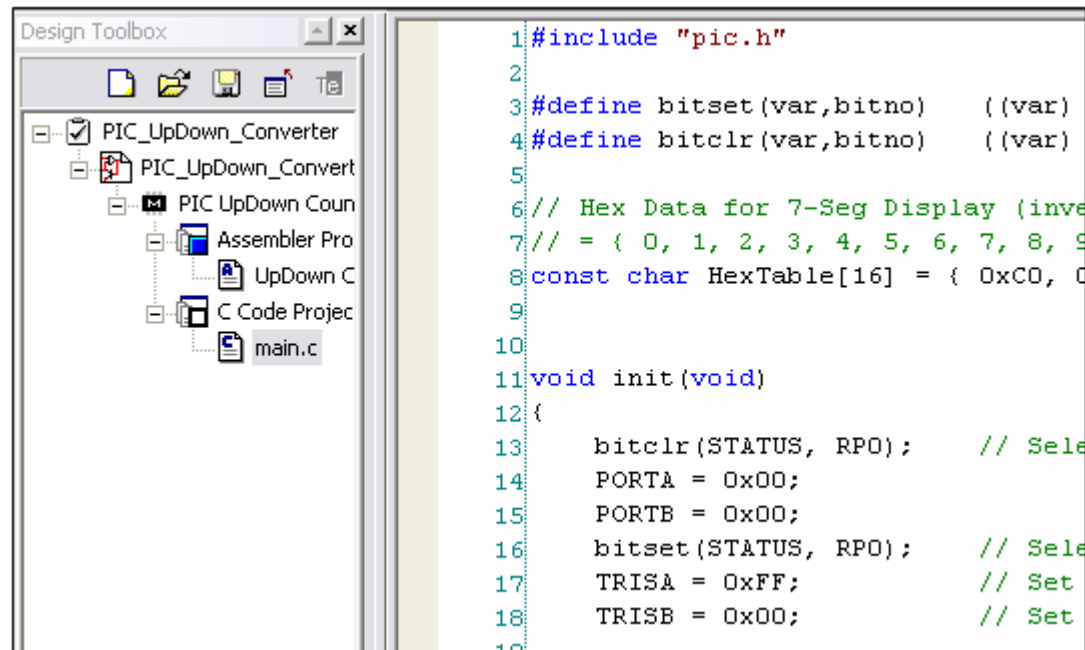
- Manage MCU files
- Enter build settings for source code
- Define compilers
- Create new projects
- Define external ROM (XROM)
- Set special Link or library calls
- **MCU»<MCU name>»MCU Code Manager**

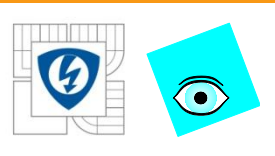




Source Code Editor

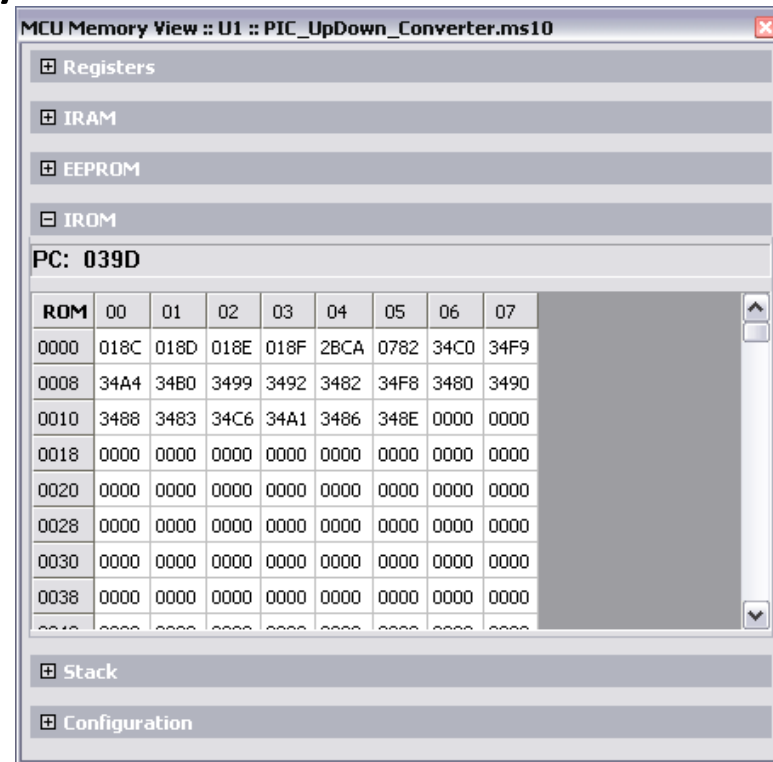
- Click source file in the Design Toolbox to open editor
- Color coded text editor
- Similar to other programming IDEs

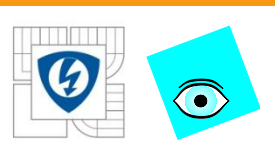




Memory View

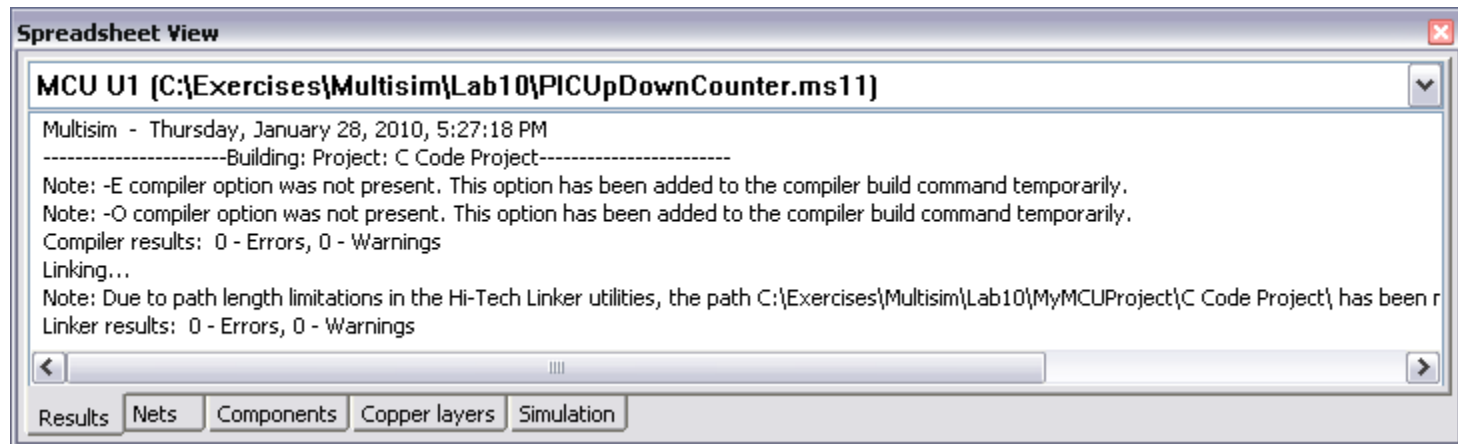
- MCU»<MCU name>»Memory View
- Pause simulation to view memory addresses in real-time
- Click an address to change its value
- Load or save EEPROM hex values



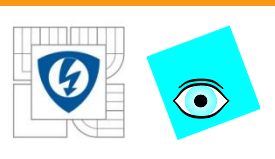


Debugging Features

- Build Process messages in the Results tab of the Spreadsheet View

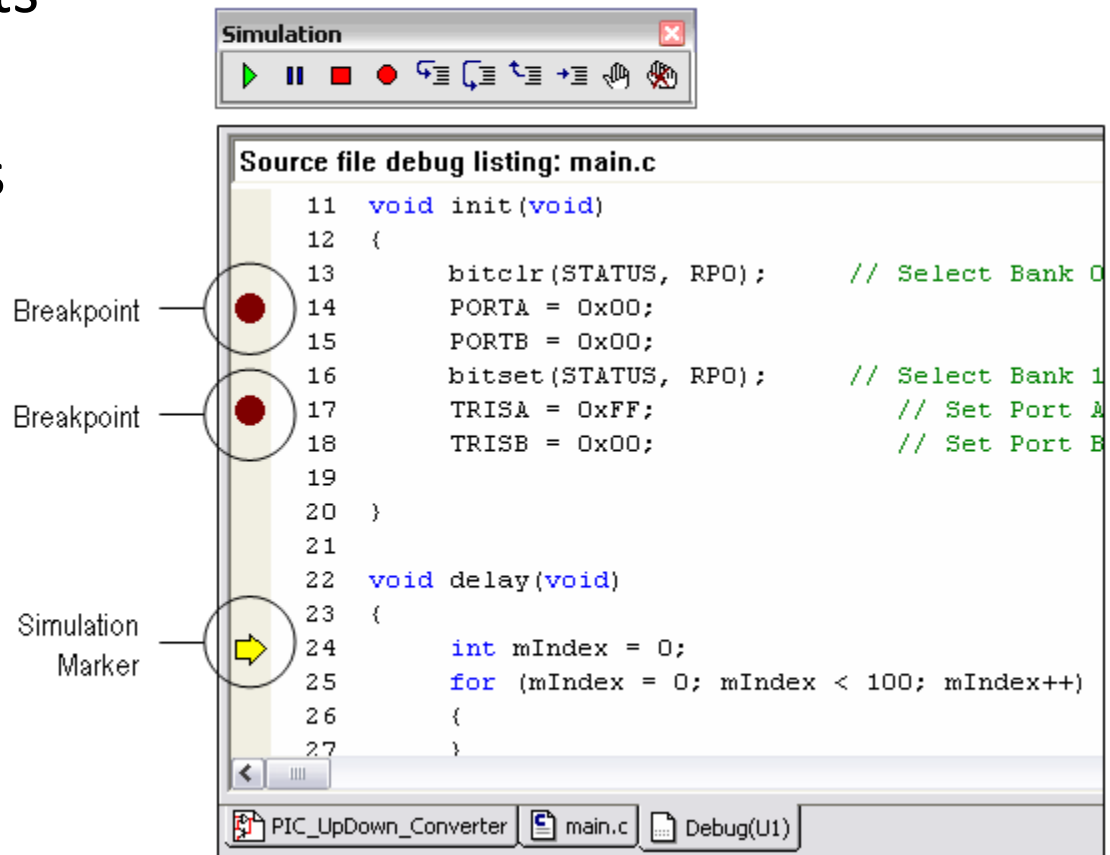


- Debug View lets you follow and track a sequence of events
 - Breakpoints
 - Debug Stepping



Debugging Features – Breakpoints

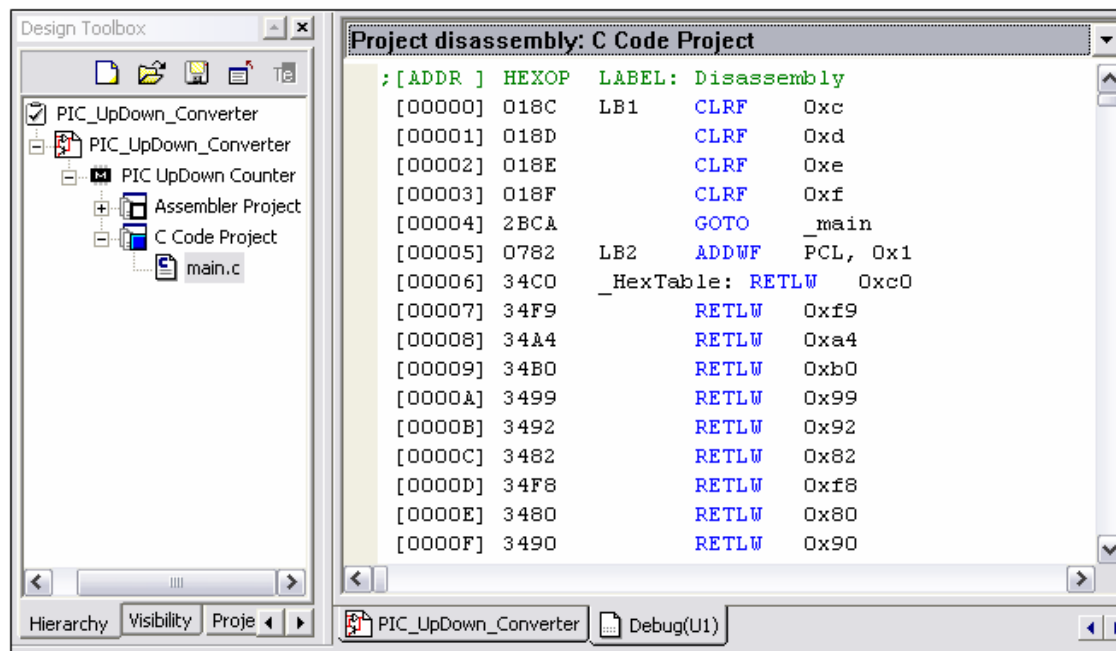
- Place breakpoints in left margin
- Simulation stops at breakpoint
- Use stepping functions
 - Step Into
 - Step Over

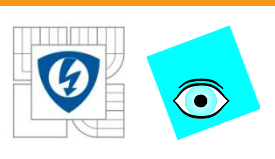




Debugging Features – Disassembly

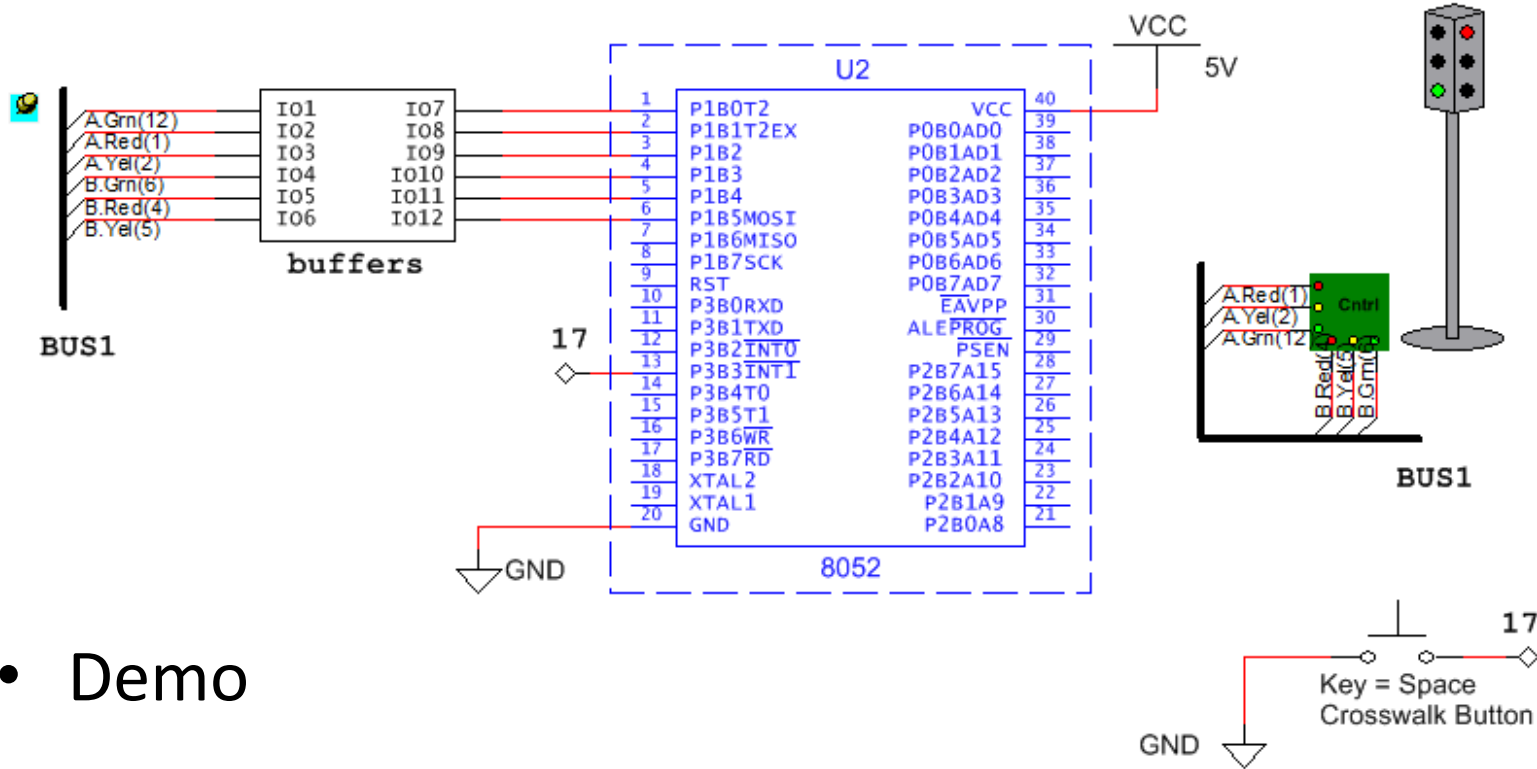
- Debug View drop-down list lets you select
 - Source Code View
 - Disassembly View



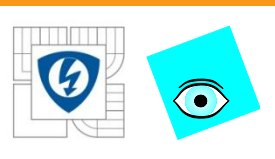


MCU modul

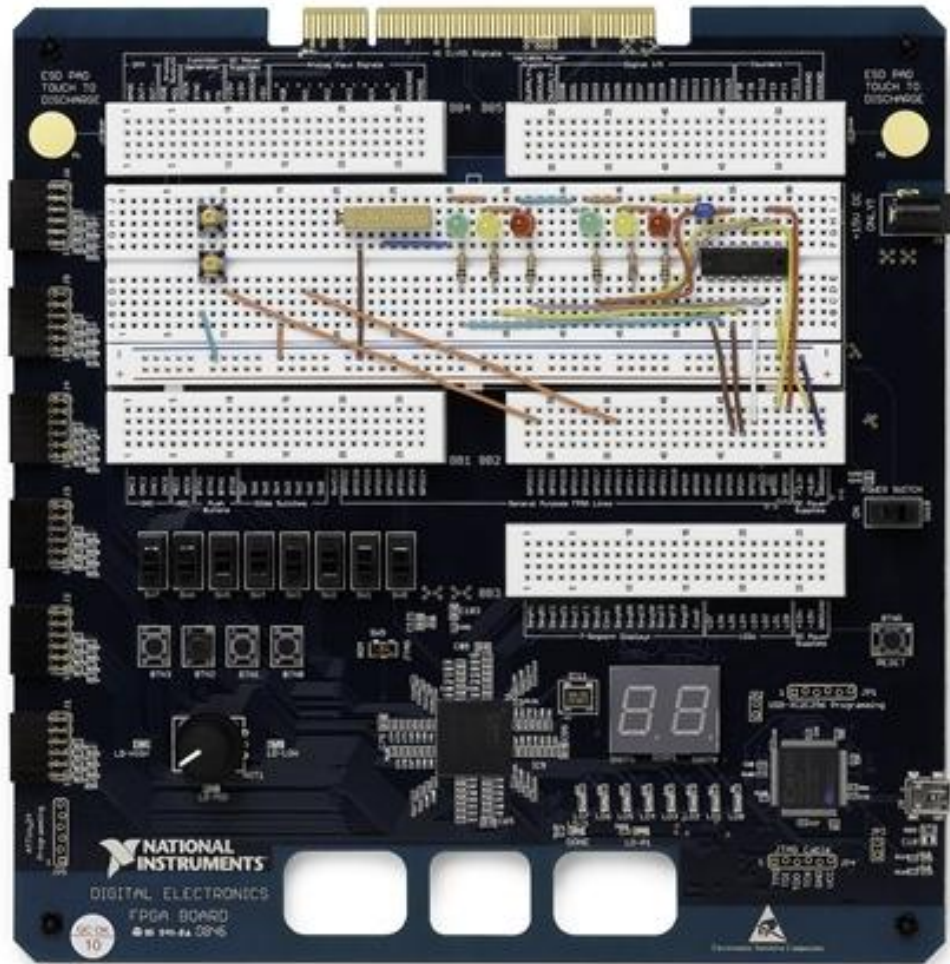
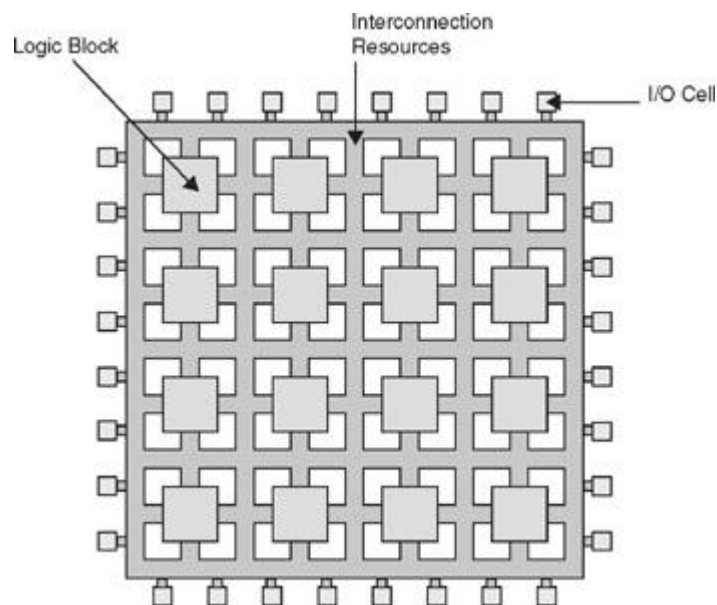
Traffic Light Controller



- Demo

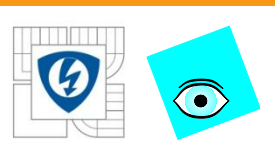


PLD / FPGA modul



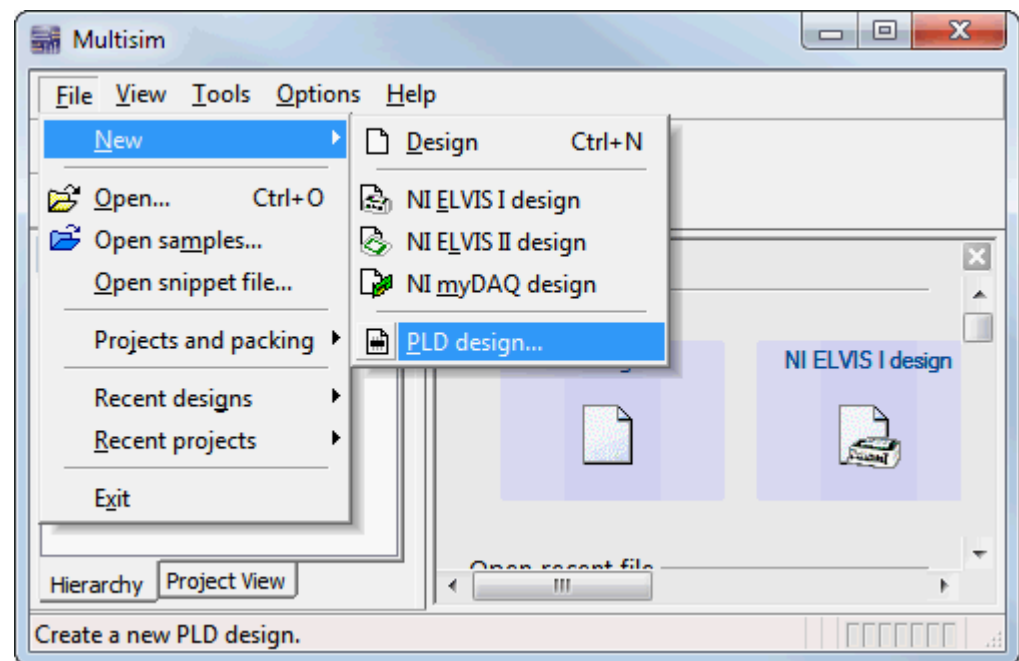
13. 4. 2012

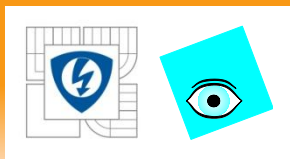
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



PLD / FPGA modul

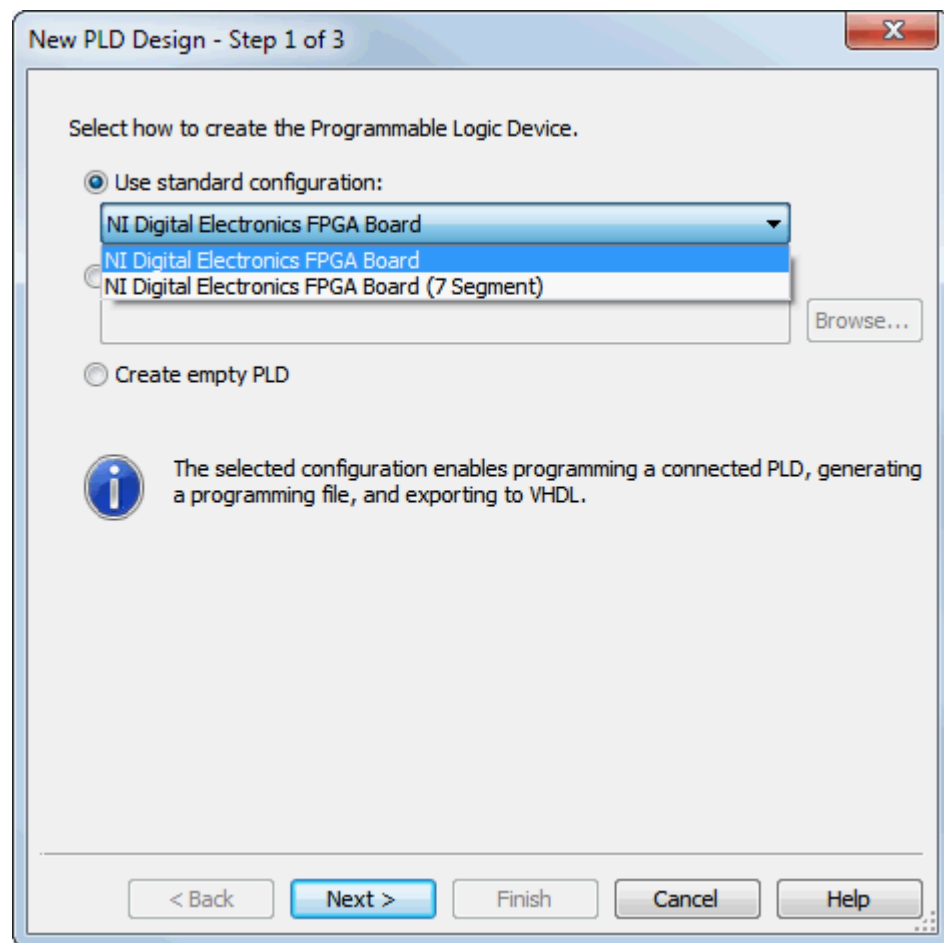
- Create new PLD Design in Multisim

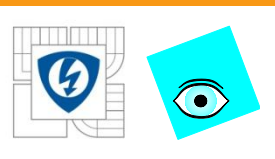




PLD / FPGA modul

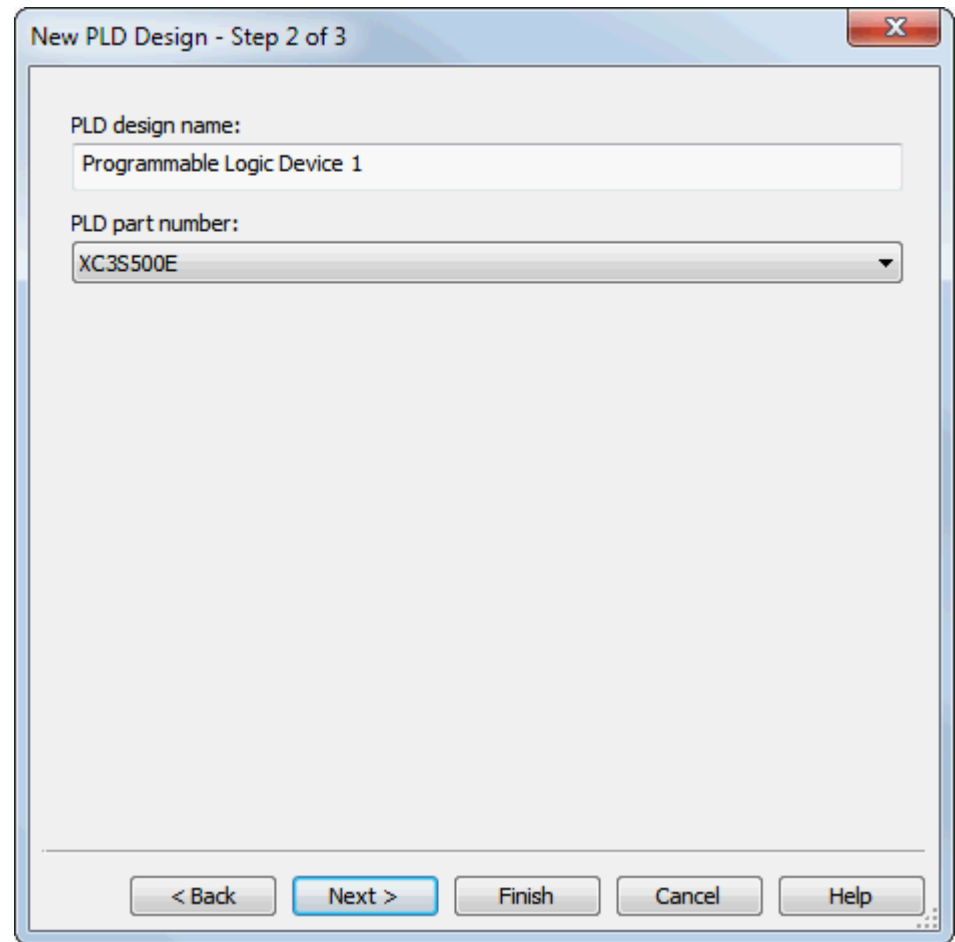
- Select PLD Target

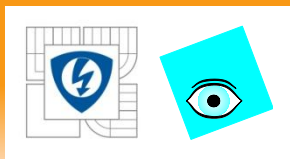




PLD / FPGA modul

- Select PLD family





PLD / FPGA modul

- Select I/Os

New PLD Design - Step 3 of 3

Default operating voltages

Input connector: 3.3 V

Output connector: 3.3 V

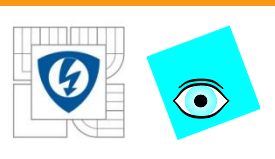
Bidirectional connector: 3.3 V

Select the defined connectors to place on the PLD:

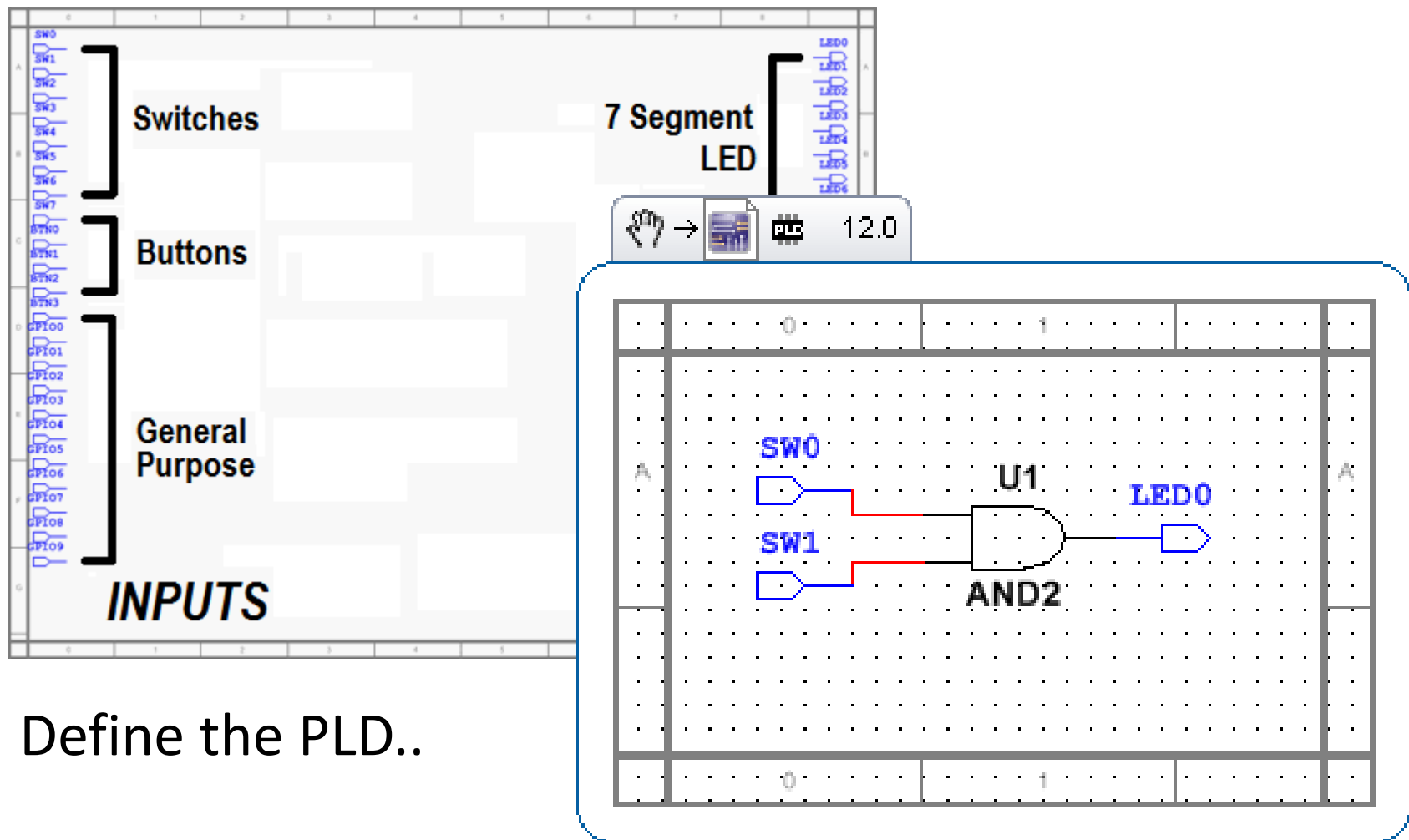
<input type="checkbox"/> AD_CONV	<input type="checkbox"/> COM0	<input checked="" type="checkbox"/> GPIO4	<input type="checkbox"/> GPIO12
<input type="checkbox"/> AMP_CS	<input type="checkbox"/> COM1	<input checked="" type="checkbox"/> GPIO5	<input type="checkbox"/> GPIO13
<input type="checkbox"/> AMP_DO	<input type="checkbox"/> DAC_CLR	<input checked="" type="checkbox"/> GPIO6	<input type="checkbox"/> GPIO14
<input type="checkbox"/> AMP_SHDN	<input type="checkbox"/> DAC_CS	<input checked="" type="checkbox"/> GPIO7	<input type="checkbox"/> GPIO15
<input checked="" type="checkbox"/> BTN0	<input checked="" type="checkbox"/> GPIO0	<input checked="" type="checkbox"/> GPIO8	<input type="checkbox"/> GPIO16
<input checked="" type="checkbox"/> BTN1	<input checked="" type="checkbox"/> GPIO1	<input checked="" type="checkbox"/> GPIO9	<input type="checkbox"/> GPIO17
<input checked="" type="checkbox"/> BTN2	<input checked="" type="checkbox"/> GPIO2	<input type="checkbox"/> GPIO10	<input type="checkbox"/> GPIO18
<input checked="" type="checkbox"/> BTN3	<input checked="" type="checkbox"/> GPIO3	<input type="checkbox"/> GPIO11	<input type="checkbox"/> GPIO19

Check all Uncheck all

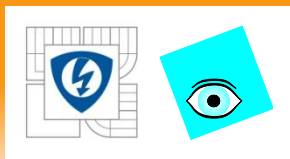
< Back Next > Finish Cancel Help



PLD / FPGA modul

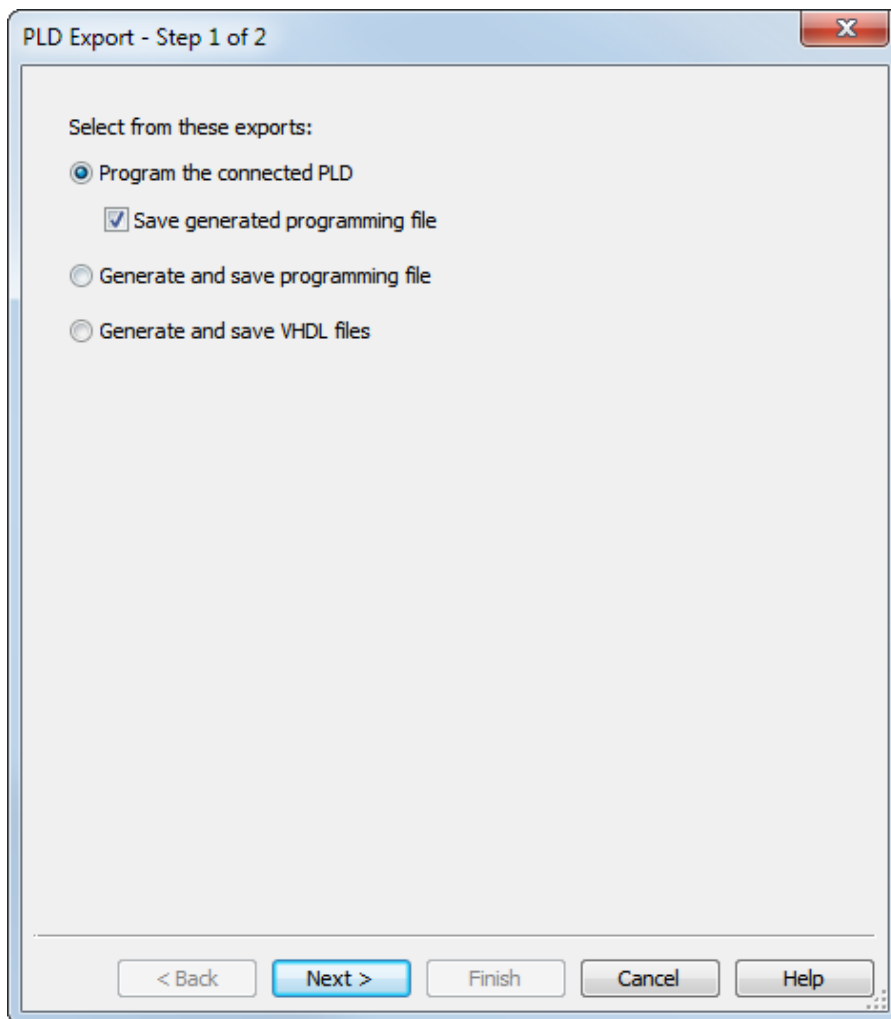


- Define the PLD..



PLD / FPGA modul

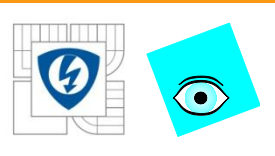
Transfer»Export to PLD...



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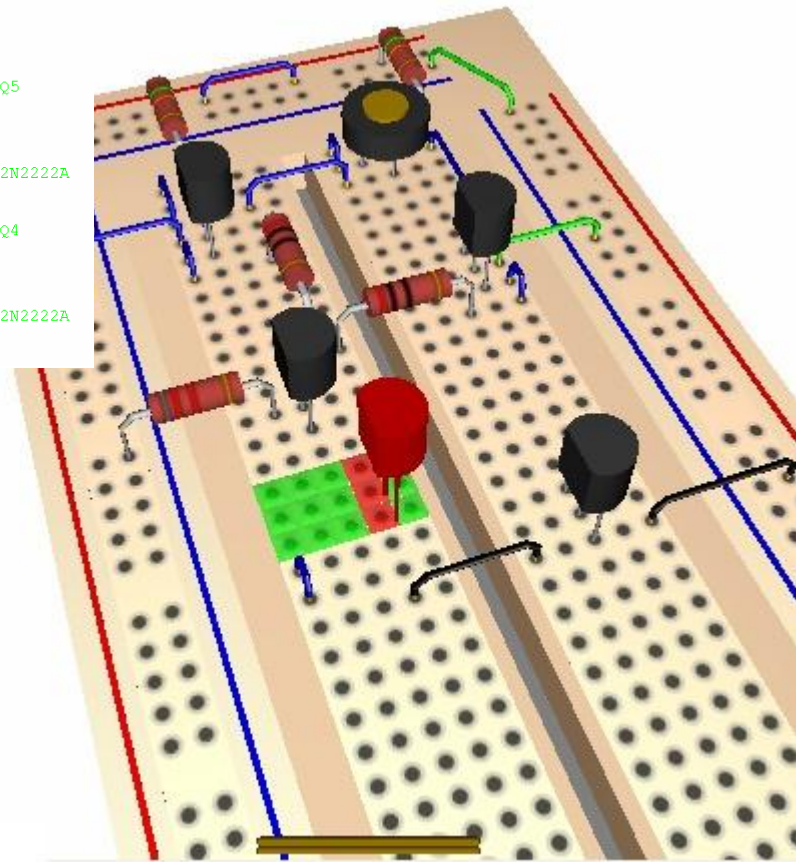
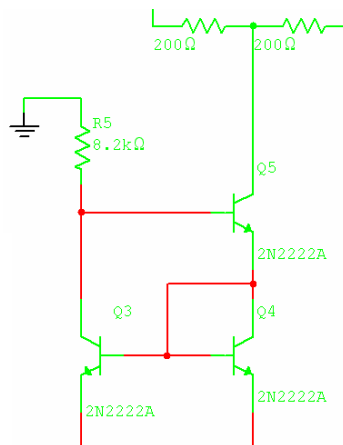
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

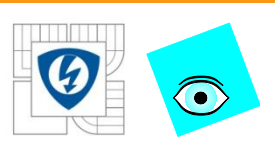




3D Breadboard

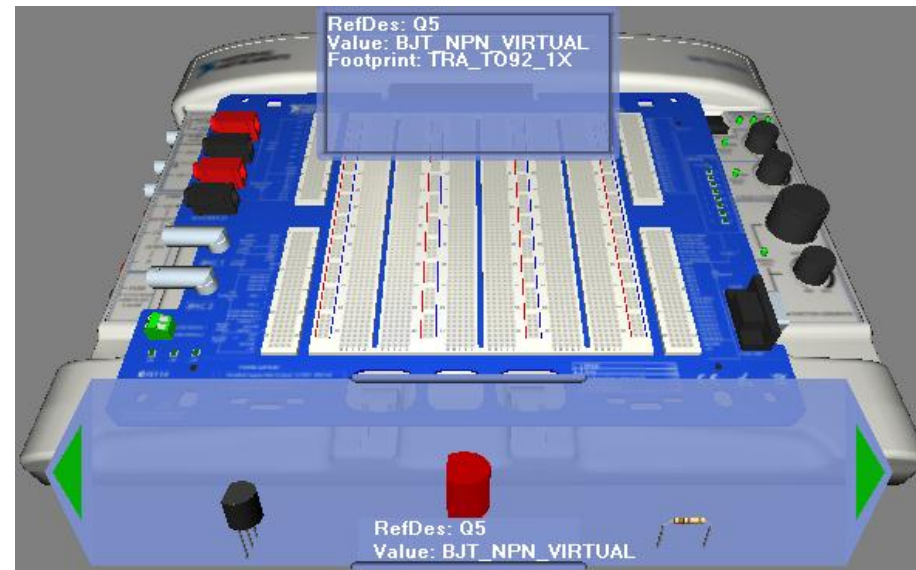
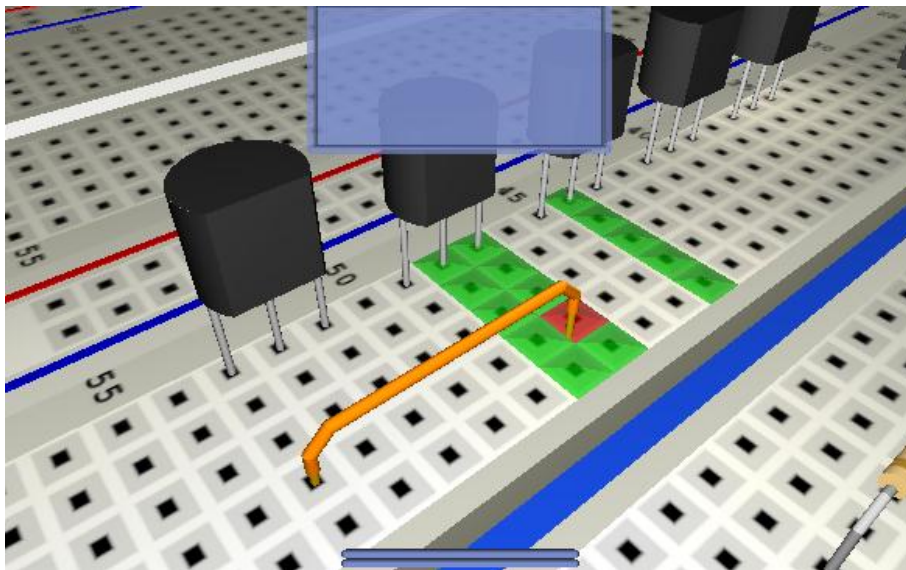
- Place components in 3D on a virtual breadboard
- Practice wiring a breadboard based on a circuit diagram
- Component symbols and wires turn green when placed correctly on breadboard





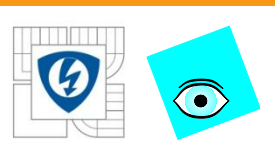
3D ELVIS Breadboard

- **File»New»NI ELVIS I Design ... Or NI ELVIS II Design**
- Interact with NI ELVIS instruments
- Place and verify diagram similar as the virtual breadboard



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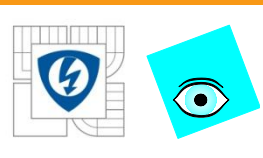
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



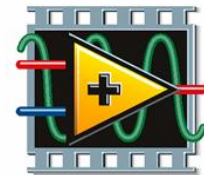
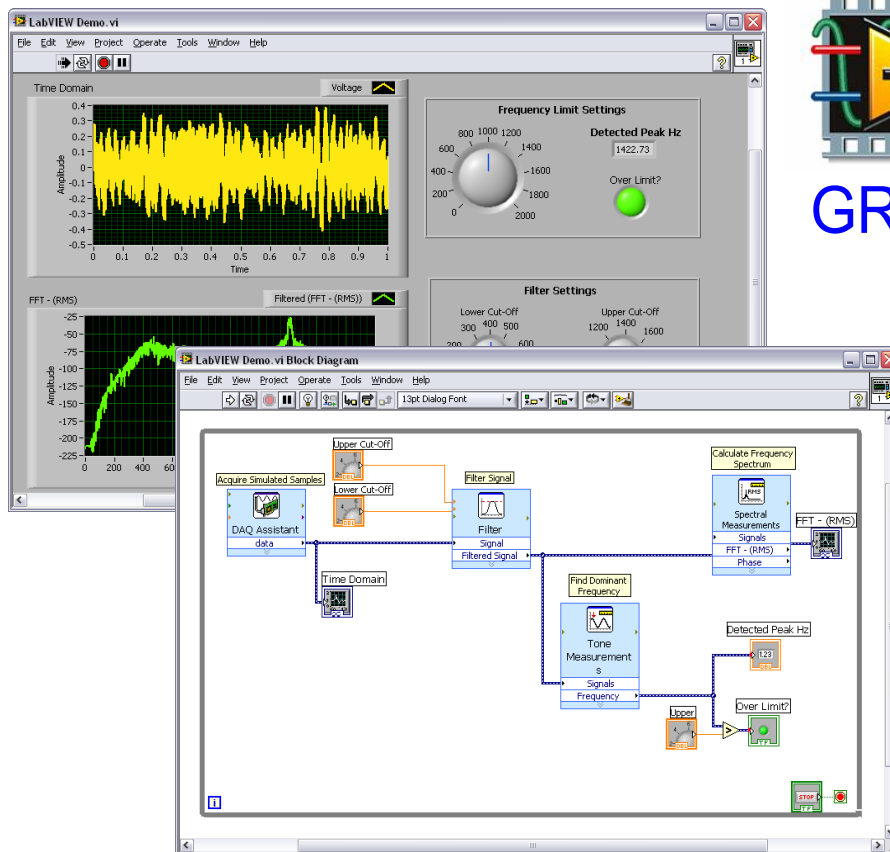
E. Measurement and Comparisons

*“In theory, theory and practice are the same.
In practice, they are not.”
- “Yogi” Berra*





Introduction to LabVIEW



NATIONAL INSTRUMENTS

LabVIEW™

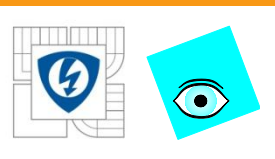
GRAPHICAL PROGRAMMING

FOR ENGINEERS AND SCIENTISTS

13. 4. 2012

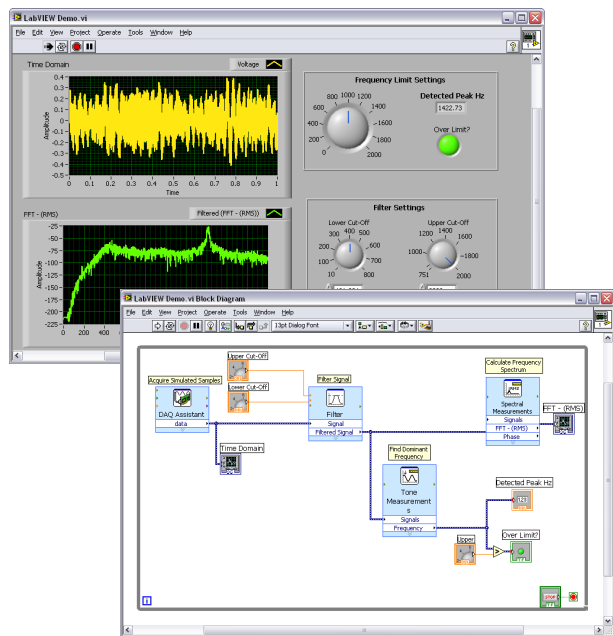
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LabVIEW Graphical Development System

- Graphical Programming Environment
- Compile code for multiple OS and devices
- Useful in a broad range of applications

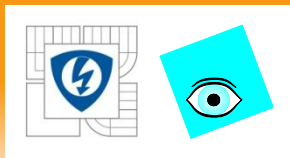


LabVIEW Graphical Development Platform for Design, Control, and Test

Embedded Design and Prototyping		Industrial Monitoring and Control		Automated Test and Measurement	
Filter Design/DSP	Advanced Control	HMI/SCADA	Data Logging and NVH	Communications Test	
System Prototyping	Industrial Control (PID)	Machine Vision and Motion		ATE	
Computing Targets					
 Desktop	 Industrial	 Mobile	 Embedded		

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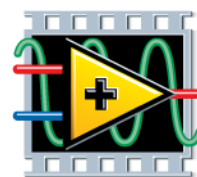
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Virtual Instrumentation Applications

- **Design**
 - Signal and Image Processing
 - Embedded System Programming
 - (PC, DSP, FPGA, Microcontroller)
 - Simulation and Prototyping
 - And more...
- **Control**
 - Automatic Controls and Dynamic Systems
 - Mechatronics and Robotics
 - And more...
- **Measurements**
 - Circuits and Electronics
 - Measurements and Instrumentation
 - And more...

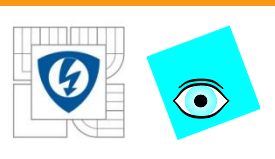
Graphical System Design



NATIONAL INSTRUMENTS

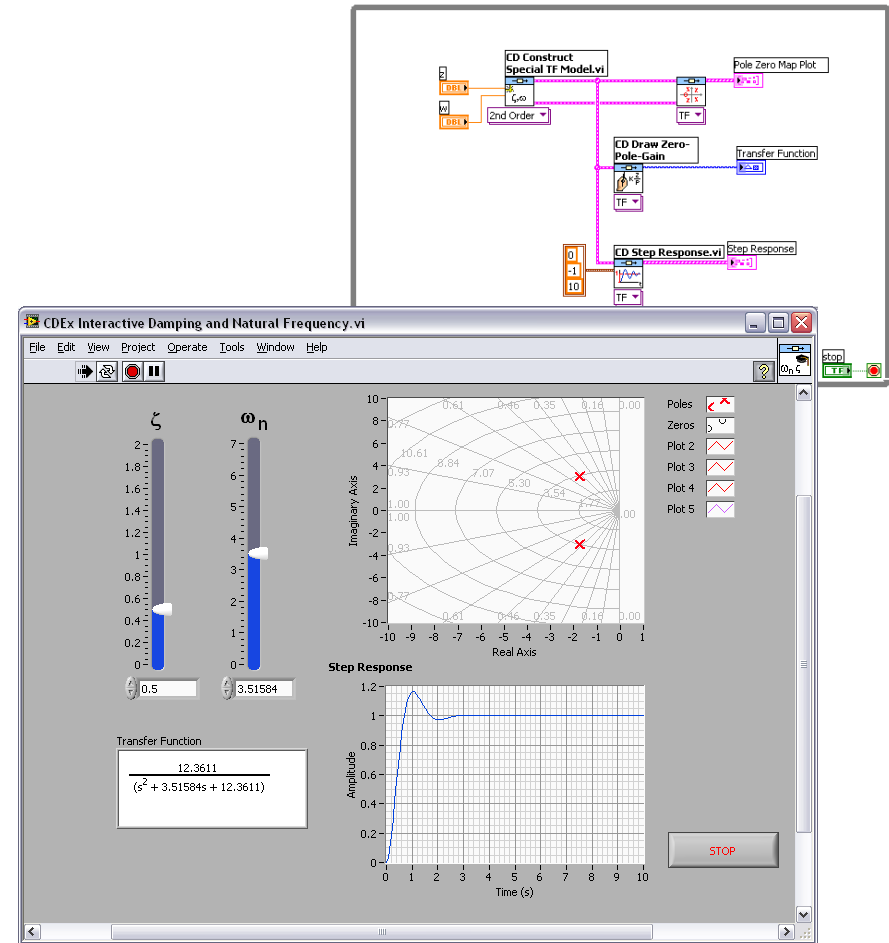
LabVIEW™

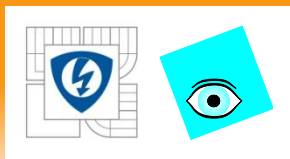
Demo



LabVIEW Control Design

- Easily create interactive control design and analysis VIs
- Use both textual .m file and graphical approach
- Model construction, conversion and reduction
- Time and frequency response
- Dynamic characteristics
- Classical control design including *analytical PID*
- State-space control and estimation - *LQR, LQG, Model Predictive Control, Kalman Filter..*





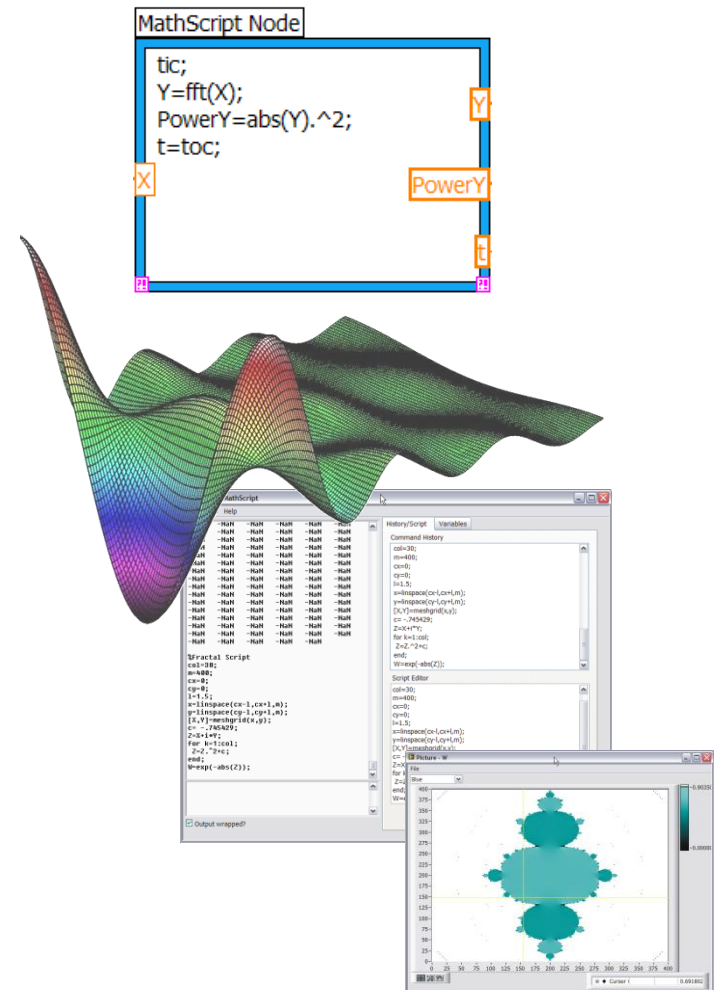
LabVIEW MathScript RT

- **Powerful textual programming for Control Design, Signal Processing, and Math**

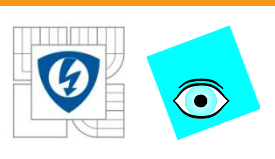
- Hundreds of built-in functions
- Reuse many of your m-file scripts created with The MathWorks, Inc.'s MATLAB® software and others
- Partially based on original math from MATRIX_x

- **A native LabVIEW solution**

- Interactive and programmatic interfaces
- Does not require 3rd party software

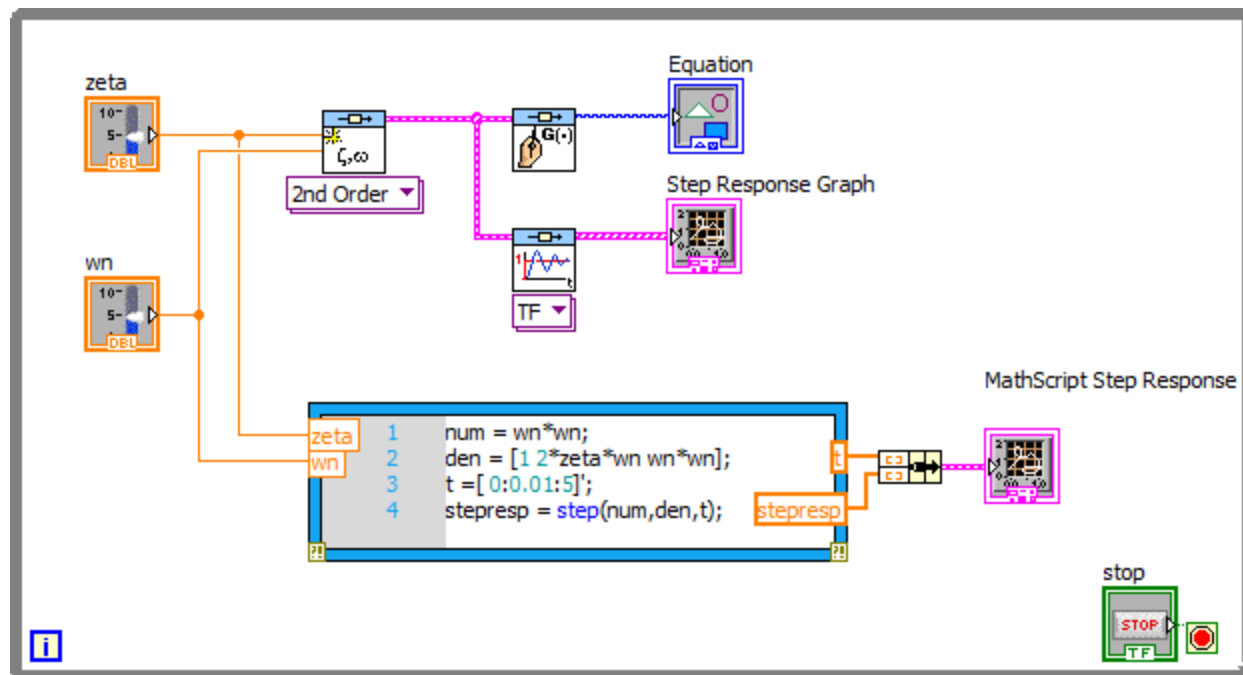


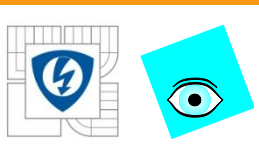
MATLAB® is a registered trademark of The MathWorks, Inc.



LabVIEW MathScript RT Demo

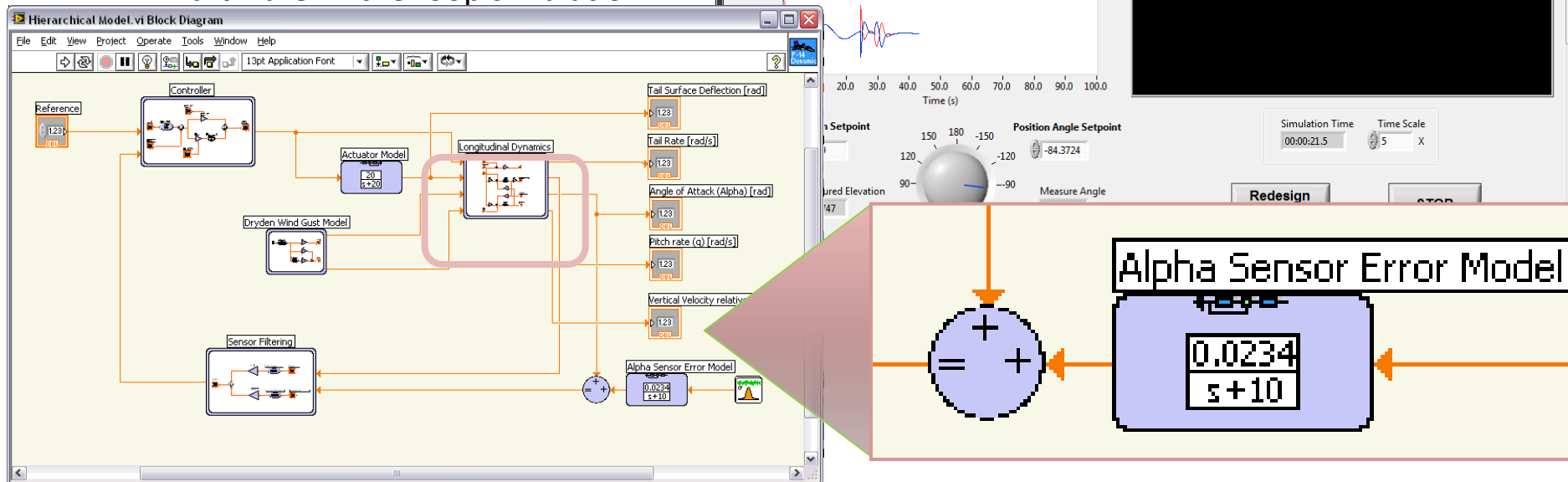
- Graphical and textual programming
- Interactive user-interface





Dynamic System Simulation & Control

- Both signal flow and .m file development
- Single environment for:
 - Simulation of dynamic systems
 - Real-time implementation for rapid control prototyping or hardware-in-the-loop simulation

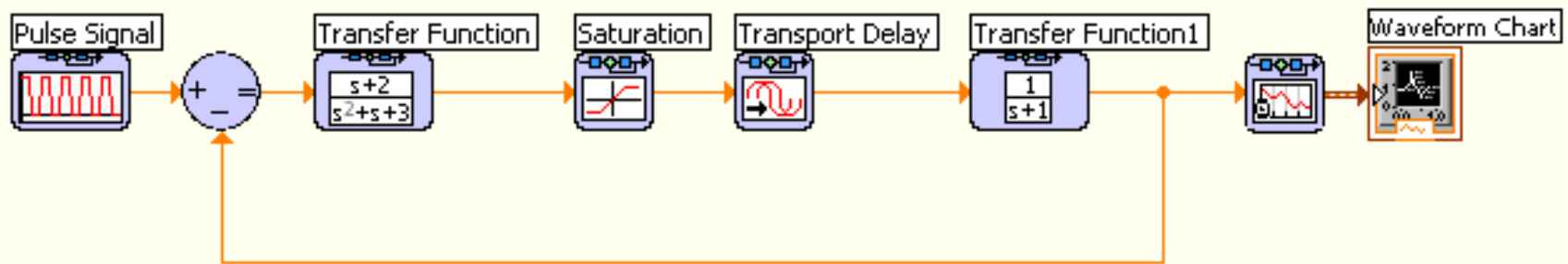


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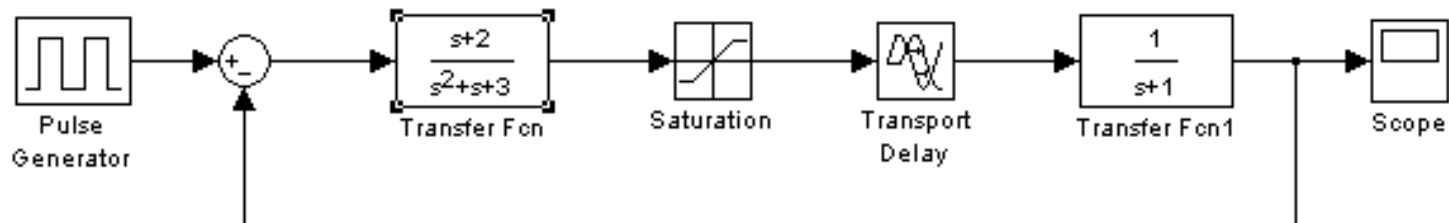
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Standard Notation Reduces Learning Curve

- LabVIEW Control Design & Simulation Module



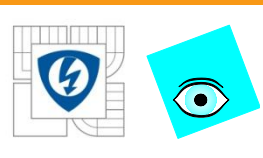
- The Simulink[®] software environment



Simulink[®] is a registered trademark of The MathWorks, Inc.

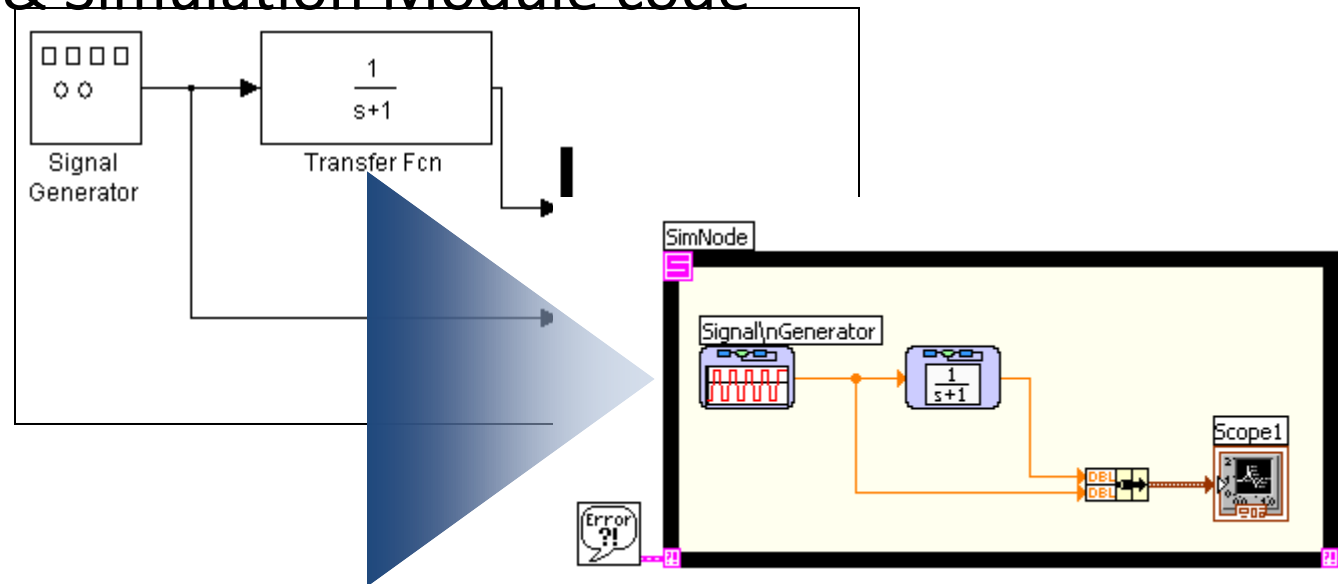
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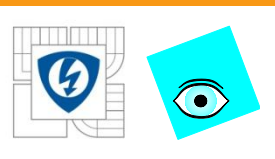


Simulink® conversion

Convert plant and controller models you create in the Simulink® environment into LabVIEW Control Design & Simulation Module code

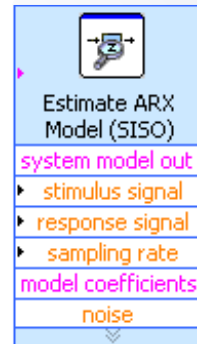
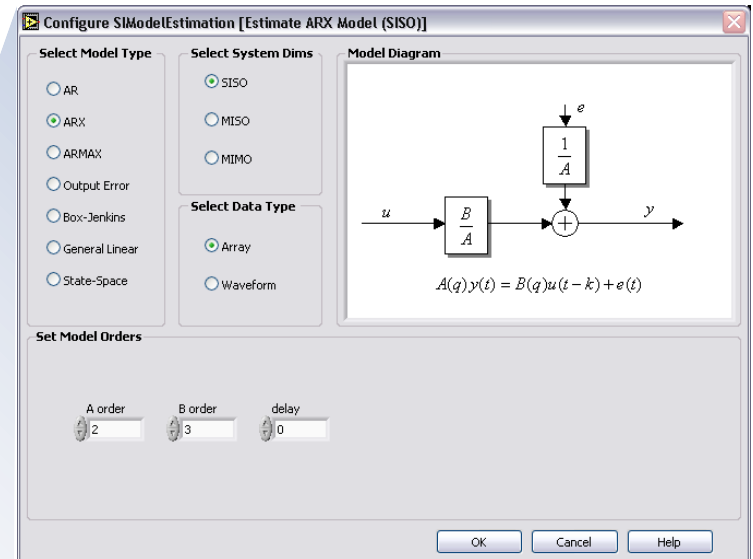


Simulink® is a registered trademark of The MathWorks, Inc.

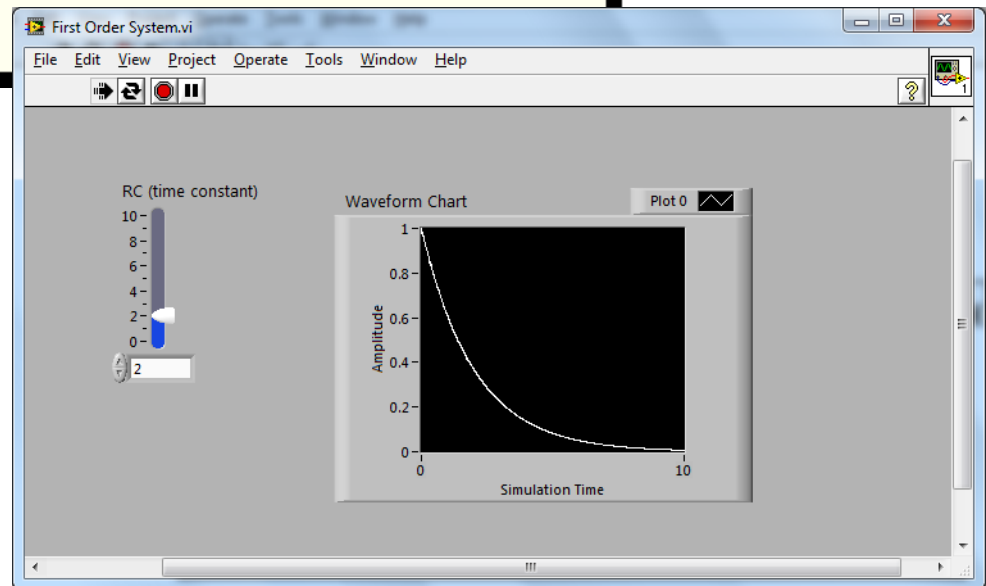
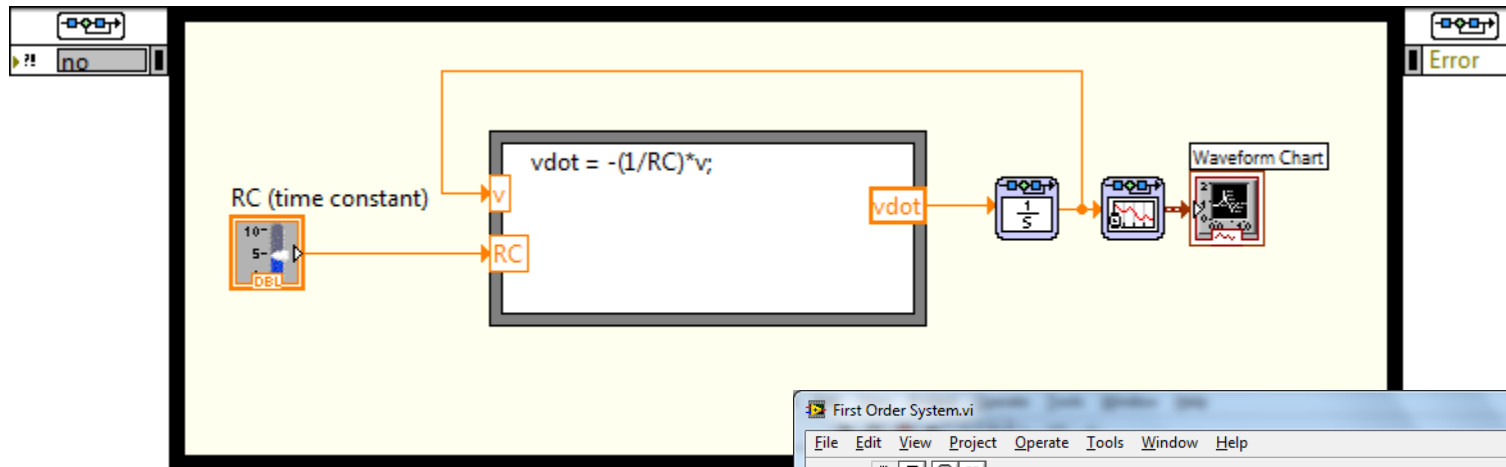


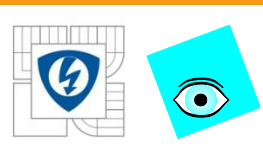
LabVIEW System Identification Toolkit

- Data preprocessing
 - Down Sampling, Remove Trends, Split Signal, Filters
- Parametric model estimation
- Nonparametric model estimation
- MIMO capability
- Nonlinear model estimation
- Grey box system identification
- Closed-loop system identification
- Model validation
- System identification assistant



Solving ODE Example





NI Platform for Control

LabVIEW Development Environment

**Control Design &
Simulation Module**

System ID Toolkit

Statechart Module

DFD Toolkit

**Simulation Interface
Toolkit**

NI Motion Control

LabVIEW Real-Time

LabVIEW FPGA

LabVIEW Microprocessor

Targets



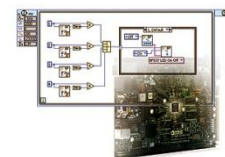
PXI



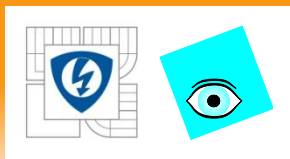
cRIO, sbRIO



Desktops & SBC's

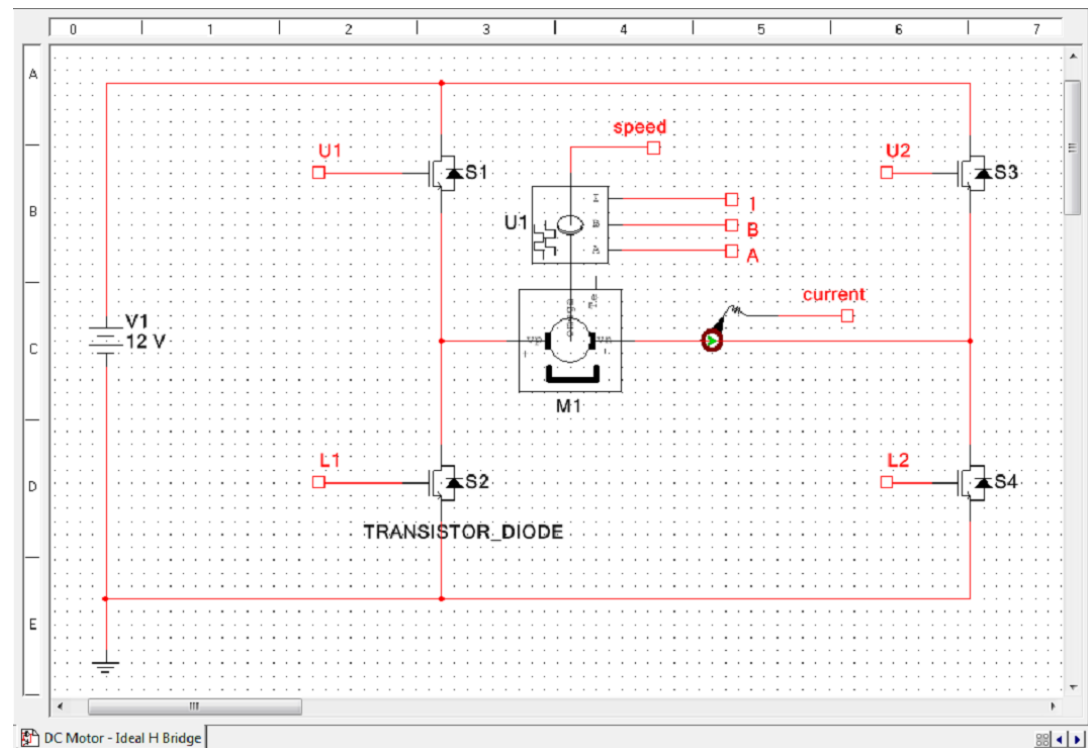


32-bit µp



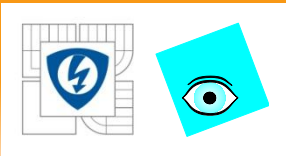
Multisim Power Components

- 92 new component models of power and electromechanical devices
- Reconfigurable transformers
- Power switches
- Power controllers
- Non-ideal RLCs



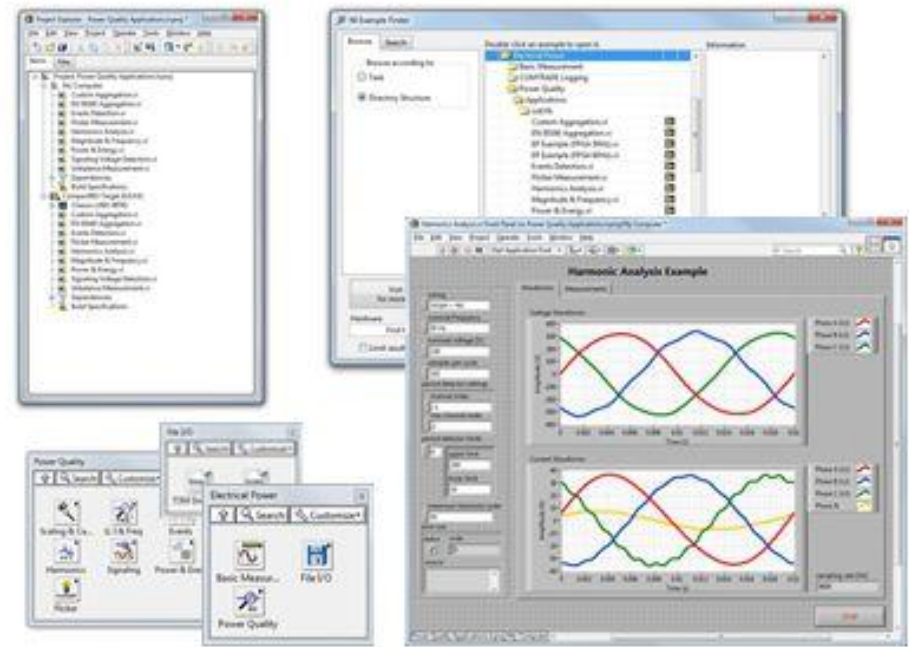
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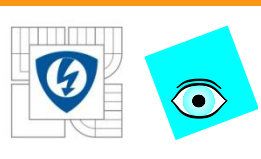
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Electrical Power Measurement Suite

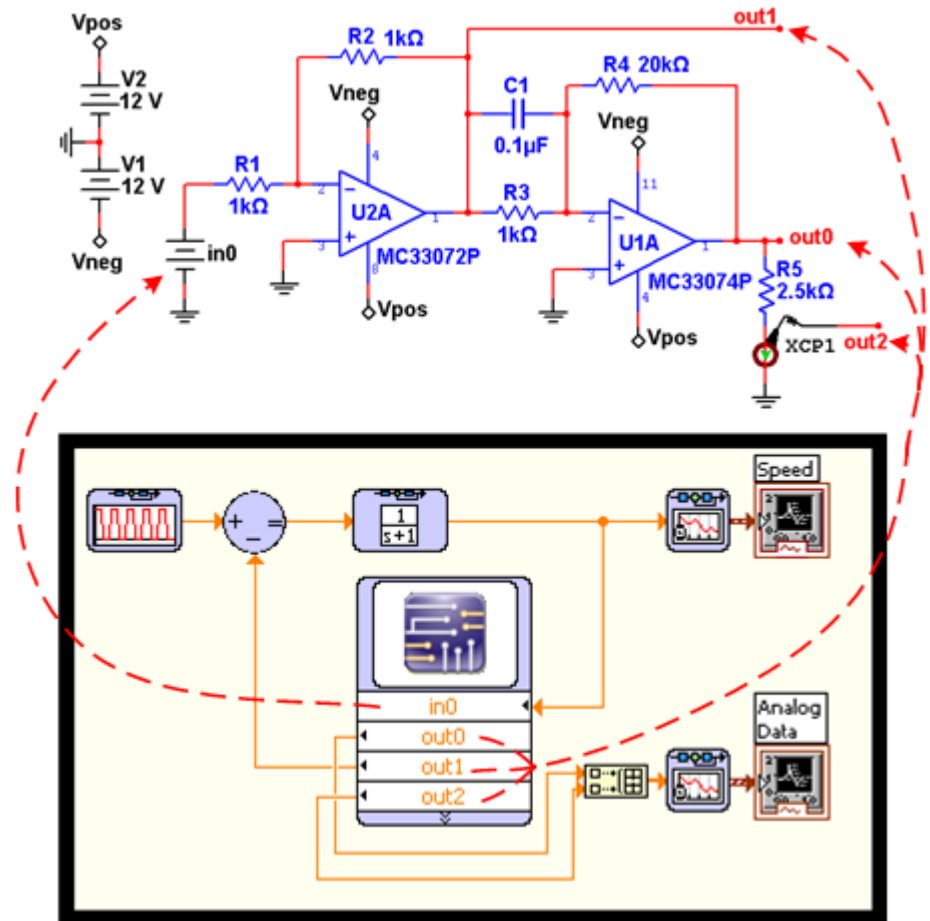
- Measure power quality and energy features to IEC, EN, and IEEE standards
- Harmonics (IEC 61000-4-7)
- Flicker (IEC 61000-4-15)
- Sag/swell/interruption with standard or custom levels (IEC 61000-4-30)
- Rapid voltage change with standard or custom levels (IEC 61000-4-30)
- Compatibility with the COMTRADE (IEEE 37.111) file format





Multisim-LabVIEW Co-simulation

- Control Design and Simulation Module
 - External Modeling Interface (EMI)
- Prototype features:
 - Lock-step synchronization
 - Step-size negotiation
 - Support for all continuous-time LabVIEW solvers
 - Multisim block configuration



Demo

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