Použití mikropočítačů pro vývoj embedded aplikací

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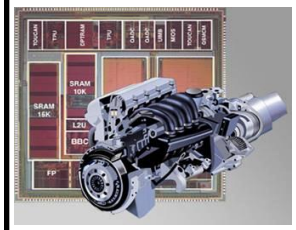
11. – 12. listopadu 2010

Tato prezentace je spolufinancována Evropským sociálním fondem a státním rozpočtem České republiky.

Časový rozvrh

- 09:00 – 10:30 – blok 1
- 10:30 – 10:45 – přestávka
- 10:45 – 12:00 – blok 2
- 12:00 – 13:00 – oběd
- 13:00 – 14:15 – blok 3
- 14:15 – 14:30 – přestávka
- 14:30 – 15:45 – blok 4
- 15:45 – 16:00 – přestávka
- 16:00 – 17:00 – blok 5

The Freescale Controller Continuum

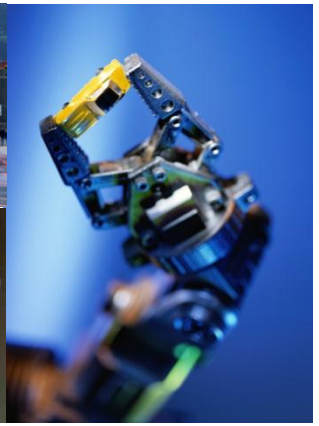


Timing Solutions
Sensor Products
Analog Products
CodeWarrior IDE

08
S08
S12
S12x
Digital Signal Controller
Application Specific
ColdFire
Power PC

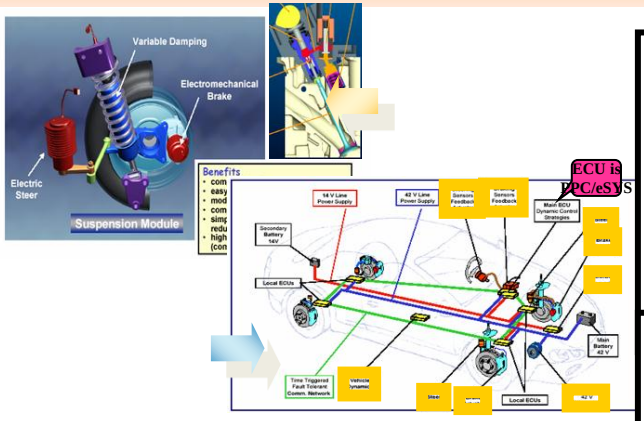
16, 32-bit

Performance



A solution for virtually every project at every account

Digital Signal Controller Target Markets



Automotive

- EPAS, Braking, X-Wire
- Transmission/Valve Actuators
- Alternator Starter, Active Suspension
- Inertial Sensors, BLDC motor

Appliance

- Washing Machine
- Refrigeration, Dishwasher
- Induction Cooking

Appliance

Industrial

- SMPS, Frequency Inverters
- UPS, Electrical Protection
- Plant Equipment

Industrial

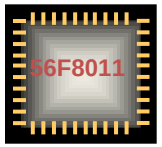
General

- Motor/Motion Control
- Vending machines, Metering
- Security and Safety Systems
- Intelligent toys, Home automation

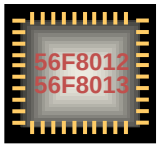
General

DSC56F80xx Products Roadmap

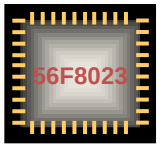
Memory and Features



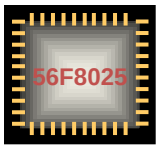
12KB P Flash
2KB RAM
32pin
1 SPI
1SCI
1 I2C
PWM
12bit ADCs
4 Timers



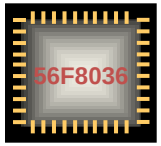
16KB P Flash
4KB RAM
32pin
1 SPI
1 SCI
1 I2C
PWM
12bit ADC
4 timers



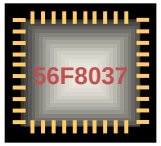
32KB P Flash
4KB RAM
32pin
2 Comparators
1 DAC
1 QSPI
1 QSCI
1 I2C
PWM
12bit ADCs
5 Timers



32KB P Flash
4KB RAM
48pin
2 Comparators
1 DAC
1 QSPI
1 QSCI
1 I2C
PWM
12bit ADCs
7 Timers



64KB P Flash
8KB RAM
48pin
2 Comparators
2 DAC
1 QSPI
1 QSCI
1 I2C
PWM
12bit ADCs
7 Timers
CAN

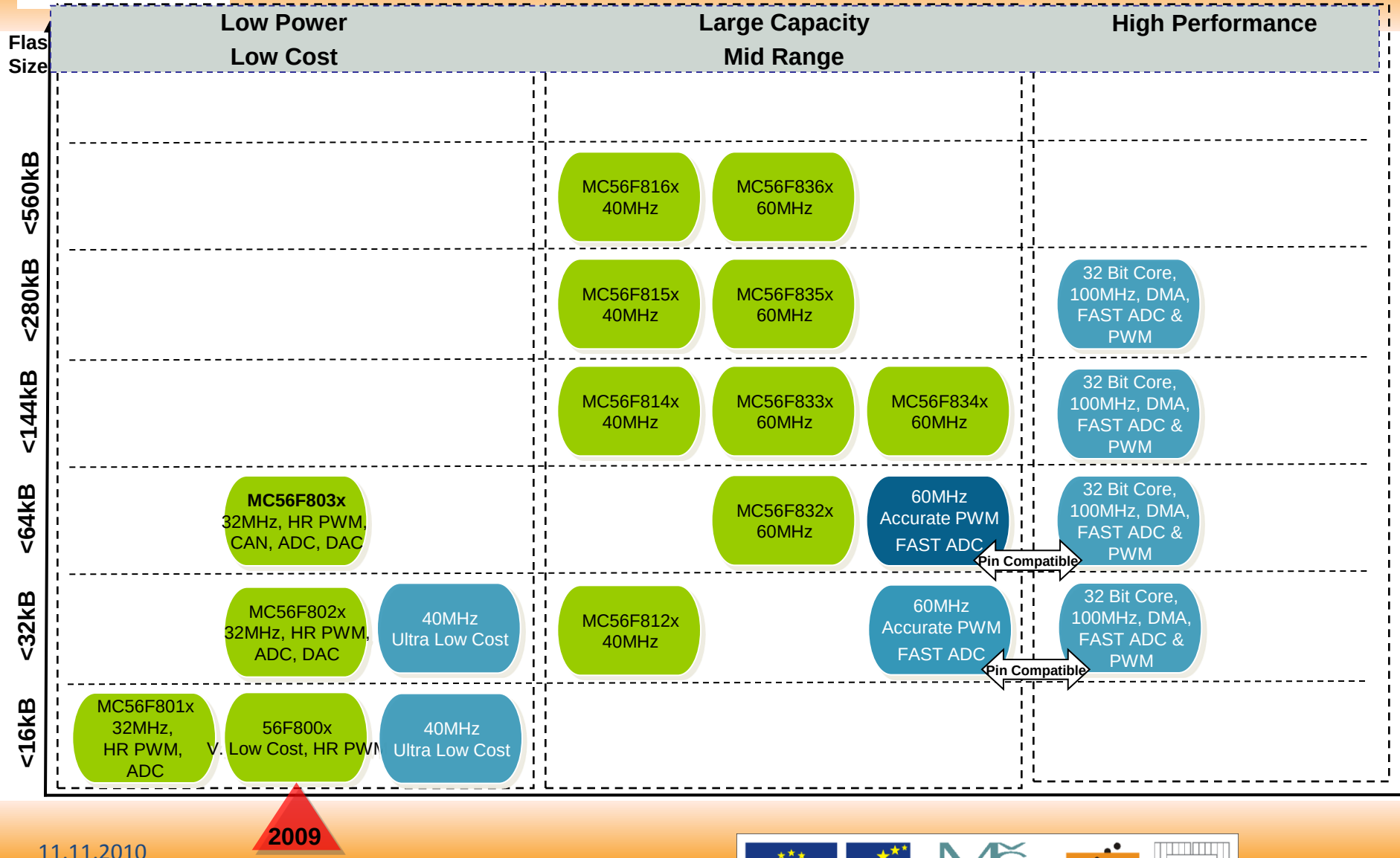


64KB P Flash
8KB RAM
64pin
2 Comparators
2 DACs
2 QSPIs
2 QSCIs
1 I2C
PWM
12bit ADCs
11 Timers
CAN

DSC56F80xx Series Feature Summary

	56F8011	56F8013	56F8014	56F8023	56F8025	56F8036	56F8037
Performance	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs
Temp Range (V)	-40C to 105C	-40C to 105C	-40C to 105C	-40C to 105C	-40C to 105C	-40C to 105C	-40C to 105C
Temp Range (M)		-40C to 125C					
Voltage Range	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V
Program/Data Flash	12KB	16KB	16KB	32KB	32KB	64KB	64KB
Program/Data RAM	2KB	4KB	4KB	4KB	4KB	8KB	8KB
On Chip Relaxation Osc.	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PLL	Yes	Yes	Yes	Yes	Yes	Yes	Yes
COP	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PWM	1 x 6ch	1 x 6ch	1 x 5ch	1 x 6ch	1 x 6ch	1 x 6ch	1 x 6ch
PWM Fault Inputs	4	4	3	4	4	4	4
12-bit ADCs	2 x 3ch	2 x 3ch	2 x 4ch	2 x 3ch	2 x 4ch	2 x 4ch	2 x 8ch
12-bit DACs				2 (Internal)	2 (Internal)	2 (Internal)	2 (External)
Analog Comparator				2	2	2	2
16-bit Timers	4	4	4	4	4	4	8
Prog. Interval Timers				1	3	3	3
GPIO (max)	26	26	26	26	35	39	53
IIC	1	1	1	1	1	1	1
SCI (UART) / LIN Slave	1 - SCI	1 - SCI	1 - SCI	1 - QSCI	1 - QSCI	1 - QSCI	2 - QSCI
SPI (Synchronous)	1 - SPI	1 - SPI	1 - SPI	1 - QSPI	1 - QSPI	1 - QSPI	2 - QSPI
CAN						MSCAN	MSCAN
JTAG/EOnCE	JTAG/EOnCE	JTAG/EOnCE	JTAG/EOnCE	JTAG/EOnCE	JTAG/EOnCE	JTAG/EOnCE	JTAG/EOnCE
Package (V) - Industrial **Package (M) - Automotive**	32LQFP	32LQFP 32LQFP	32LQFP	32LQFP (.8p)	44QFP (.8p)	48LQFP (.5p)	64LQFP (.5p)

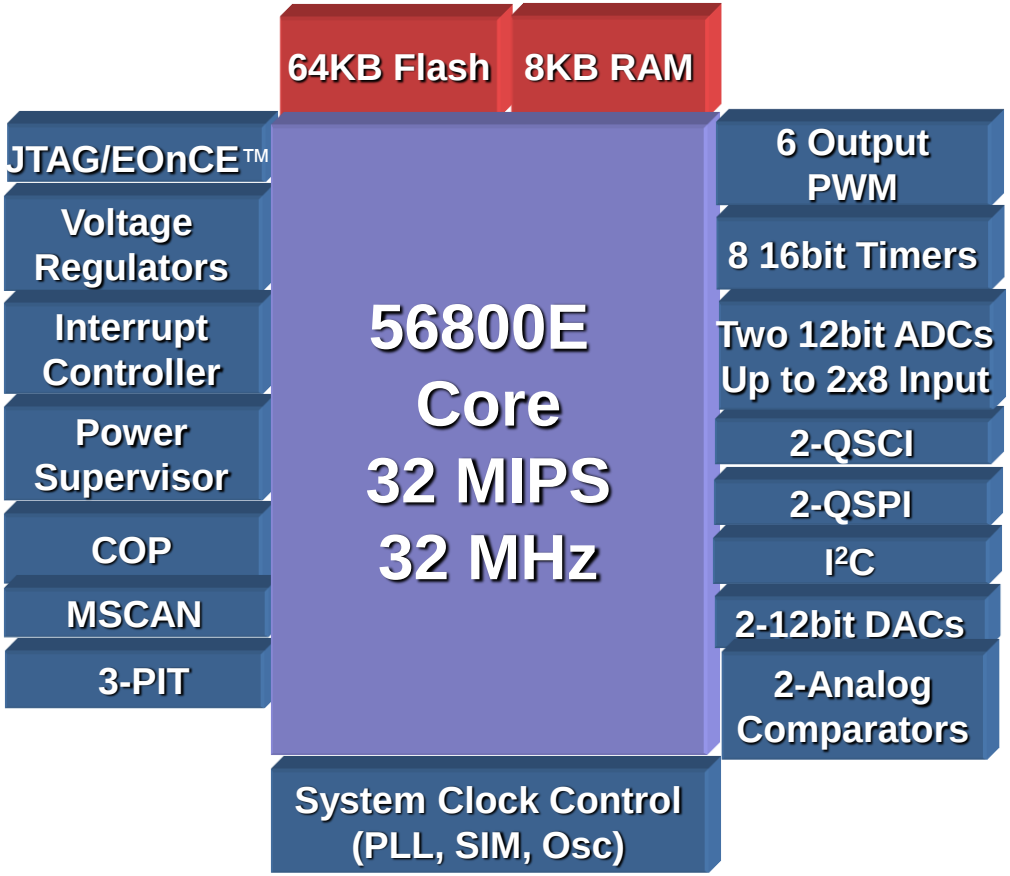
DSC Roadmap


Low Power
Low Cost
Large Capacity
Mid Range
High Performance
Flas
Size
<560kB
<280kB
<144kB
<64kB
<32kB
<16kB
MC56F816x
40MHz
MC56F836x
60MHz
MC56F815x
40MHz
MC56F835x
60MHz
32 Bit Core,
100MHz, DMA,
FAST ADC &
PWM
MC56F814x
40MHz
MC56F833x
60MHz
MC56F834x
60MHz
MC56F803x
32MHz, HR PWM,
CAN, ADC, DAC
MC56F832x
60MHz
60MHz
Accurate PWM
FAST ADC
Pin Compatible
MC56F802x
32MHz, HR PWM,
ADC, DAC
40MHz
Ultra Low Cost
MC56F812x
40MHz
Pin Compatible
MC56F801x
32MHz,
HR PWM,
ADC
56F800x
V. Low Cost, HR PWM
40MHz
Ultra Low Cost
2009

DSCs - 56F802x/3x

56F8023/56F8025/56F8036/56F8037

Features



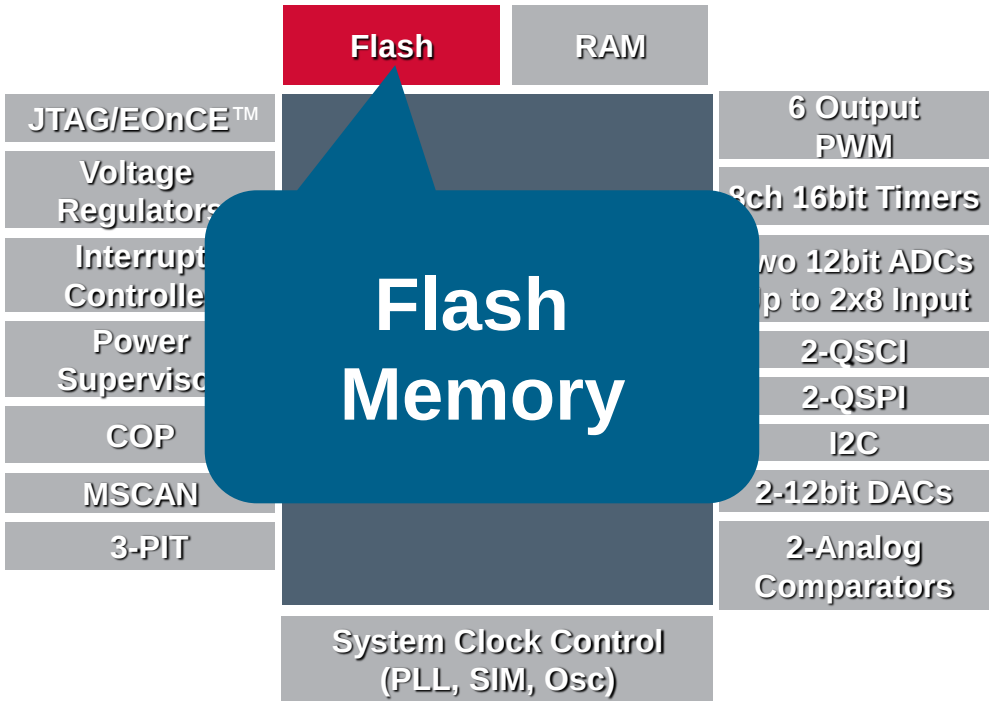
- 32 MHz/32 MIPS 56800E Core
- 3.0-3.6V Operation
- 32K-64K Bytes Program FLASH
- 4K-8K Bytes Program/Data RAM
- Flash security
- Tunable Internal Relaxation Oscillator
- Software Programmable Phase Locked Loop
- Up to 96 MHz Peripherals – Timers and PWMs
- 6 Output PWM Module with 4 Programmable Fault Inputs
- 2-12-bit ADCs for 6-8 Inputs w/ Internal or External Vref
- **Up to 2 12-bit Digital to Analog Converters**
- **2 - Analog Comparators**
- Synchronization between PWM and ADC
- 4 or 8 16-bit General Purpose Programmable Timers
- **1 or 3 Programmable Interval Timers**
- Computer Operating Properly Timer
- **2-Queued Serial Communications Interface**
- **2-Queued Serial Peripheral Interface**
- Optional MSCAN
- I2C Communications Interface
- Up to 53 GPIOs
- JTAG/EOnCE™ Debug Port
- Lead Free “Green” Packages
- Industrial & Automotive temp

•Package: 32 LQFP, 44QFP, 48LQFP, 64LQFP

•4 Derivatives

• MC56F8023/56F8025/56F8036/56F8037

- **Flash Memory**
- **Pulse Width Modulation**
- **Quad Timer**
- **Analog to Digital Converter**
- **Digital to Analog Converter**
- **Analog Comparator**
- **PIT Timer**
- **MSCAN Module**
- **QSCI Module**
- **QSPI Module**
- **I2C Module**
- **Power Supervisor**
- **General Purpose I/O (GPIO)**
- **COP and Power Supervisor**
- **PLL and Clock Generation Module**
- **Interrupt Controller (ITCN)**
- **Debugging Unit**



Flash Memory

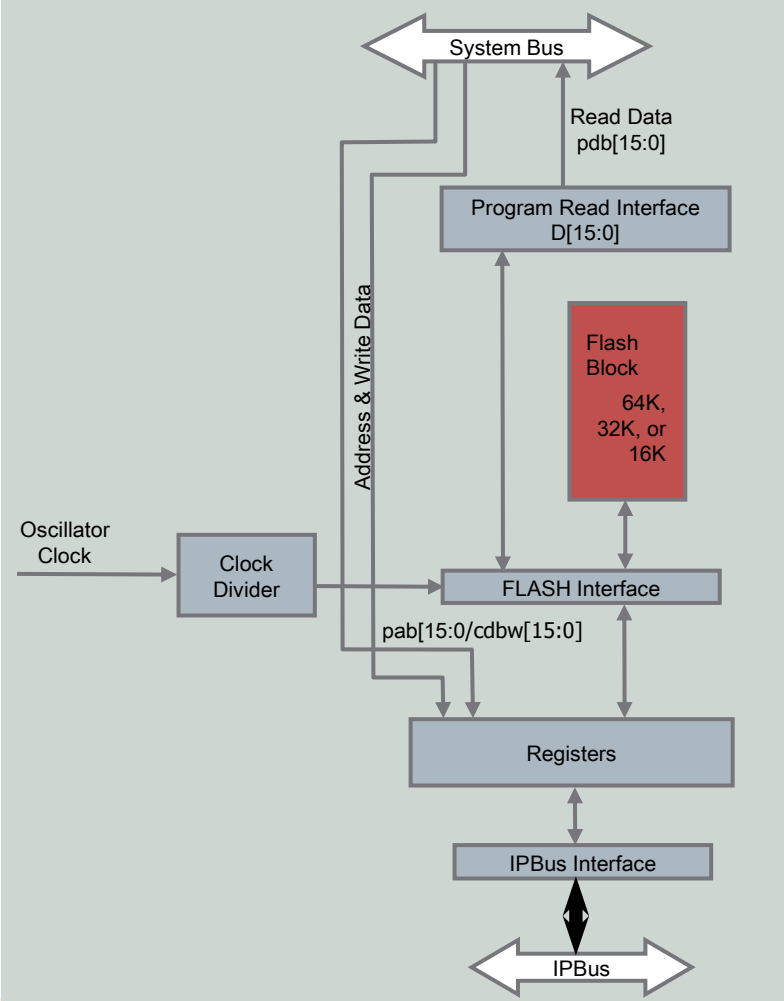
- Memory Options

	56F8023	56F8025	56F8026	56F8036	56F8037
Program/Data Flash	32KB	32KB	32KB	64KB	64KB
Program/Data RAM	4KB	4KB	4KB	8KB	8KB
Protected Sectors	16				
Sector Size [kB]	2KB	2KB	2KB	4KB	4KB

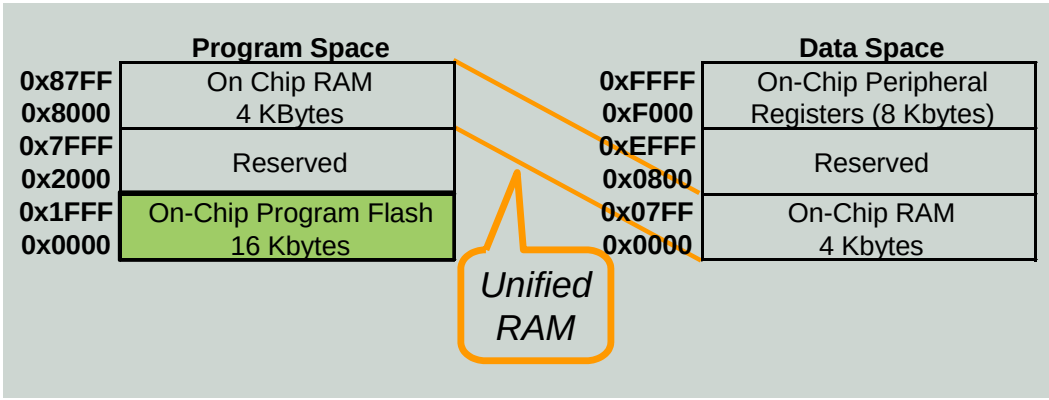
- Up to 64K Bytes Flash memory
- Up to 8K Bytes Unified RAM
- On Chip Dual Harvard Architecture
- Programmable “Code Protection” feature
- Programmable “Code Security” feature
- Flash with 256 word page size enabling EEPROM emulation (HW & SW Support)
- Can program one word at a time
- Flash memory programmable via JTAG/OnCE interface or user defined programming (such as SPI, SCI, MSCAM, I2C)
- Flash Signature Calculator
- 32MHz operation at 105°C

Memory

- Block Diagram



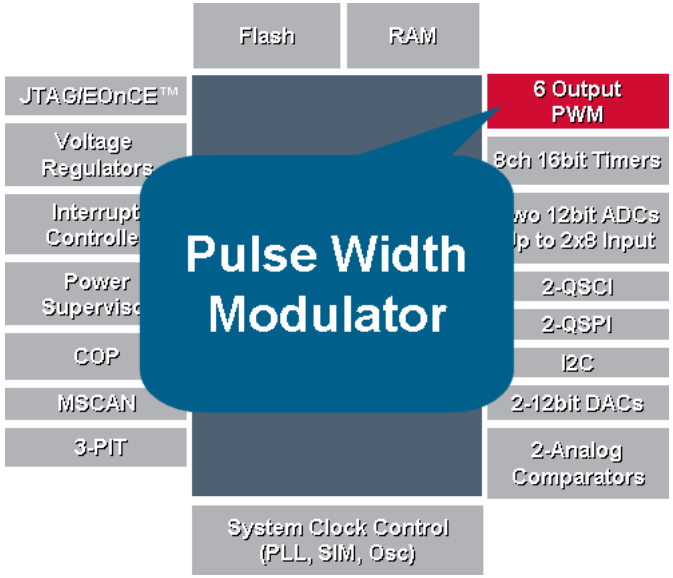
- **Program Flash: 64 Kbytes / 32 KWords**
- **Unified RAM: 8 Kbytes / 4 KWords**
- **RAM shared between Program Space (starting at 0x8000) and Data Space (starting at 0x0000)**
- **Flash Features**
  - ***16 Protectable Sectors***
  - ***256 Word Pages***
  - ***10,000 Erase/Write cycles***
  - ***15 Years Retention***



EEPROM EMULATION POSSIBILITY

• MC56F8023/56F8025/56F8036/56F8037

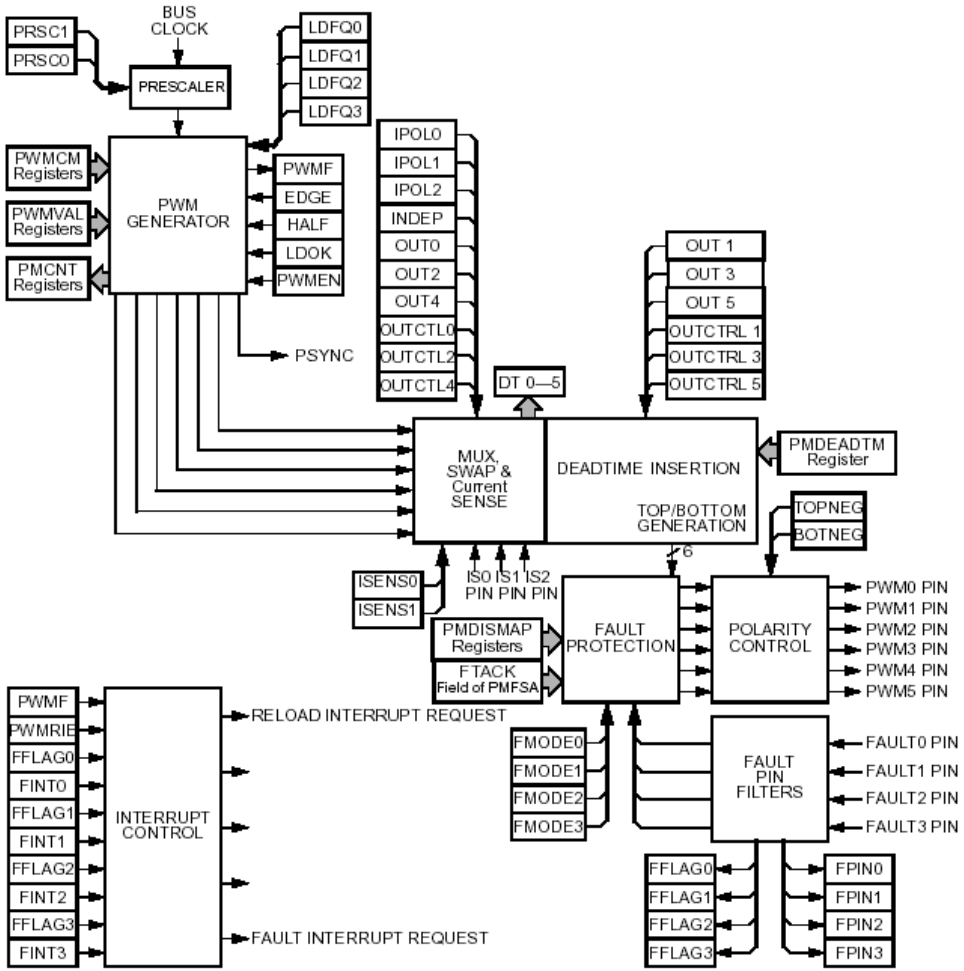
- Flash Memory
- Pulse Width Modulator
- Quad Timer
- Analog to Digital Converter
- Digital to Analog Converter
- Analog Comparator
- PIT Timer
- MSCAN Module
- QSCI Module
- QSPI Module
- I2C Module
- Power Supervisor
- General Purpose I/O (GPIO)
- COP and Power Supervisor
- PLL and Clock Generation Module
- Interrupt Controller (ITCN)
- Debugging Unit



DSC56F80xx Pulse Width Modulator

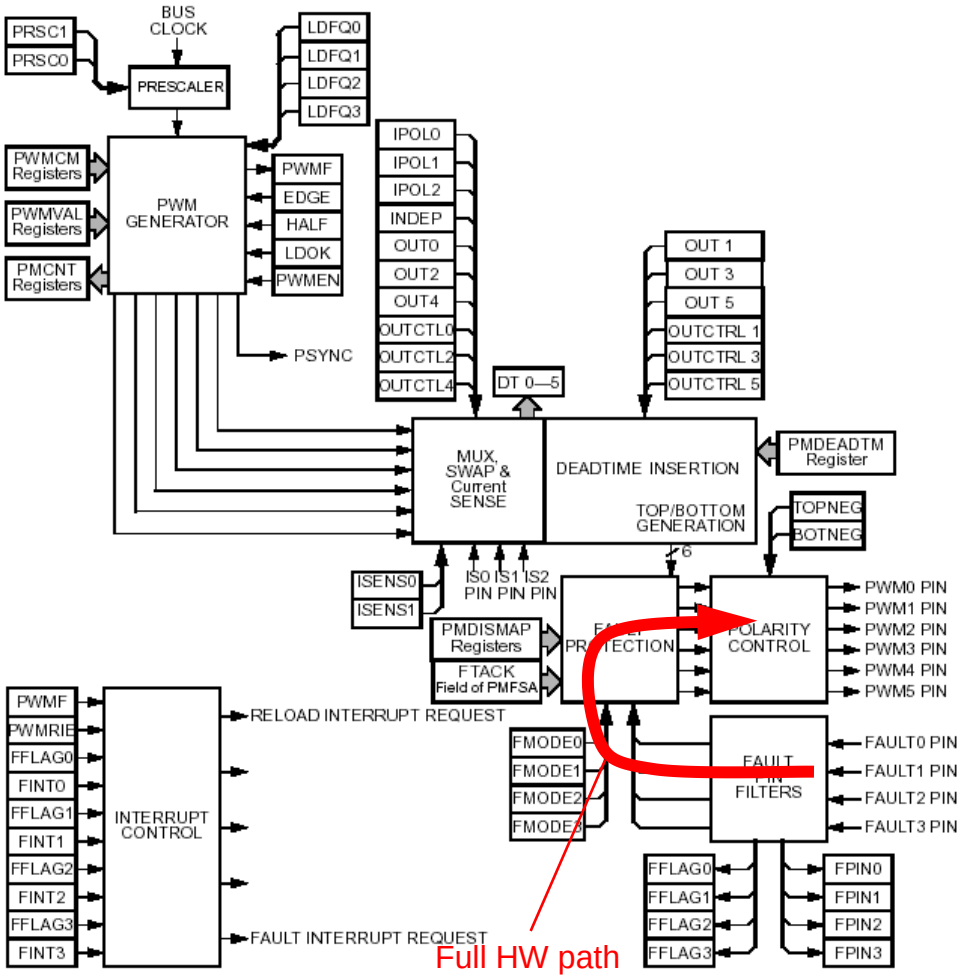
- **Up to 96 MHz operation**
- Six PWM signals
  - All independent
  - Complementary pairs
  - Mix independent and complementary
- Features of complementary channel operation
  - **Independent top and bottom deadtime insertion**
  - Separate top and bottom pulse width correction via current status inputs or software
  - Separate top and bottom polarity control
  - **Can be controlled from internal PWM generator, software, external digital pins, timers or results of ADC**
- Edge- or Center-Aligned PWM signals
- Asymmetric PWM outputs
- 15-bits of resolution
- Half-cycle reload capability
- Integral reload rates from 1/2 to 16
- Individual software controlled PWM output
- Programmable fault protection
- Write protected registers
  - Protection for key parameters

DSC56F80xx Pulse Width Modulator



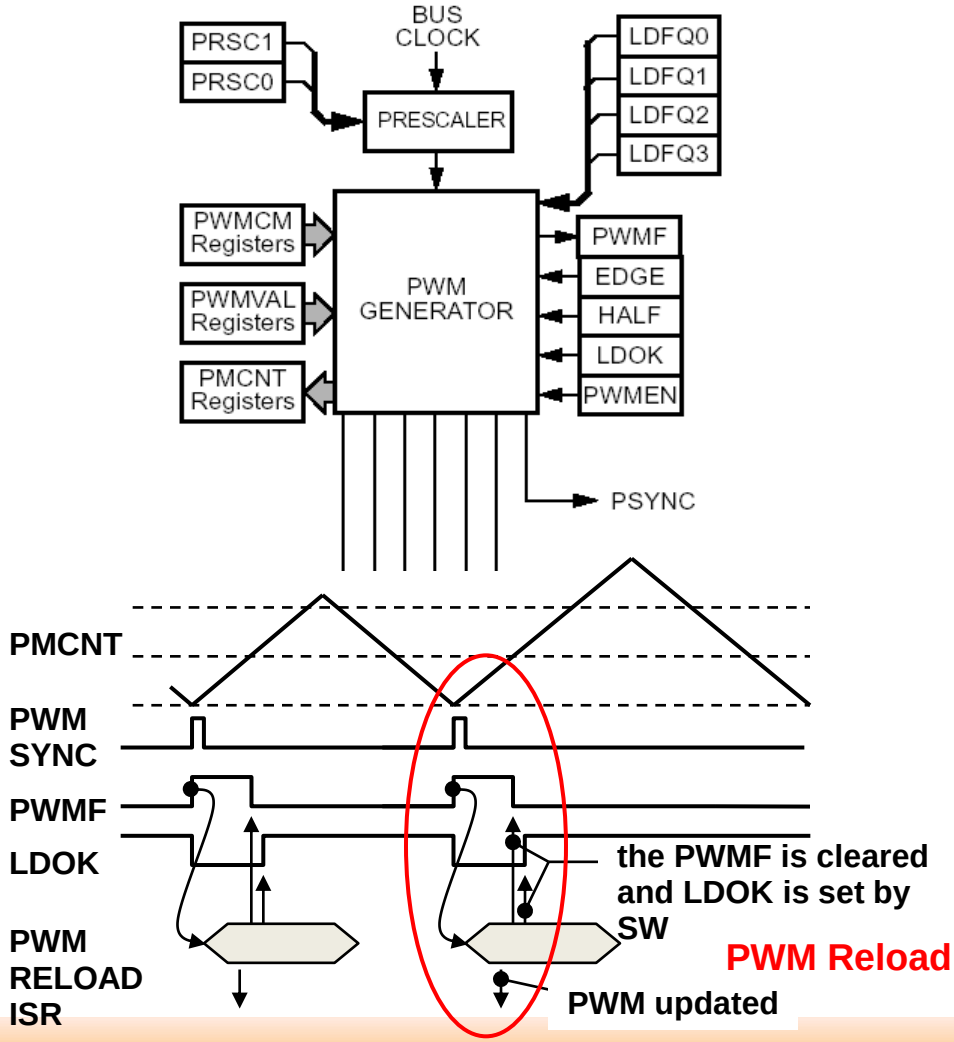
- **Safety** - Write protected registers
- Prescaler
- PWM Generator
- MUX Swap & Current sense
- Deadtime Insertion Top/Bottom Generation
- Software Output Control
- Fault Protection
- Fault Pin Filters
- Polarity Control
- Interrupt Control

PWM - Safety



- **Safety critical setting can be protected** by the write-protect bit (WP).
  Once set **it prevents** any further **writes to write-protected registers or bits**.
  Protection can be cleared only by RESET !
- The list of write-protected registers (their bits) and functions:
  - **PWM polarity**
  - **Complementary PWM pair operation**
  - **Centre aligned PWM channels**
  - **Deadtime value**
  - **PWM fault disable mapping matrix**
  - **HW acceleration features**
  - **PWM generator channels swapping**
  - **Enable PWM in Debug or Wait mode bits**
  - **56F80x Compatibility bit**
- The functions which are still available:
  - PWM Value setting, PWM Frequency setting
  - PWM Clock Prescaller setting
  - PWM Re-load Frequency + Half Cycle reload
  - Deadtime Correction Method setting, odd/even PWMVALx selection for Deadtime Correction
  - Fault Interrupts Enable/Disable, Fault Clearing Mode selection, Fault acknowledging
  - PWM Pins SW Output Control
  - PWM channels masking.
- **At fault the PWM's are forced to INACTIVE state ! It is faster than tri-stating PWM's.**

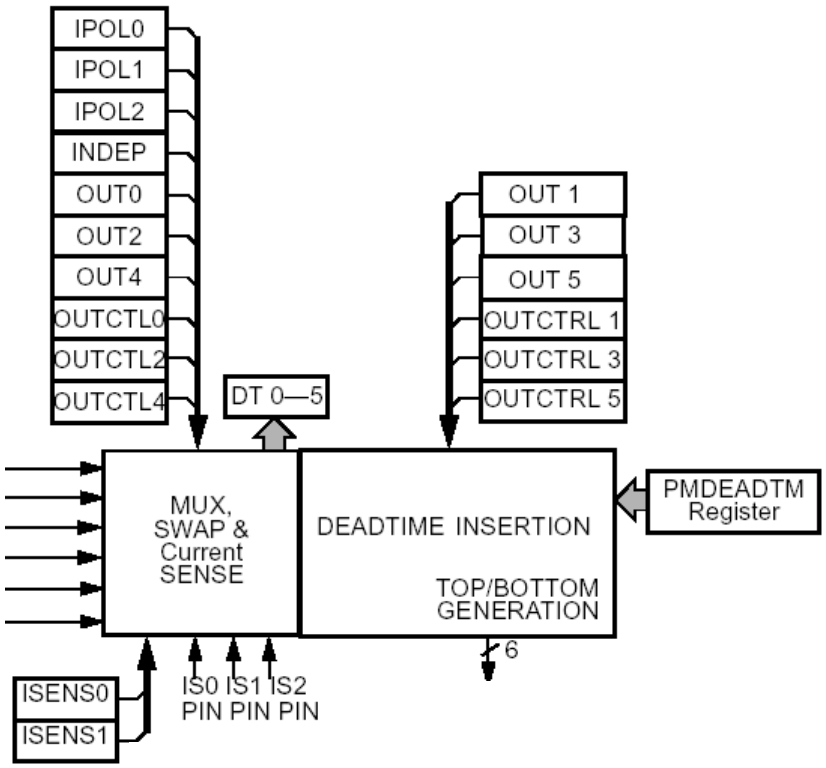
PWM - 6xPWM Generator



- **Prescaler** - 1, 2, 4, 8
- **PWM Generator**
  - **Contains up/down counter counts**
    - 15 bit resolution
    - up to 96 MHz max → 10.417 nsec resolution
  - **Alignment** - edge/centre-aligned
  - **Period** - set by PWM Counter Modulus
  - **Pulse Widths** - defined by PWM Value Registers
    Resolution:
    - 12.2bit @ 20 kHz PWM(edge-aligned)
    - 11.2bit @ 20 kHz PWM(centre-aligned)
  - **Reload Frequency** - half to 16 cycles
  - **Load Enable** interlock bit - prevents reloading of the PWM parameters before software is finished calculating them - **coherent update**
  - **Synchronization output** - high-true pulse occurs for each PWM reload
  - **HW Acceleration** - enables multi-write access of the PWM Value Registers

PWM Reload Interlock Mechanism for Coherent PWM Update

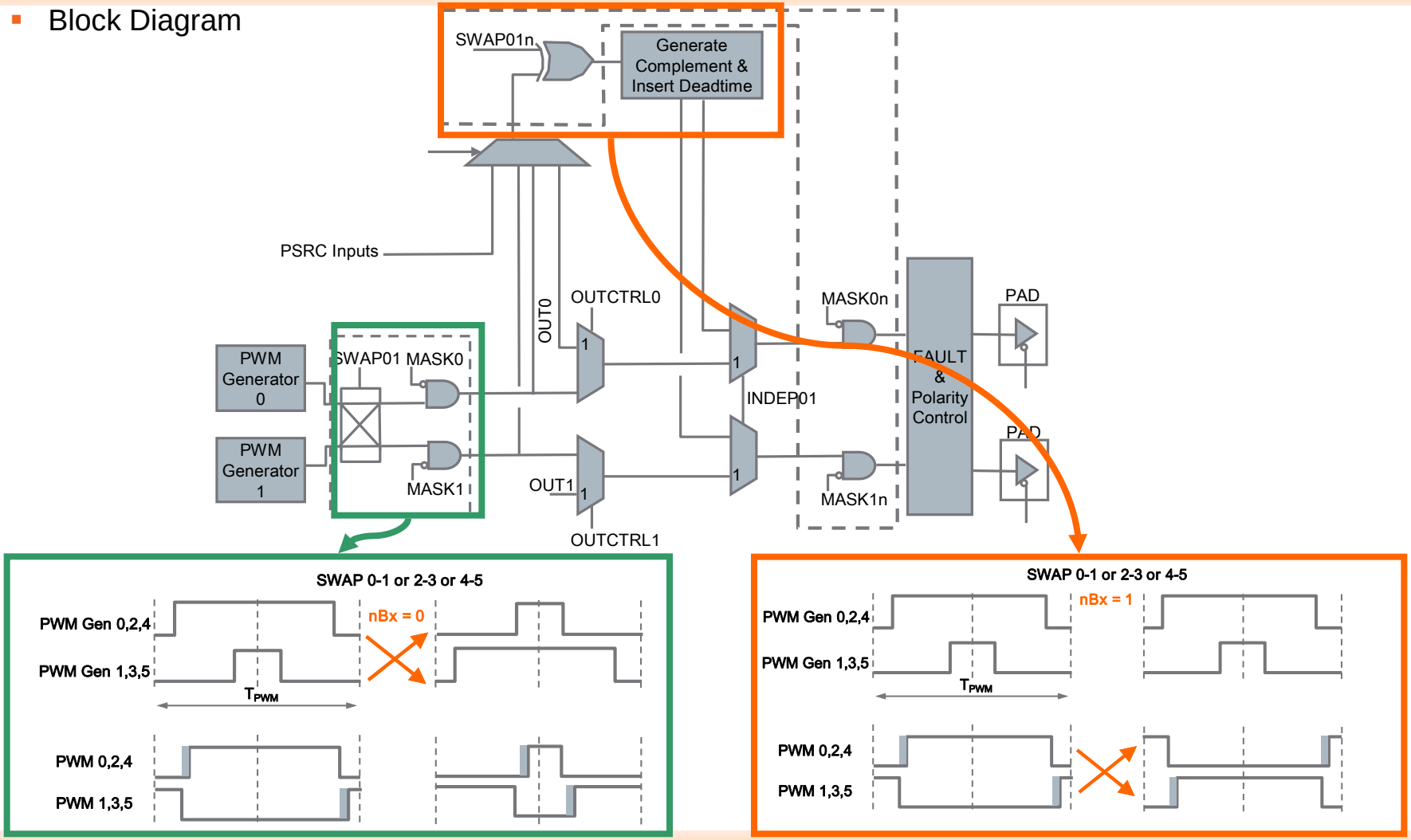
PWM - MUX, SWAP, MASK, Deadtime, SW OUT CTRL



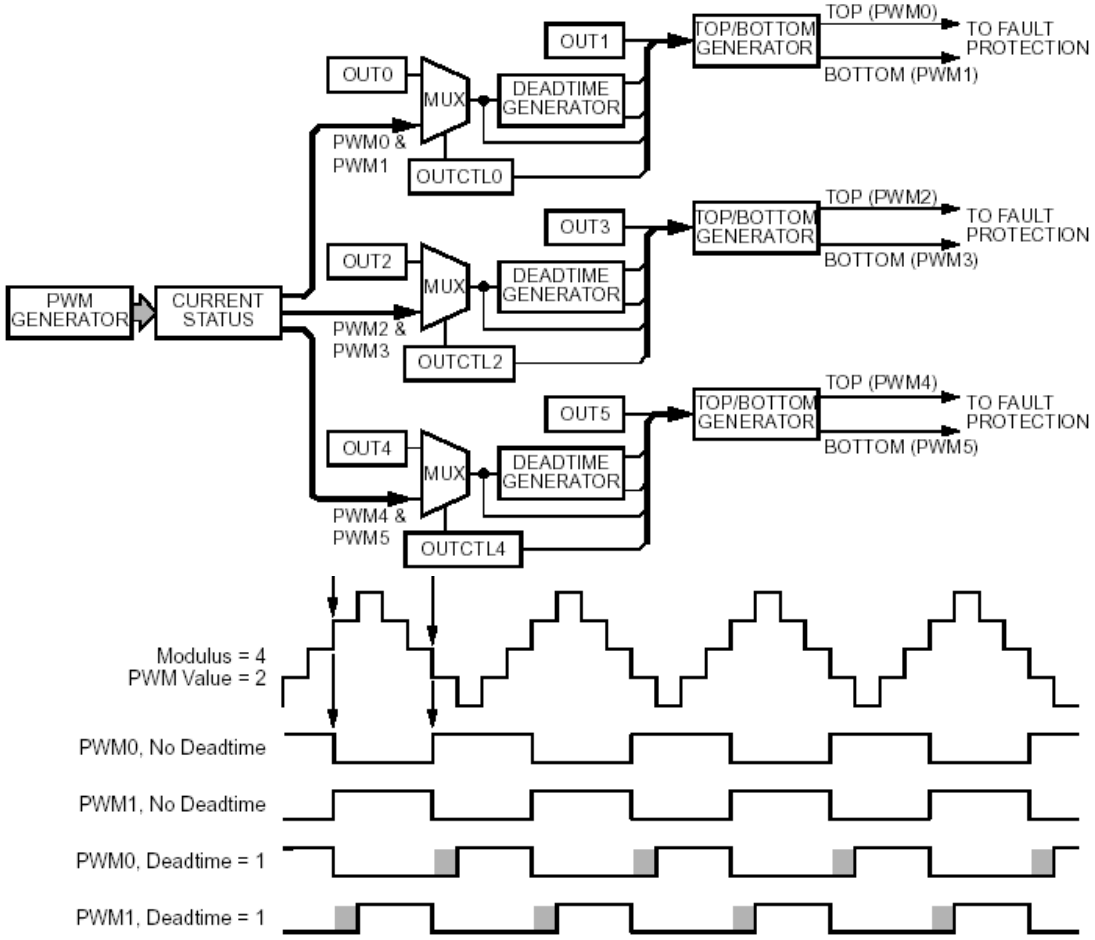
- **MUX Swap & Current sense**
  - **Channel Mask & Swap** - individually swaps and masks PWM generator channels
  - **MUX & Current Sense** - enables SW Output Control and Dead time correction
  - **SW Output Control** - individually controls the PWM outputs with respect to deadtime and complementary operation settings
- **Deadtime Insertion & Top/Bottom Generation**
  - Deadtime generators automatically insert software-selectable “deadtimes” into each pair of PWM outputs
  - The Pulse Module Deadtime register specifies the number of PWM clock cycles to use for deadtime delay
  - Every time the deadtime generator inputs changes state, deadtime is inserted
- **Software Output Control**
  - In an independent mode the output bit OUTx controls the PWMx channel.
  - In a complementary channel operation the OUT0/2/4 bits control the top/bottom pair.

PWM – Mux and Swap Options

- Block Diagram



PWM - Deadtime Generators

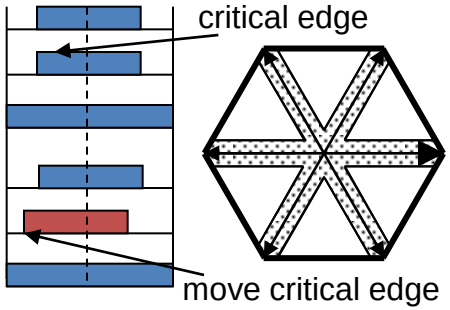


Deadtime Insertion in Centre-aligned Mode

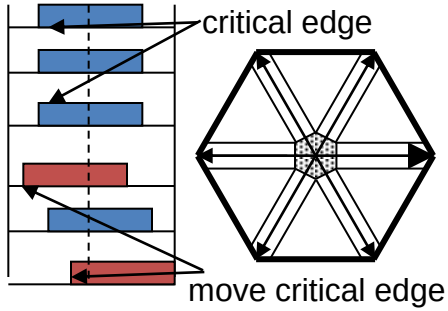
- **Deadtime Generators**
  - Deadtime generators automatically insert software-selectable “deadtimes” into each pair of PWM outputs
  - Every time the deadtime generator inputs changes state, deadtime is inserted
  - In Software Output Control
    - Deadtime generators continue to insert deadtime whenever an OUT0/2/4 bit toggles.
    - Deadtime is not inserted when the OUT1/3/5 bit toggles.
  - The Pulse Module Deadtime register specifies the number of PWM clock cycles to use for deadtime delay

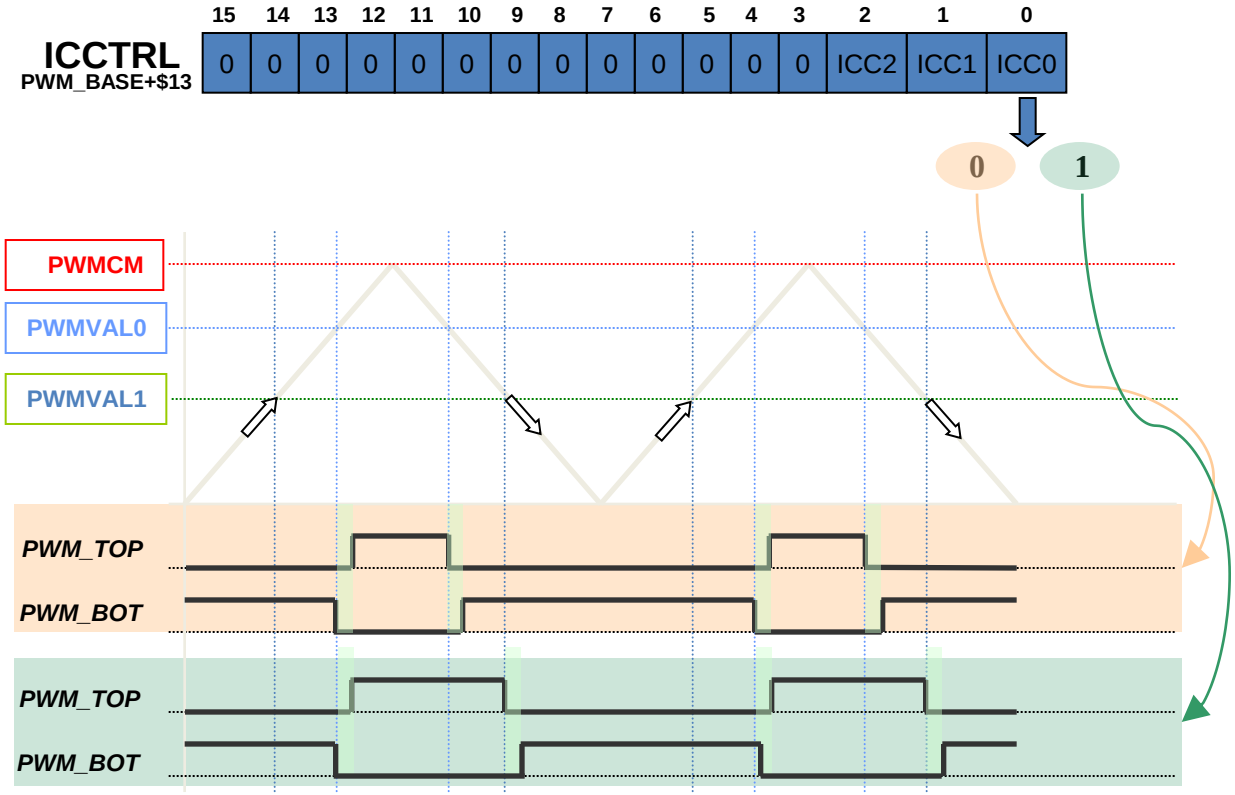
PWM – Asymmetrical Generation

- Passing active vector



- Low modulation index



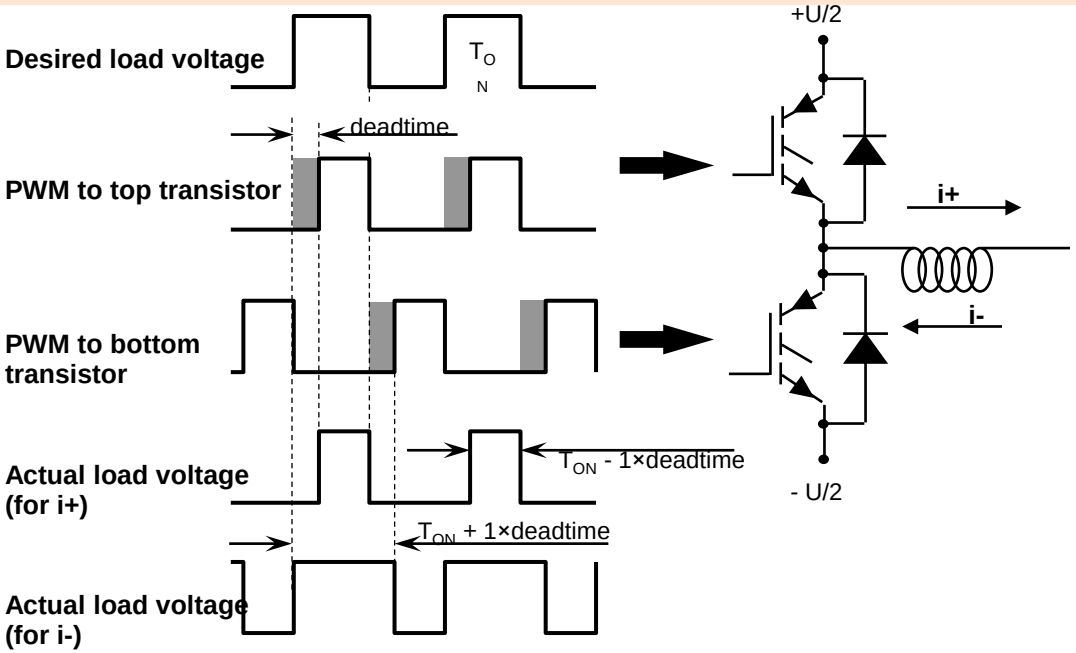


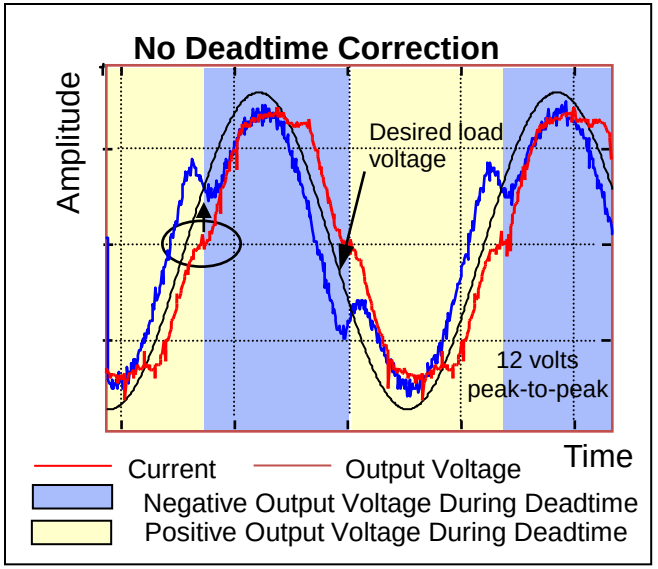
PWM - SW Output Control - Details

OUTx bit	Complementary channel operation	Independent channel operation
OUT0	1—PWM0 is active + deadtime insertion 0—PWM0 is inactive	1—PWM0 is active 0—PWM0 is inactive
OUT1	1—PWM1 is complement of PWM 0 0—PWM1 is inactive	1—PWM1 is active 0—PWM1 is inactive
OUT2	1—PWM2 is active + deadtime insertion 0—PWM2 is inactive	1—PWM2 is active 0—PWM2 is inactive
OUT3	1—PWM3 is complement of PWM 2 0—PWM3 is inactive	1—PWM3 is active 0—PWM3 is inactive
OUT4	1—PWM4 is active + deadtime insertion 0—PWM4 is inactive	1—PWM4 is active 0—PWM4 is inactive
OUT5	1—PWM5is complement of PWM 4 0—PWM5 is inactive	1—PWM5 is active 0—PWM5 is inactive

- ✓ **Complementary channel pairs still cannot be active simultaneously !**
  The OUT0/2/4 replace the PWM generator outputs as inputs to the deadtime generators.
  Deadtime generators continue to insert deadtime whenever an OUT0/2/4 bit toggles.
  Deadtime is not inserted when the OUT1/3/5 bit toggles.
- ✓ **Setting the OUTCTLx bits does not disable the PWM generators and current status sensing circuitry!**
  They continue to run, but no longer control the output pins.
  When the OUTCTLx bits are cleared, the outputs of the PWM generator become the inputs to the deadtime generators at the **beginning of the next PWM cycle**.
- ✓ **Software can drive the PWM outputs even when PWM enable bit (PWMEN) is set to zero.**
- ✓ **During software output control, TOPNEG and BOTNEG still control output polarity !**

PWM - Distortion Caused by Inductive Loads



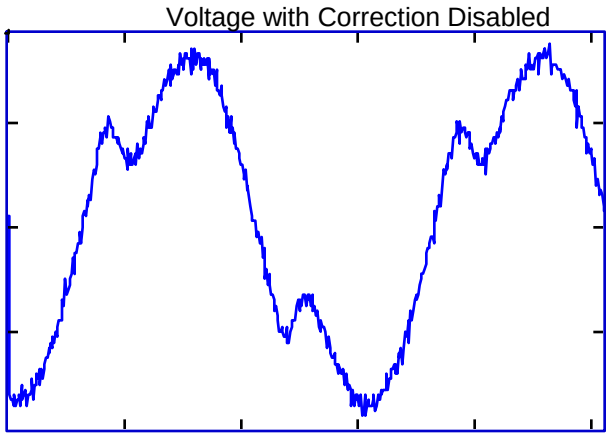


- ✓ Both transistors are "off" during deadtime. **Load inductance** keeps current flowing through the diodes and thus **defines an output voltage**.
- ✓ **Positive current flow** causes negative output voltage during deadtime – **top transistor controls output voltage.**
- ✓ **Negative current flow** causes positive output voltage during deadtime – **bottom transistor controls output voltage.**

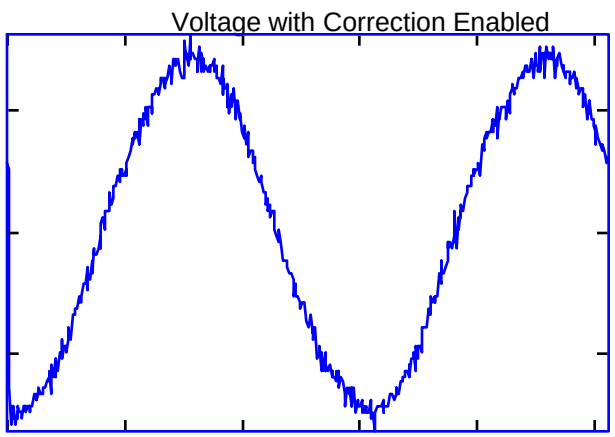
- ✓ **Causes poor low-speed motor performance**
- ✓ **Torque ripple**
- ✓ **Distorts current**
- ✓ **Produces noise in audible region**

PWM - Patented PWM Distortion Correction

Actual waveforms taken on a 1/2 horsepower motor



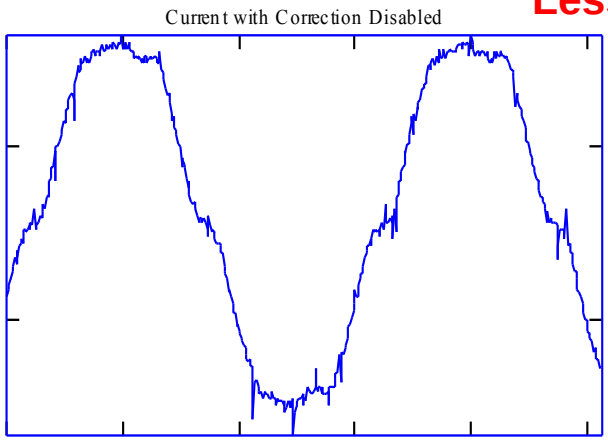
Motor Voltage



Before

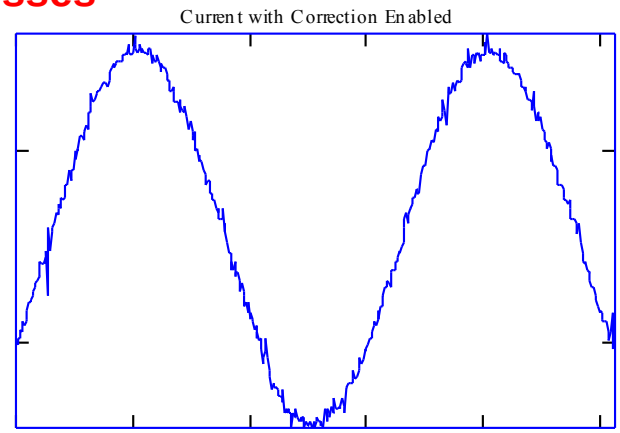
Quieter operation
Smoother operation
Less motor harmonic losses

After



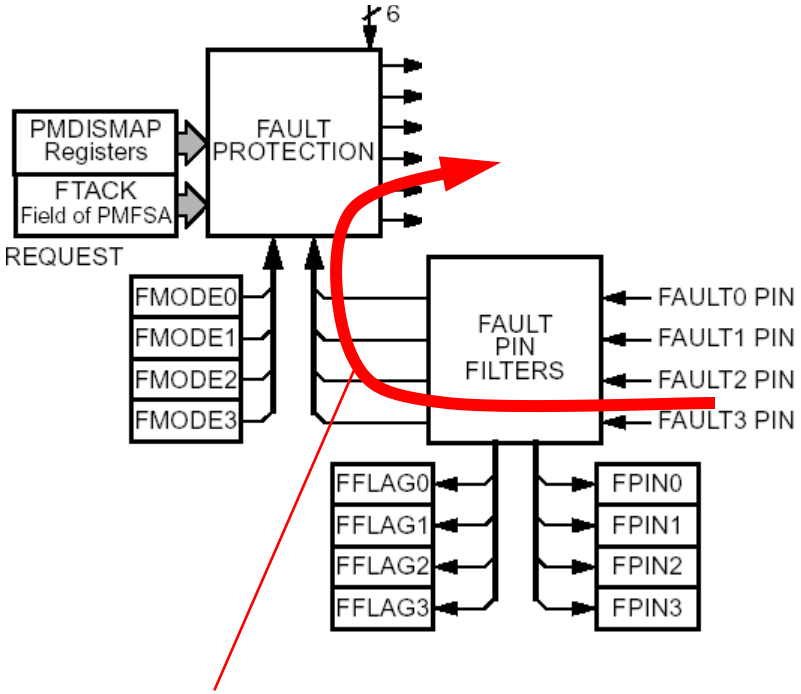
Motor Current

1/2 horse 3 phase motor
PWM Frequency = 7.3 KHz
Dead Time = 3 uS
Output ω = 1.7 Hz.



More details in dedicated presentation

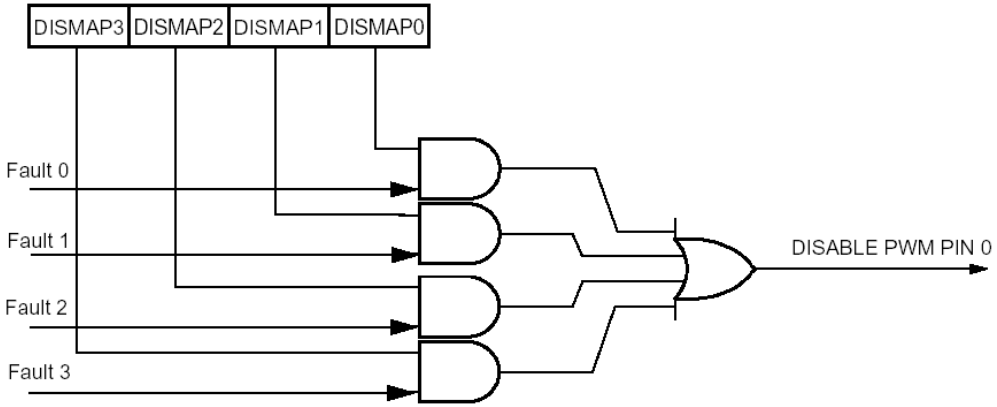
PWM - Fault Protection



Full HW path

- **Fault Protection**
  - **Fault protection can automatically disable any combination of PWM pins !**
  - Faults are generated by a logic 1 on any of the FAULT pins.
  - **When fault occurs, only the output pins are deactivated - the PWM generator continues to run !**
  - **The fault protection is enabled even when the PWM is not enabled**. Service faults before PWM enable.
  - **Automatic Fault Clearing -** the disabled PWM pins are enabled when the FAULTx pin returns to logic 0 and a new PWM half cycle begins.
  - **Manual Fault Clearing**
    - FAULT0/2 - the disabled PWM pins are enabled when software clears the FFLAGx flag + next PWM half cycle begins regardless of the logic level detected by the filter at the fault pin.
    - FAULT1/3 - the disabled PWM pins are enabled when software clears the FFLAGx flag + the filter detects a logic zero on the fault pin at the start of the next PWM half cycle.
- **Fault Pin Filters**
  - After every IPBus cycle setting the FAULTx pin at logic 0, the filter synchronously samples the pin once in each of the next two cycles. If both samples are logic 1s, the corresponding fault bits (FAULTx, FPINx, FAULTx, FFLAGx) are set.
  - The FPINx bit remains set until the pin returns to logic 0 and the filter samples a logic 0 synchronously once in the following IPbus cycle.

PWM - Fault Pins Mapping



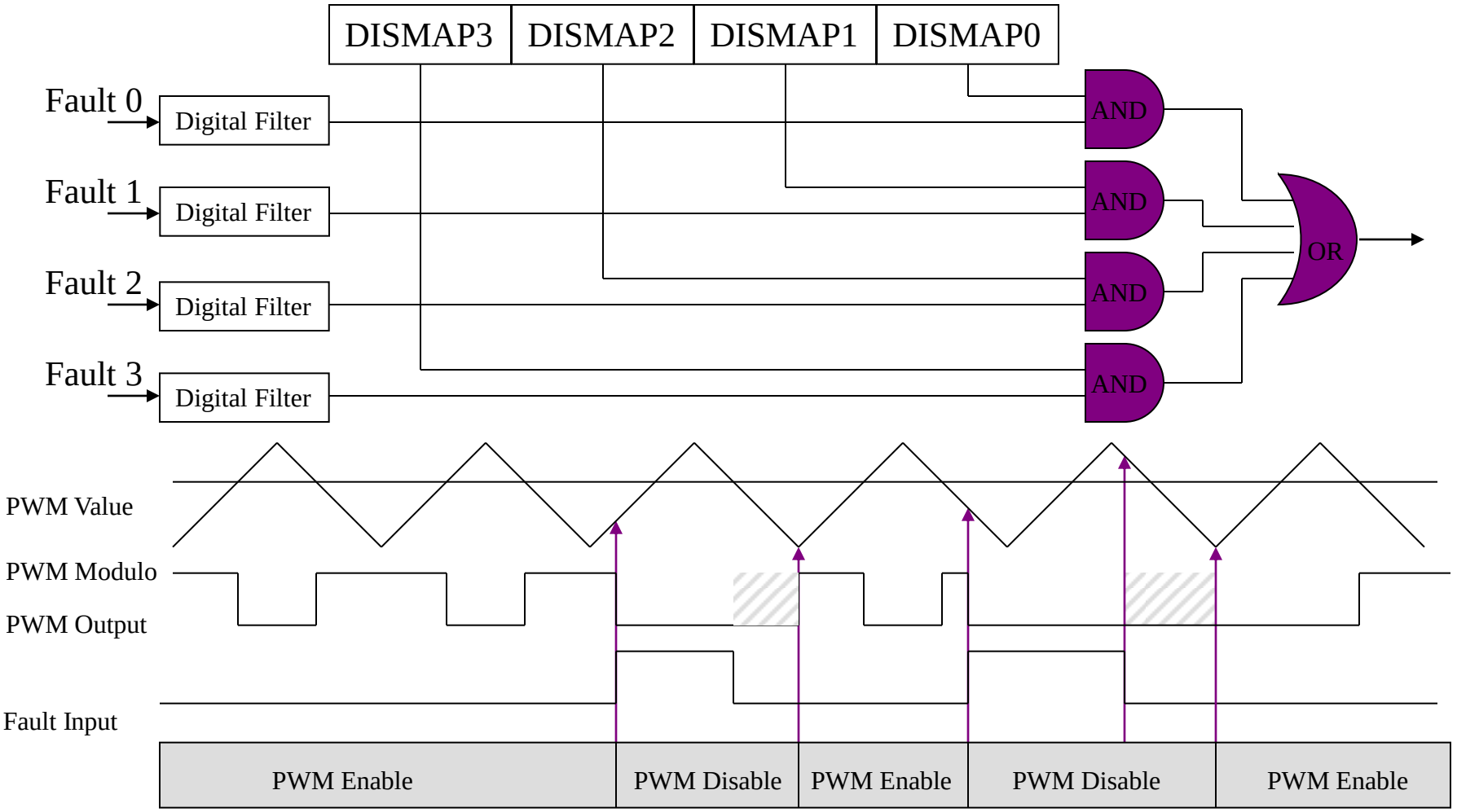
- ✓ **FAULT Pins Mapping**
  - ✓ The fault decoder disables PWM pins pre-selected by the disable mapping register.
    Each FAULT pin can be mapped arbitrarily to any of the PWM pins.
  - ✓ Each bank of four bits in the disable mapping register control the mapping for a single PWM pin.

PWM Pin to be disabled	Fault0	Fault1	Fault2	Fault3	PWM Disable Mapping Register
	to assign Fault and PWM pin set **DISMAP bit #**				
PWM0	0	1	2	3	PMDISMAP1 [0:3]
PWM1	4	5	6	7	PMDISMAP1 [4:7]
PWM2	8	9	10	11	PMDISMAP1 [8:11]
PWM3	12	13	14	15	PMDISMAP1 [12:15]
PWM4	16	17	18	19	PMDISMAP2 [0:3]
PWM5	20	21	22	23	PMDISMAP2 [4:7]

Example

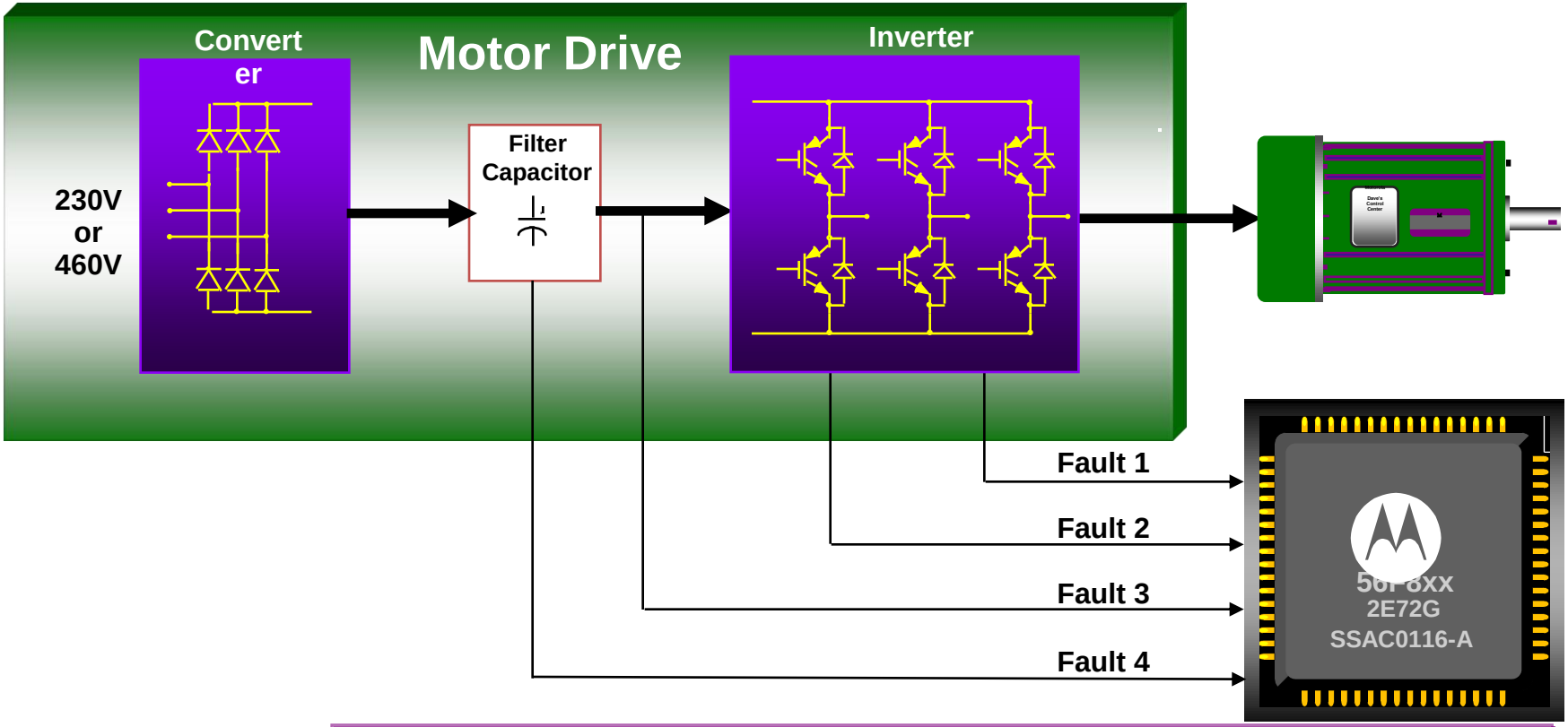
Fault Pins vs. PWM Pins Mapping

PWM Fault Decode And Automatic Clearing



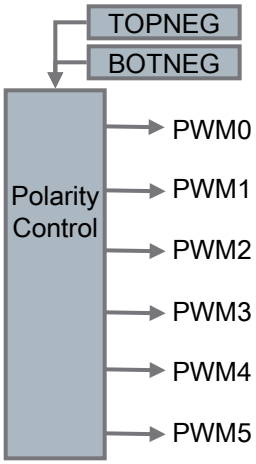
*When Fault logic returns to logic 0, the PWM restart at beginning of the next half cycle.

Multiple Fault Inputs

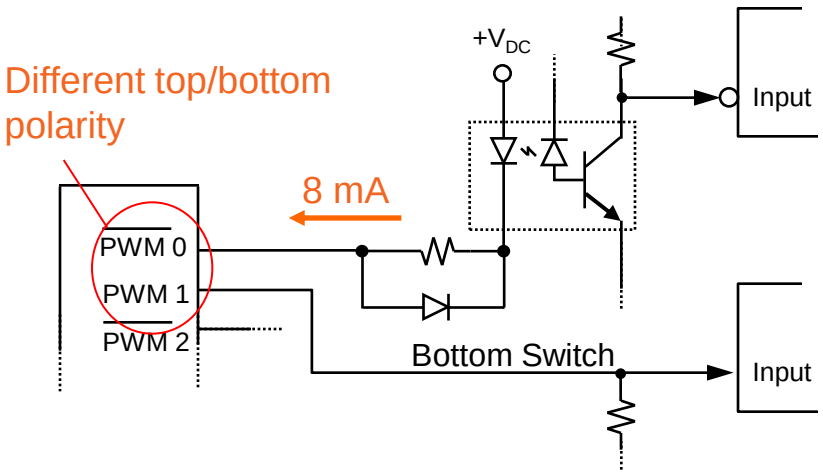


- ✓ Fault inputs can independently monitor critical system parameters, and generate an interrupt when asserted.
- ✓ Each input is mapable to immediately disable any or all PWMs
- ✓ Each input is programmable to allow Automatic or Manual PWM restart.

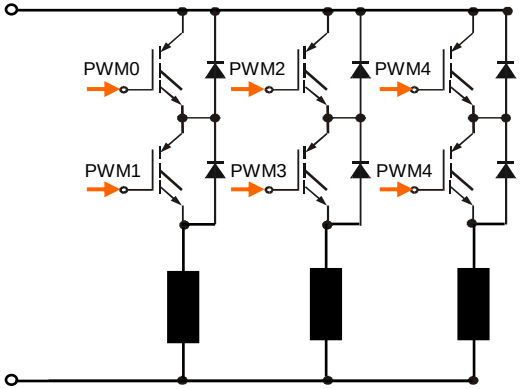
Pulse Width Modulator - Polarity Control



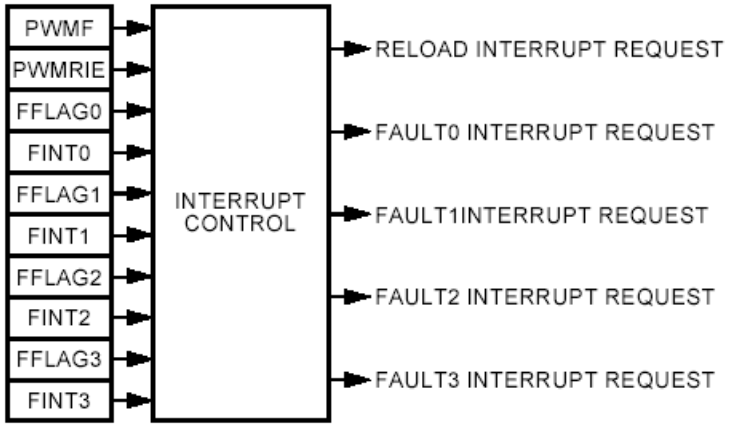
- **Polarity Control**
  - ***Positive polarity** means when the PWM is active - its output is high.*
  - ***Negative polarity** means when the PWM is active - its output is low.*
  - ***Separate control of top and bottom PWM outputs.***
    ***TOPNEG** - controls PWM0/2/4 polarity.*
    ***BOTNEG** - controls PWM1/3/5 polarity.*
- **High Current Capability**
- **8 mA current sink / current source capability**



Direct PWM pin-optocoupler connection



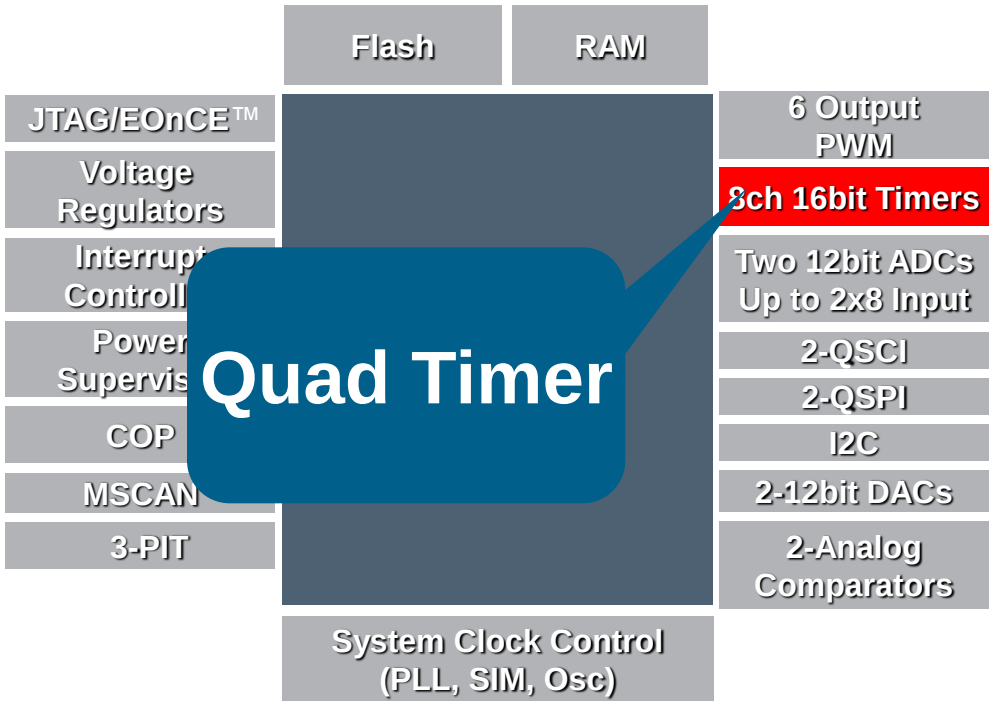
PWM - Interrupt Control



- **The PWM module can generate up to 5 interrupt requests.**
- **Reload flag (PWMF)** - PWMF is set at the beginning of every reload cycle.
  The reload interrupt enable bit (PWMRIE) enables PWMF to generate CPU interrupt requests.
- **Fault flags (FFLAG0–FFLAG3)** - The FFLAGx bit is set when fault pin filters recognises a logic 1 on the FAULTx pin.
  The fault pin interrupt enable bits (FIE0–FIE3) enable the FFLAGx flags to generate CPU interrupt requests.

• MC56F8023/56F8025/56F8036/56F8037

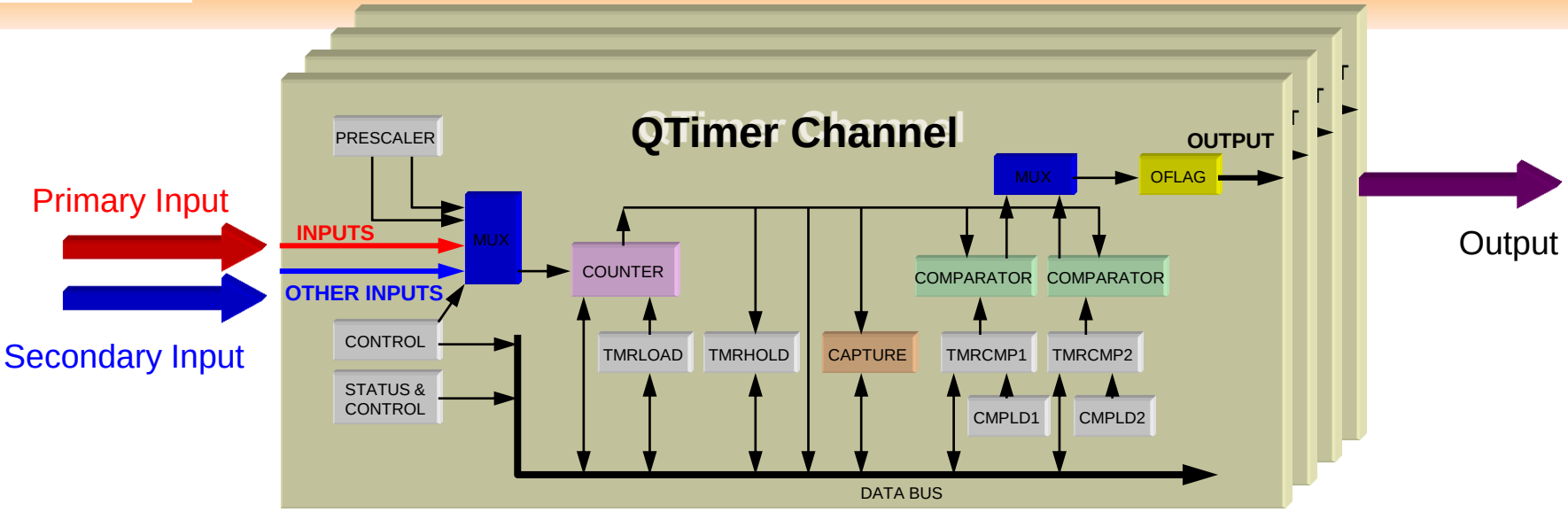
- Flash Memory
- Pulse Width Modulator
- Quad Timer
- Analog to Digital Converter
- Digital to Analog Converter
- Analog Comparator
- PIT Timer
- MSCAN Module
- QSCI Module
- QSPI Module
- I2C Module
- Power Supervisor
- General Purpose I/O (GPIO)
- COP and Power Supervisor
- PLL and Clock Generation Module
- Interrupt Controller (ITCN)
- Debugging Unit



Quad Timer Module

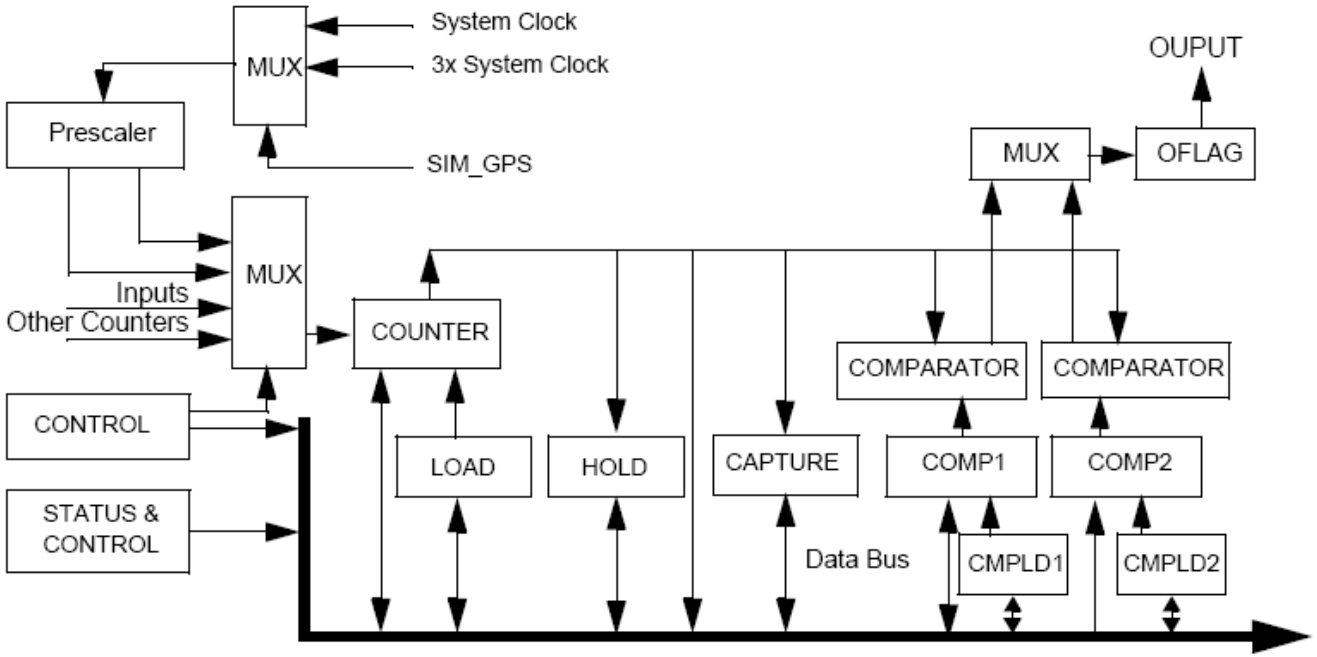
- **4x 16-bit general purpose up/down timer/counters per module**
- **Up to 96 MHz operation**
- **Individual channel capability**
  - Input capture trigger
  - Output compare
  - Clock source
  - Prescaler
- **Max. count rate**
  - external events counting - peripheral clock/2
  - internal clock counting - peripheral clock
- **Counters are pre-loadable**
- **Count once or repeatedly**
- **Programmable count modulo**
- **Input pins are fully shareable within timer module**
- **Pins available as general I/O when timer(s) not in use**
- **Counters in module can be daisy-chained to yield longer counter lengths**
- **Master operation**
  - “Broadcasts” compare function
  - channel re-initialization for coherent operation
- **Up to 12 operation Modes**

Quad Timer Module



- **Unique architecture with -** 2x Inputs (Primary + Secondary) and 1x Output
- **Powerful MUX -** Primary Input, Secondary Input and Output can be connected to ext. pins
- **Individual channel capability -** Input capture trigger, Output compare, Clock source, Prescaler
- **Counters are pre-loadable, Count once or repeatedly**
- **Master Operation** - any channel can be a master that broadcasts its compare signal to the other channels. Such way they can be configured to reinitialize their counters and/or force their OFLAG output signals to predetermined values.
- **Compare** - The TMRCMP1/2 registers provide the compare values (up/down) for the counter. If a match occurs, the OFLAG signal can be set, cleared, or toggled (polarity is selectable). If enabled, an interrupt is generated, and the new compare value is loaded into TMRCMP1 or 2 registers from TMRCMPLD1 and 2 (as enabled).
- **Capture** register stores a copy of the counter's value when an input edge (positive, negative, or both) is detected. Once a capture event occurs, no further updating of the Capture register will occur until the Input Edge Flag is cleared.

Quad Timer Module



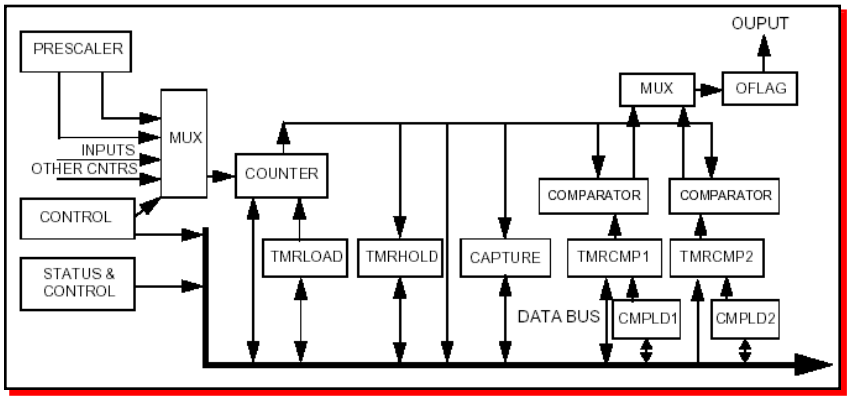
- Maximum count rate equals System Clock, or 3x System Clock for internal clocks
- Maximum count rate equals System Clock/2 for external clocks

Quad Timer Operating Modes

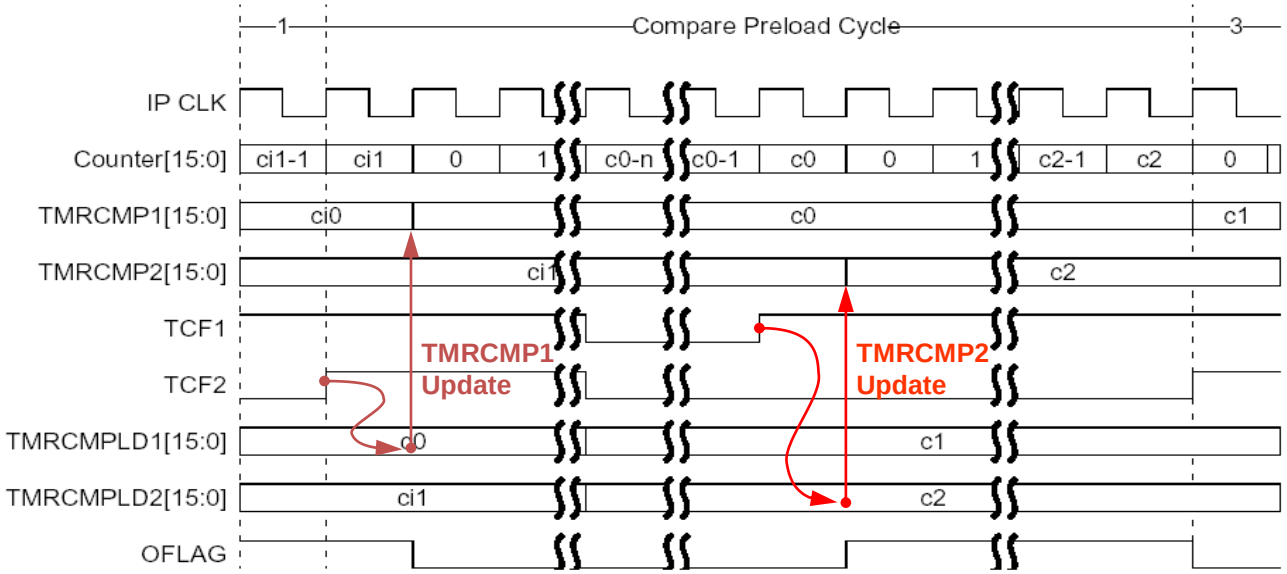
- **Stop Mode** - the counter is inert. No counting will occur, but interrupts are still possible according to input transitions on the selected input pin
- **Count Mode** - counts on rising edges (generating periodic interrupts, timing purposes)
- **Edge-Counting** - count edges (counting of simple encoder wheel)
- **Gated-Counting** - counts primary input signal if signal on secondary input is high (signal width measurement)
- **Quadrature-Counting** - counter will decode the primary and secondary external inputs as quadrature encoded signals (movement monitoring)
- **Signed-Counting** - counter increments/decrements primary clock source accordingly to level of signal asserted on secondary source
- **Triggered-Counting** - counts primary clock source if rising edge of the secondary input detected and stops counting if either rising edge or compare event occurs
- **One-Shot Mode** - provides timing delays (ADC acquisition of new samples until a specified period of time has passed since the PWM sync signal)
- **Cascade-Count Mode** - the counter's input is connected to the output of another selected counter. If any counter is read the values of other counters are captured in hold registers
- **Pulse-Output Mode** - supports stepper motor systems and provides change of signal frequency and number of pulses
- **Fixed- Freq. PWM** - fixed frequency variable duty cycle generation (driving PWM amplifiers)
- **Variable-Freq. PWM** - variable frequency and duty cycle generation (driving PWM amplifiers)

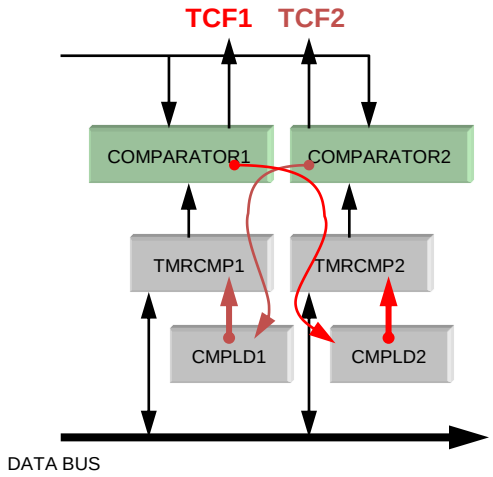
Quad Timer - Setting Modes

- **The operating modes are mainly combination of**
  - **Count Mode**
    000 = No operation
    001 = Count rising edges of primary source
    010 = Count rising and falling edges of primary source
    011 = Count rising edges of primary source while secondary input high active
    100 = Quadrature count mode, uses primary and secondary sources
    101 = Count primary source rising edges, secondary source specifies direction
    110 = Edge of secondary source triggers primary count until compare
    111 = Cascaded counter mode (up/down)
  - **Count Once setting**
    0 = Count repeatedly
    1 = Count till compare and then stop
  - **Count Length**
    0 = Roll-over
    1 = Count till compare, then re-initialized
  - **Output Mode**
    000 = Asserted while counter is active
    001 = Clear OFLAG output on successful compare
    010 = Set OFLAG output on successful compare
    011 = Toggle OFLAG output on successful compare
    100 = Toggle OFLAG output using alternating compare registers1
    101 = Set on compare, cleared on secondary source input edge
    110 = Set on compare, cleared on counter rollover
    111 = Enable Gated Clock output while counter is active



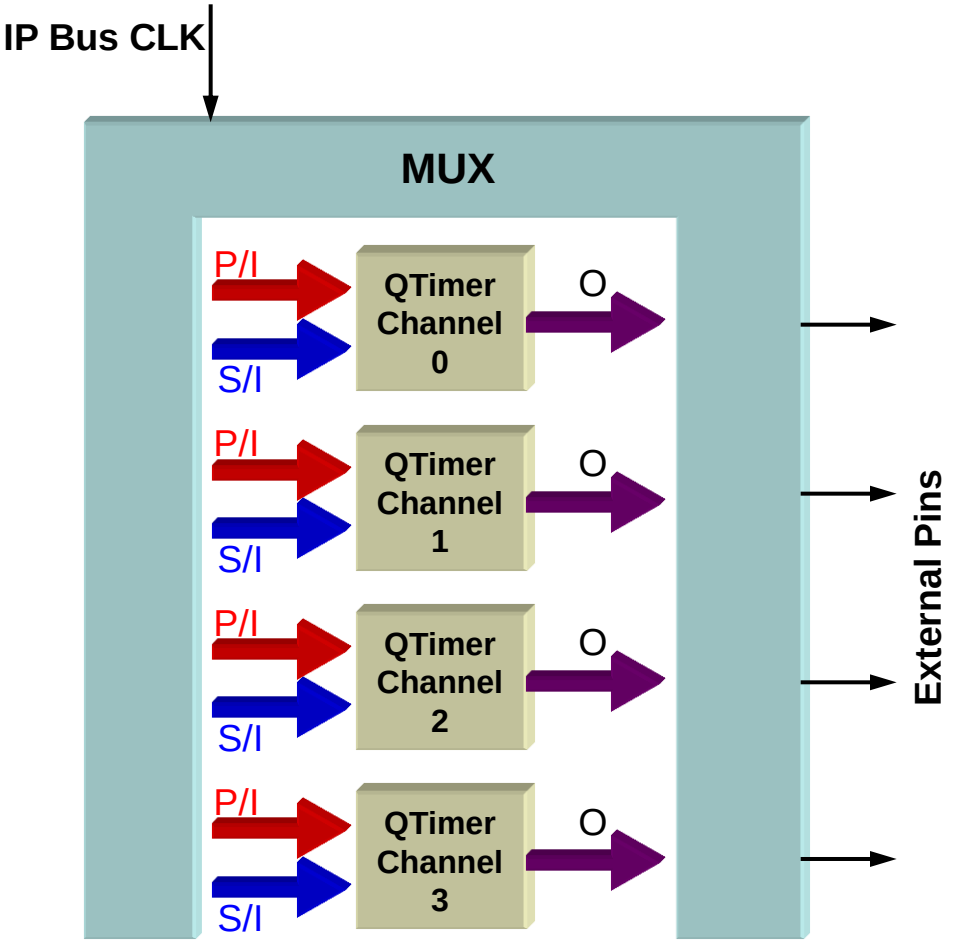
Quad Timer - Compare Pre-load - 2 Options





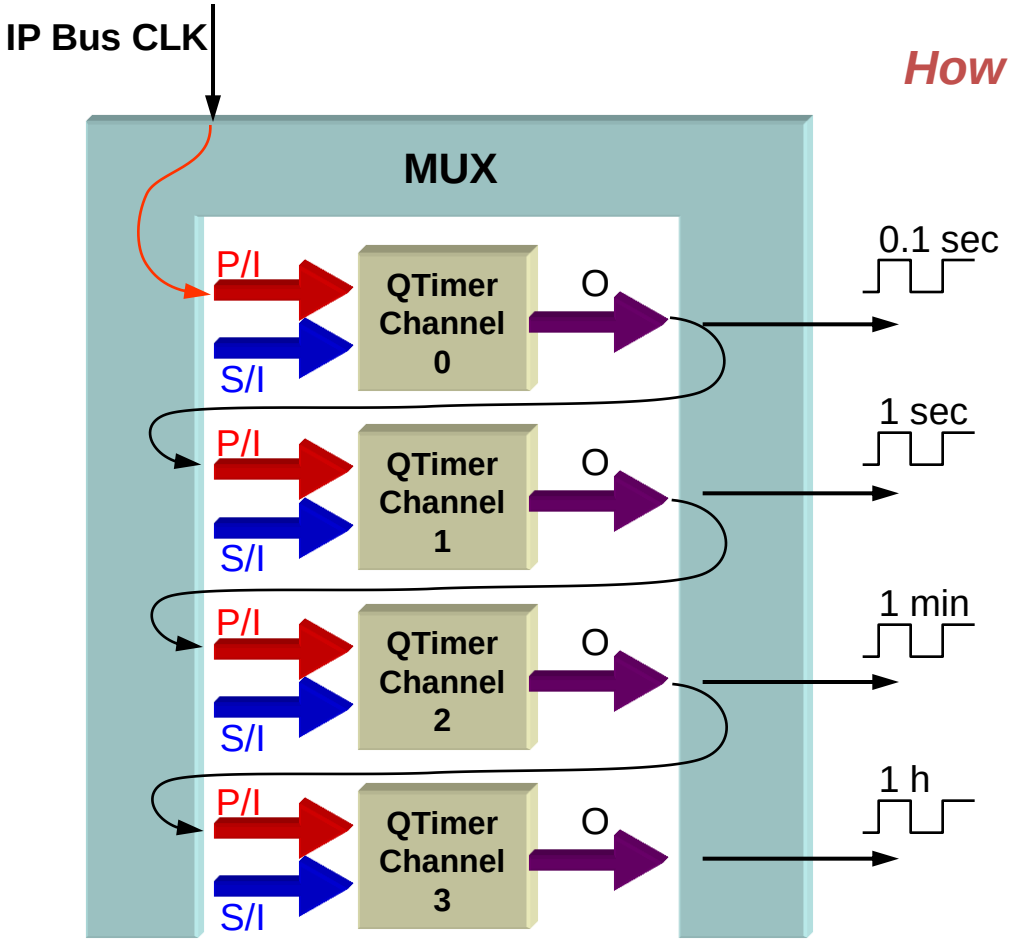
- The Compare Pre-load cycle begins with a compare event on TMRCMP2, causing TCF2 to be asserted.
- TMRCMP1 is loaded with the value in the TMRCMPLD1 one IPBus clock later.
- Additionally, an interrupt is asserted by the timer and the interrupt service routine is executed. During this time both Comparator Load registers are updated with new values.
- When TCF1 is asserted, TMRCMP2 is loaded with the value in TMRCMPLD2.
- On the subsequent TCF2 event, TMRCMP1 is loaded with the value in TMRCMPLD1.
- The cycle starts over again as an interrupt is asserted and the interrupt service routine clears TCF1 and TCF2, calculating new values for TMRCMPLD1 and TMRCMPLD2

Quad Timer Module - SW Model



- ✓ **Unique architecture with**
  - ✓ Primary input
  - ✓ Secondary input
  - ✓ Output
- ✓ **Powerful MUX**
  - ✓ Primary Input, Secondary Input and Output can be connected to ext. pins
- ✓ **Channels can be daisy-chained**
  - ✓ Output → Primary input - yields longer counter lengths
  - ✓ Output → Secondary input - time window counting of ext. event
- ✓ **Master Operation**
  - ✓ any channel can be a master that broadcasts its compare signal to the other channels.
  - ✓ Such way timer channels can be configured to reinitialize their counters and/or force their output signals to predetermined values.

Quad Timer Module - Advanced Operation #1

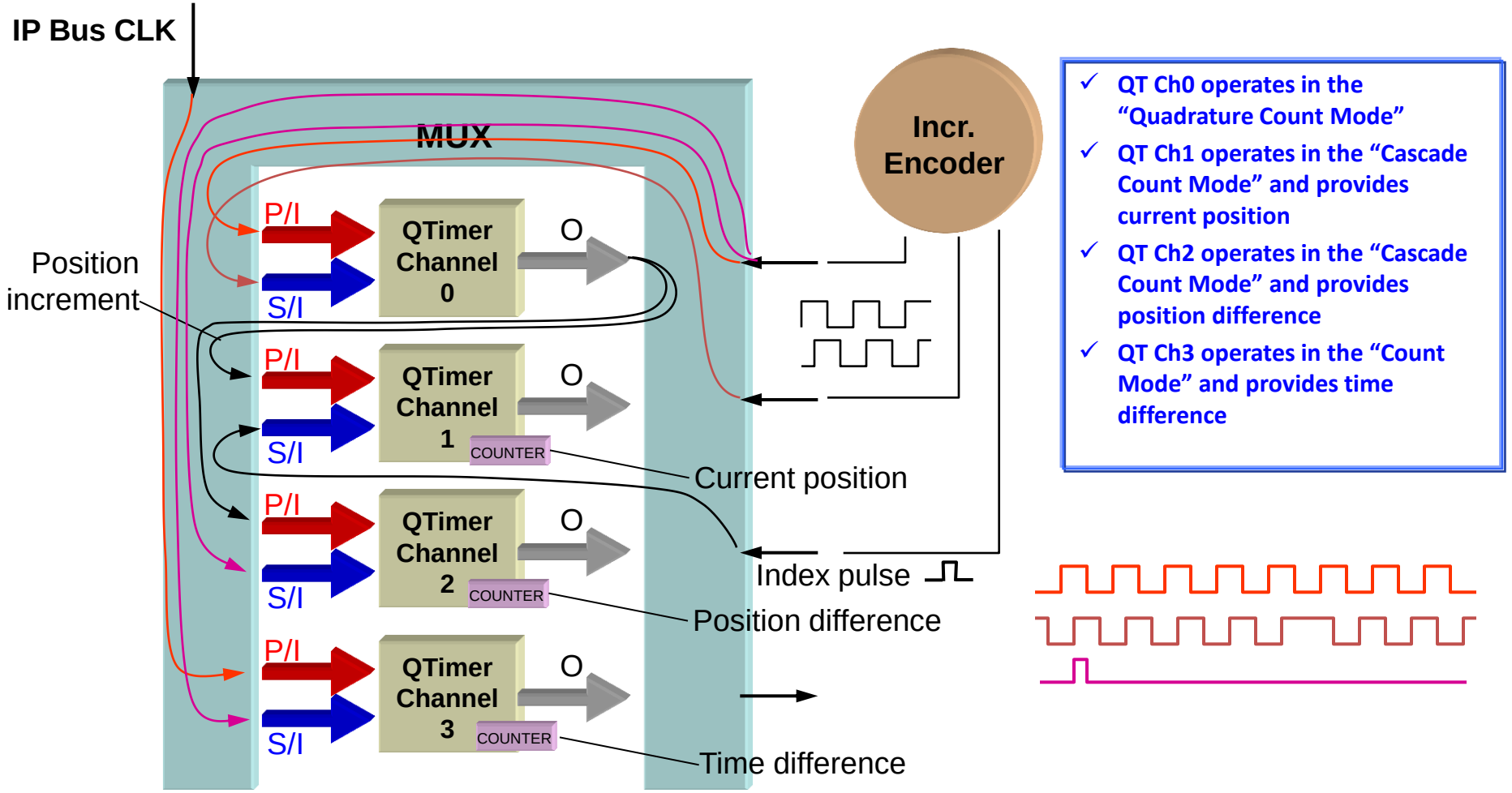


How to toggle - pin0 each 0.1 sec ?
- pin1 each 1 sec ?
- pin2 each 1 min ?
- pin3 each 1 h ?

- ✓ QT Ch0 operates in the “Count Mode”
- ✓ QT Ch1, Ch2 and Ch3 operate in the “Edge Count Mode”
- ✓ QT Ch0 compare is set to reflect 0.1 sec and to toggle the OFLAG
- ✓ QT Ch1 compare is set to reflect 1 sec and to toggle the OFLAG
- ✓ QT Ch2 compare is set to reflect 1 min and to toggle the OFLAG
- ✓ QT Ch3 compare is set to reflect 1 hour and to toggle the OFLAG
- ✓ Ch0, Ch1, Ch2 and Ch3 are “daisy-chained”

Quad Timer Module - Advanced Operation #2

How to measure the position and support the speed measurement ?



- ✓ QT Ch0 operates in the "Quadrature Count Mode"
- ✓ QT Ch1 operates in the "Cascade Count Mode" and provides current position
- ✓ QT Ch2 operates in the "Cascade Count Mode" and provides position difference
- ✓ QT Ch3 operates in the "Count Mode" and provides time difference

MC56F8023/56F8025/56F8036/56F8037

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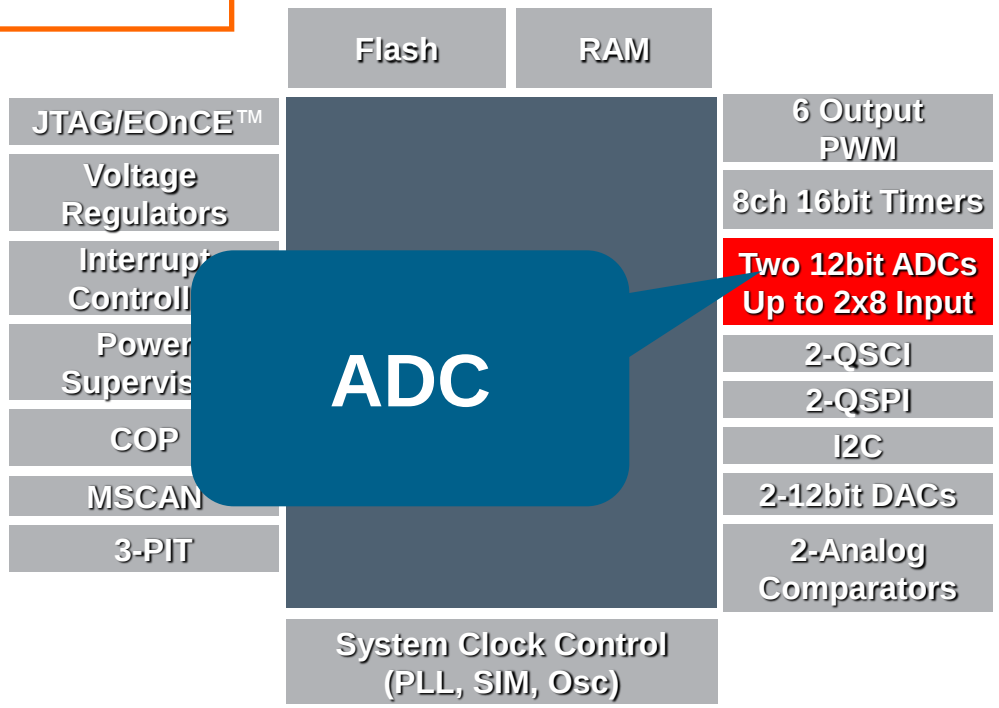
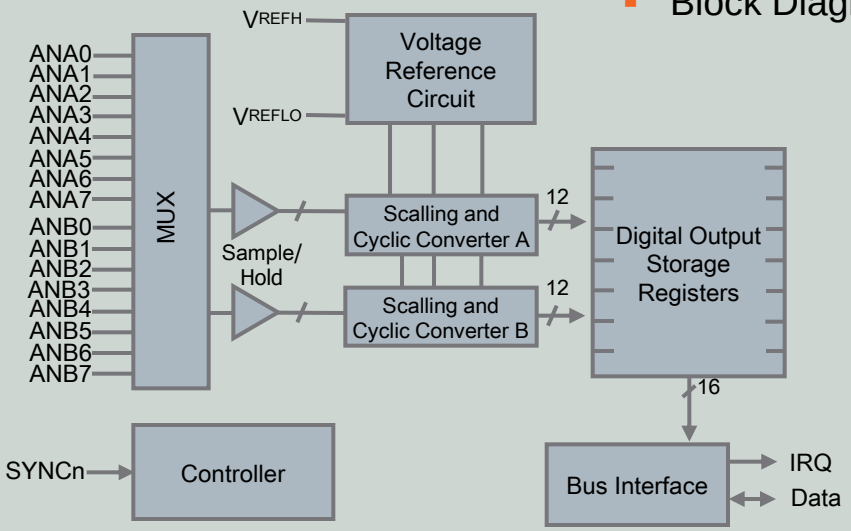


Analog to Digital Converter

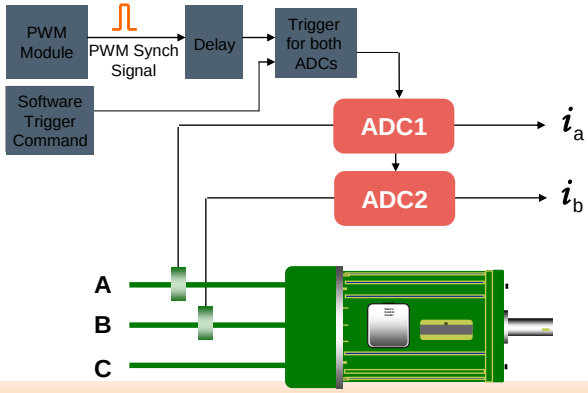
- 12-bit resolution
- Two ADCs per module
- Single ended or differential inputs
- Maximum ADC clock frequency is 5.33 MHz with 187 ns period
- Sampling rate up to 1.78 million samples per second (loop mode and simultaneous conversion considered)
- Single conversion time of 8.5 ADC clock cycles (1.59 µs)
- Additional conversion time of 6-ADC clock cycles (1.125 µs)
- Eight conversions in 26.5-ADC clock cycles (4.97µs) using parallel mode
- ADC can be synchronized to the PWM via the SYNC0/1 input signal provided the integration permits the PWM to trigger a timer channel connected to that input
- Ability to sequentially scan and store up to 16 measurements
- Ability to scan and store up to eight measurements, on each ADC converter while operating simultaneously and in parallel
- Ability to scan and store up to eight measurements, on each ADC converter while operating asynchronously to each other in parallel
- Optional interrupts at end of scan if an out-of-range limit is exceeded or at zero crossing
- Optional sample correction by subtracting a pre-programmed offset value
- Signed or unsigned result
- DAC outputs can be connected to ANA7 and ANA8 on the 56F8037

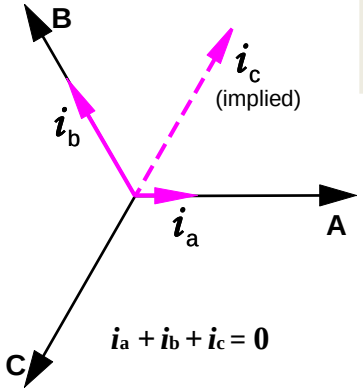
ADC – Modes of Operation

- Block Diagram



- Motor Control Example

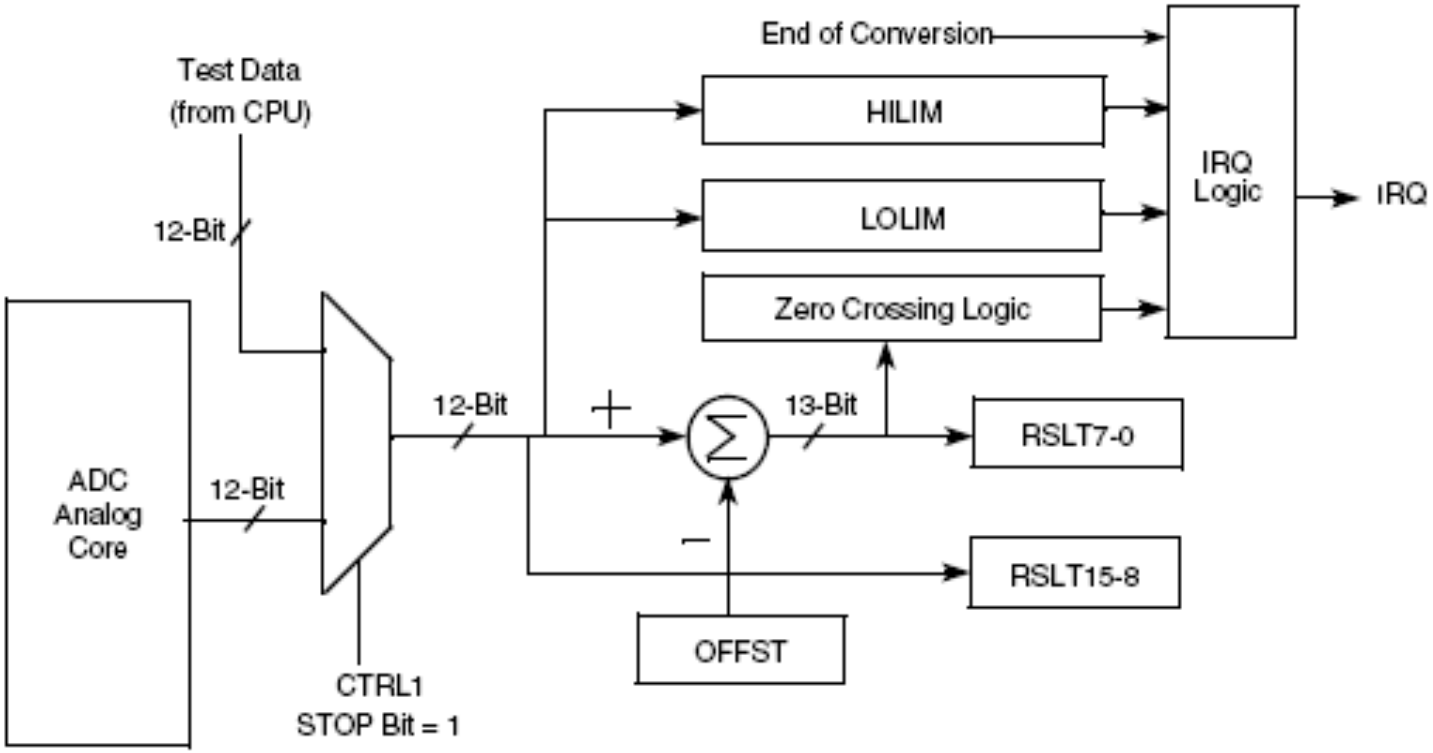




- **Once Sequential** – samples from SAMPLE0 to a first disabled channel
- **Once Simultaneous** – samples two channels at time SAMPLE0/SAMPLE4 to a first disabled channels
- **Loop Sequential** – samples selected channels in loop until STOP bit is set
- **Loop Simultaneous** – samples selected two channels in loop until STOP bit is set
- **Triggered Sequential** – sampling of single channels initiates with every recognized START command or SYNC pulse
- **Triggered Simultaneous** – sampling of two channels initiates with every recognized START command or SYNC pulse

- 12 bit resolution at 1.125us conversion time for two conversions
- Both ADCs can be triggered at the same time for simultaneous sampling

ADC Result Processing



ADC Operation Modes

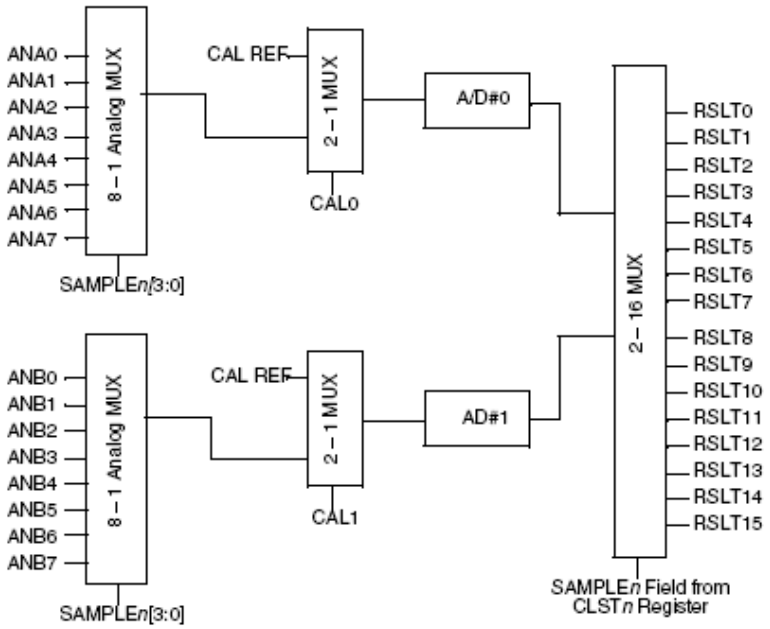


Figure 2-1. ADC Sequential Operation Mode

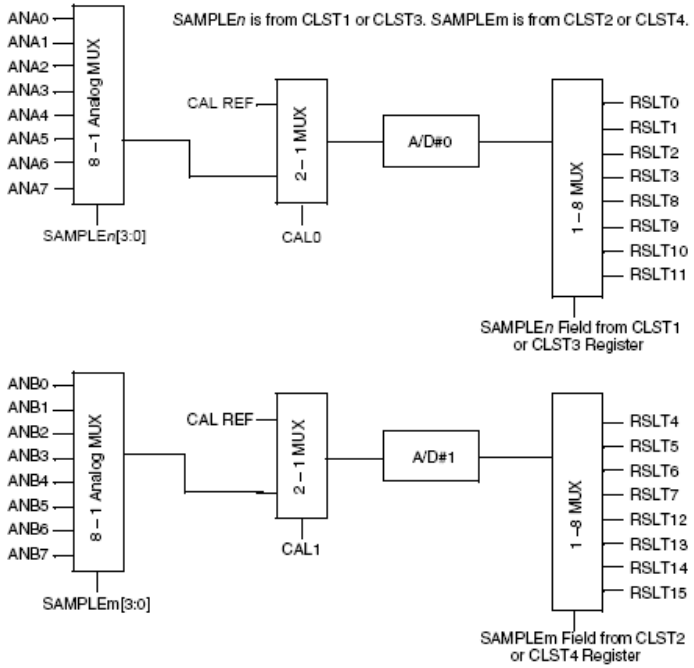
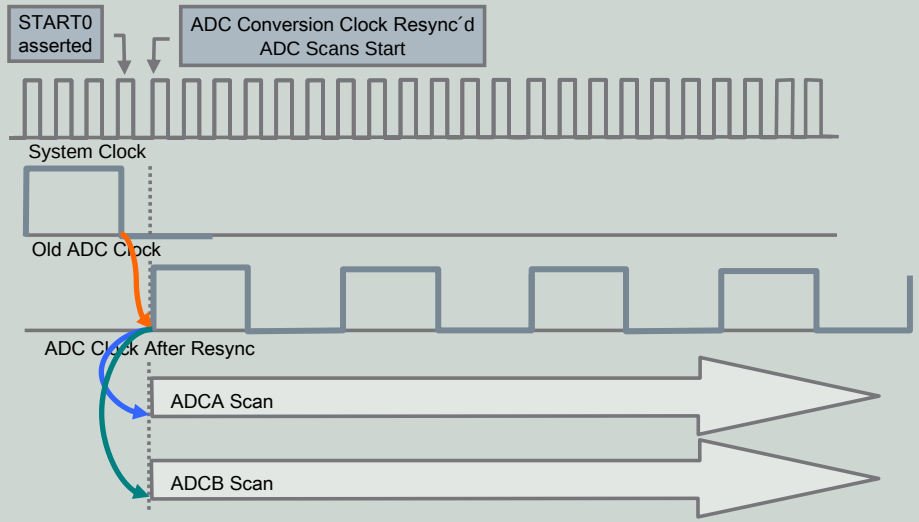
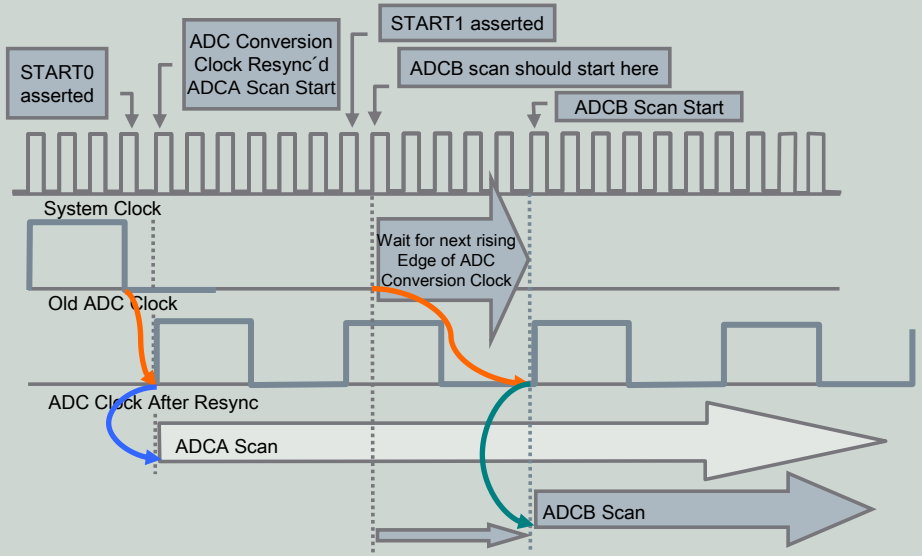


Figure 2-2. ADC Parallel Operation Mode

ADC – Clock Resynchronization

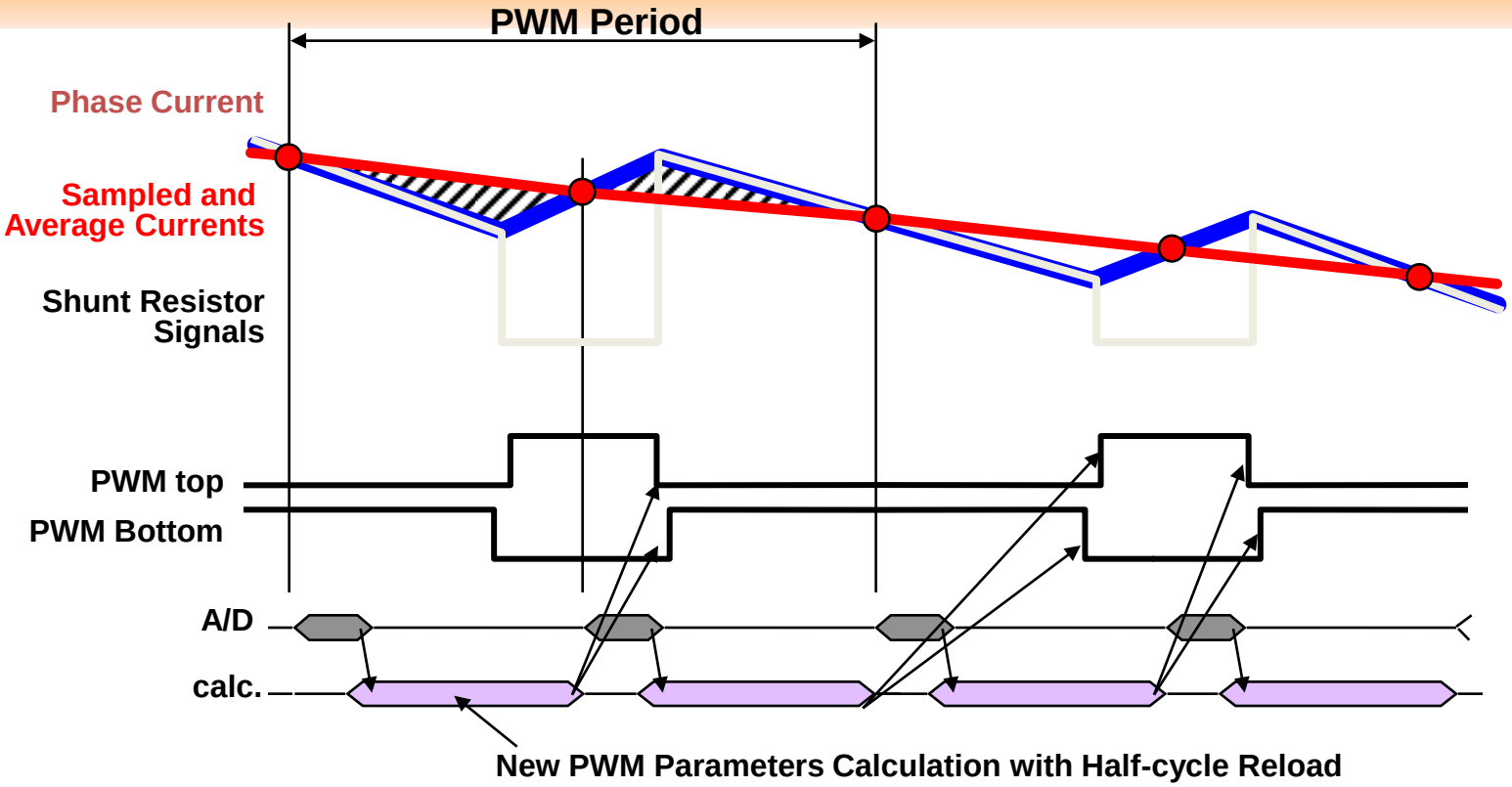


- In this case (SIMULT = 1) both ADCs are triggered by the same start signal. When asserting the start of a scan, either by writing to a STARTn bit or by a SYNCn signal, the ADC clock is re-synchronized to align it to the system clock.
- This allows the commanded scan to begin as soon as possible rather than wait up to five additional system clocks for the start of the next ADC clock period.



- In this case (SIMULT = 0) both ADCs operate using independent STARTn bits and SYNCn signals. Note that the first scan is re-synchronized to the system clock but the second scan may wait up to five additional system clocks before starting.
- Also, please note which converter is synchronized to the system clock depends on which convert first starts to use the ADC.

ADC - PWM Synchronization Benefits



- ADC Sampling helps to filtering the measured current - antialiasing.
- Noise free ADC sampling when the power switch is not acting
- ADC samples are taken when shunt resistor signal (information) is available

• MC56F8023/56F8025/56F8036/56F8037

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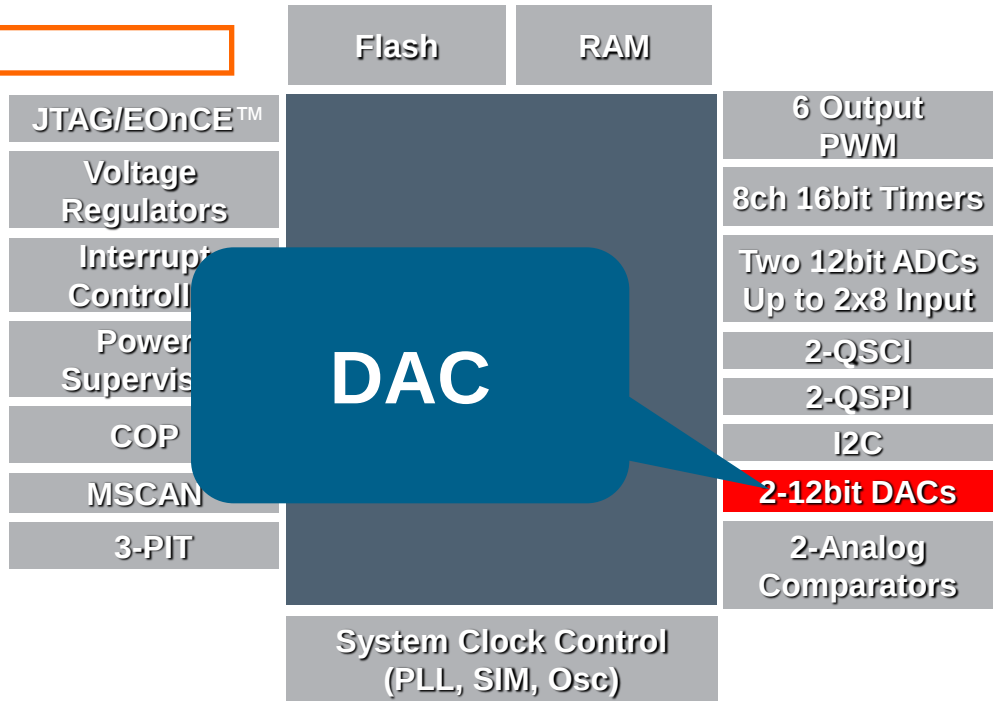
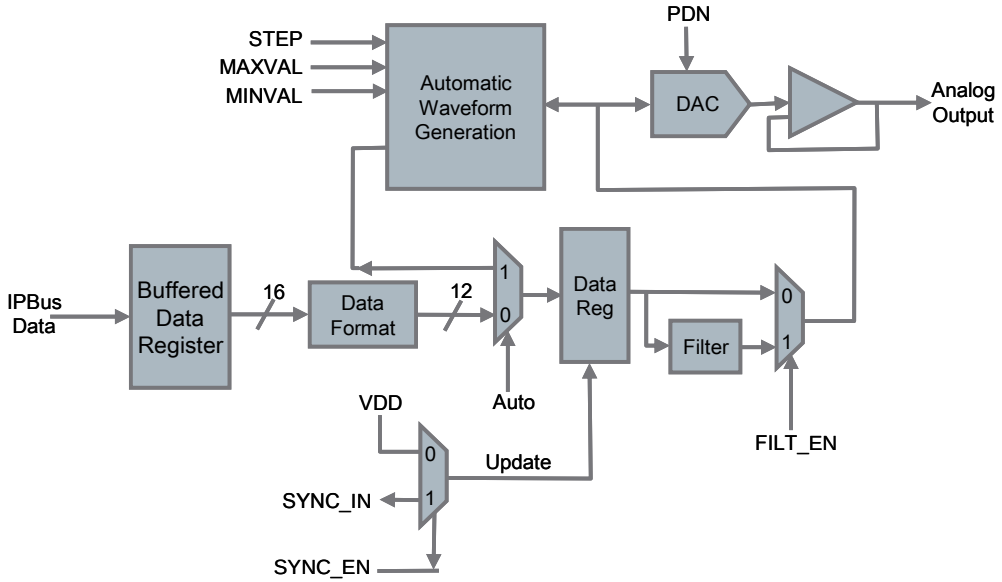
- Interrupt Controller (ITCN)
- Debugging Unit



Digital to Analog Converter



- 12-bit resolution
- 2us settling time, 0.5million conversions per second
- Software controlled power down mode
- Output can be routed to internal comparator, ADC, or optionally off chip (MC56F8037 only)
- DAC can drive 3 KΩ, 400 pF load
- Choice of asynchronous or synchronous updates
- Synchronization input can be connected to on chip PITs, TMRs, PWM reload flag, or GPIO inputs
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth waveforms
- Programmable period, update rate, and range in automatic mode

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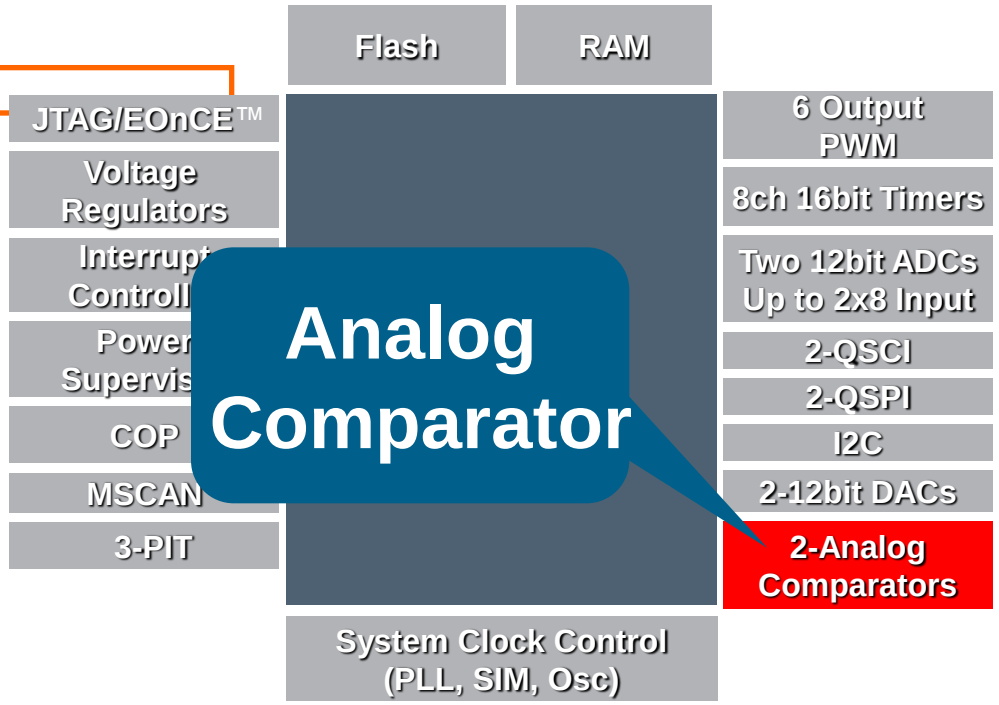
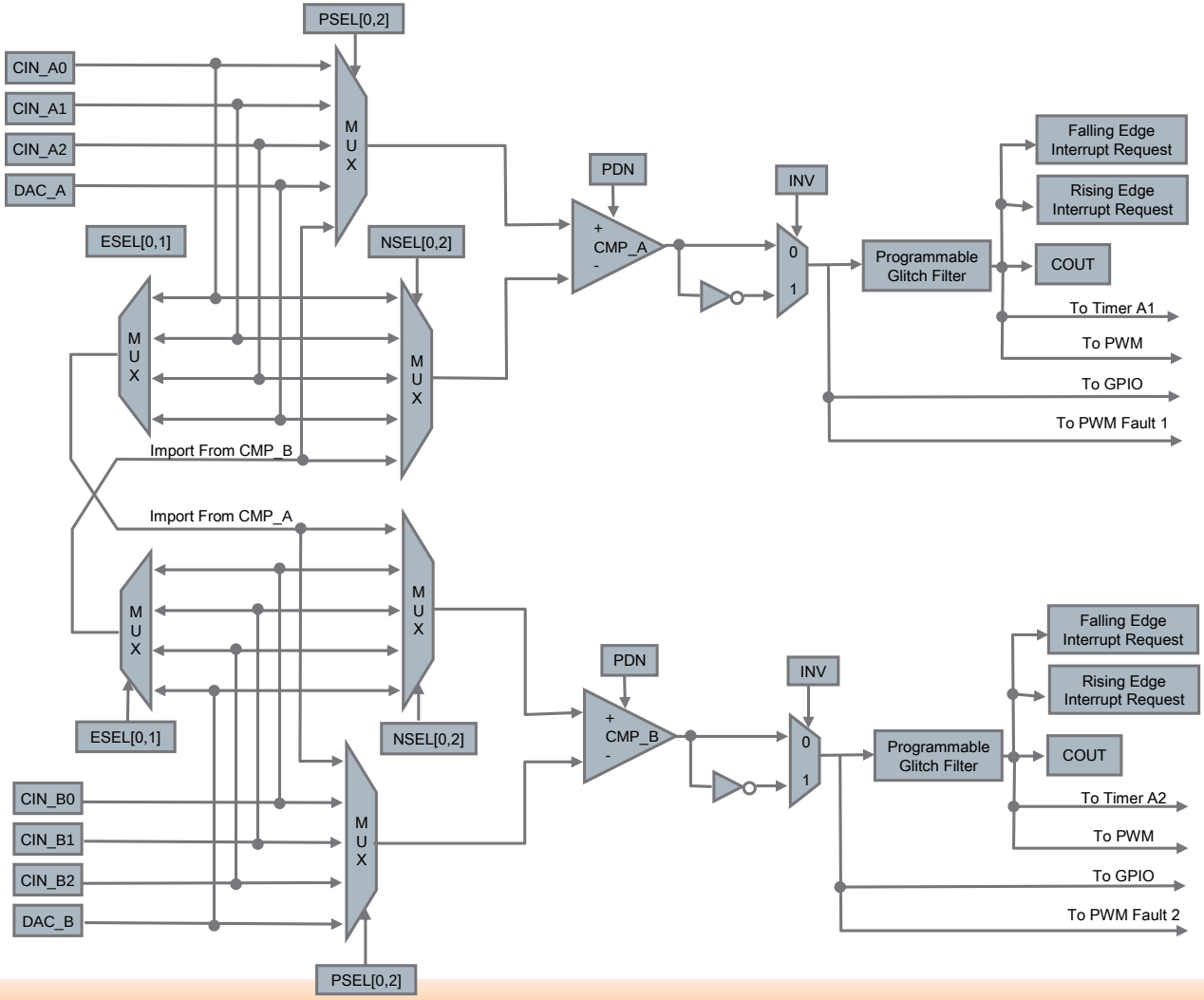


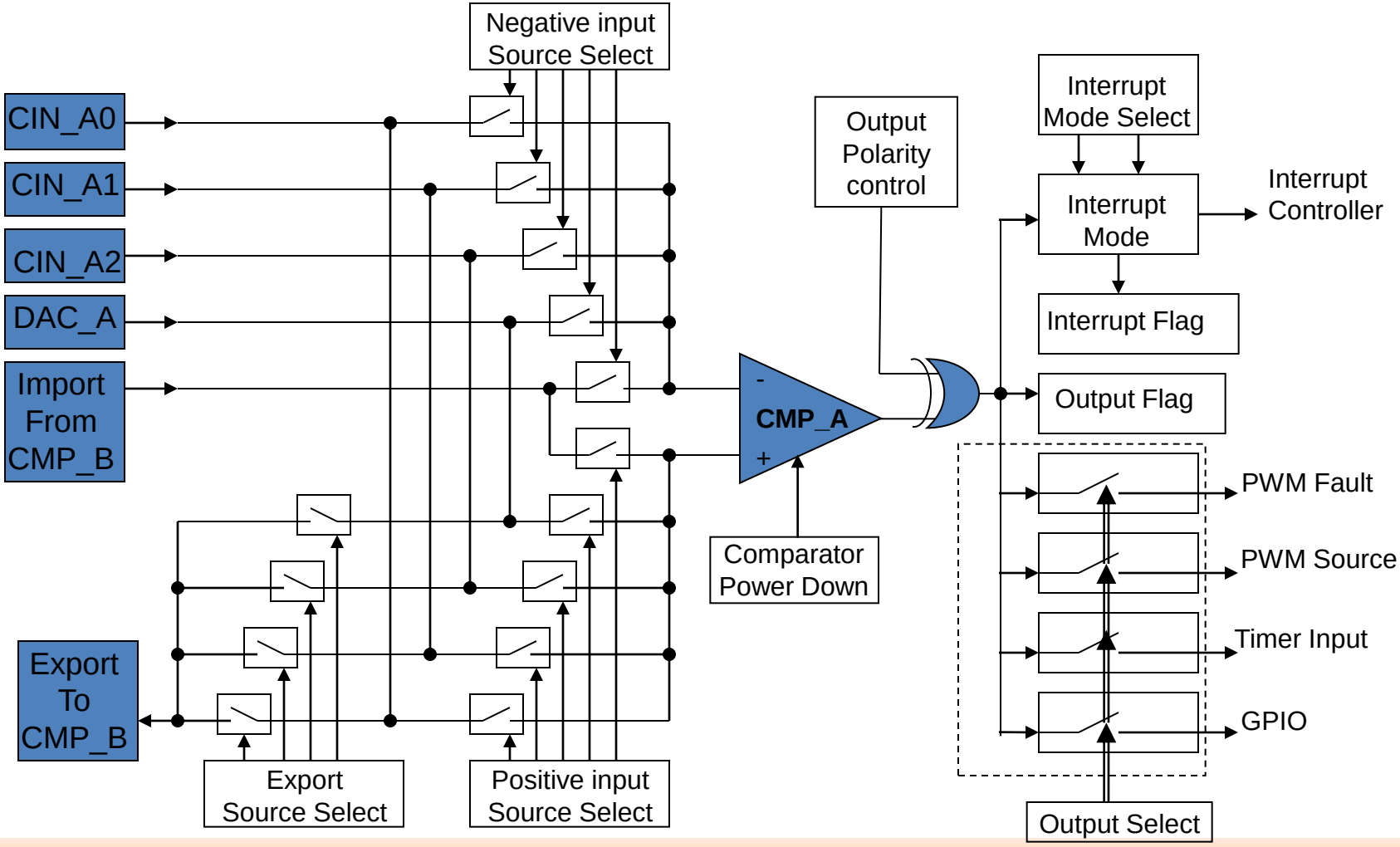
Analog Comparator

- Up to Two continuous-time differential-input analog comparator modules
- Input Propagation Delay 35 ns
- Internal switching matrix supports the independent connection of the analog inputs to the + and – input of the analog comparator and to the comparator's export output
- 5 selectable input sources:
  - *Three GPIO Pins (CIN1, CIN2, and CIN3).*
  - *One DAC output,*
  - *One import input from another comparator module*
- Analog comparator polarity control (optional inversion)
- Programmable low-pass filter
- Power saving mode
- Falling and rising comparator edge detection with compare interrupt on rising and/or falling comparator edge
- Output can be used to control Timer inputs, PWM faults, PWM control, external pin output, or as a interrupt Source.

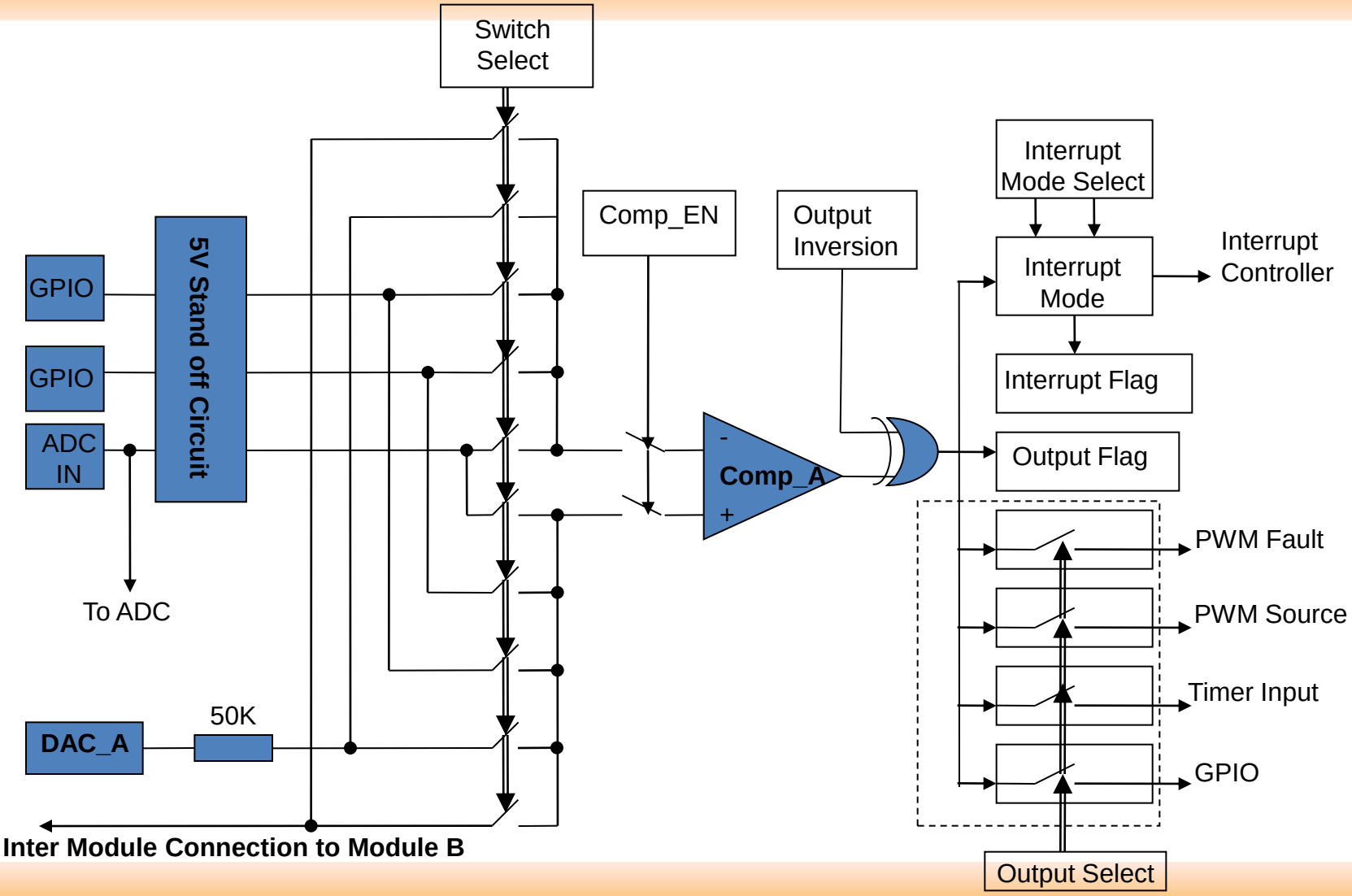
Analog Comparator – Block Diagram



Analog Comparator Interconnection

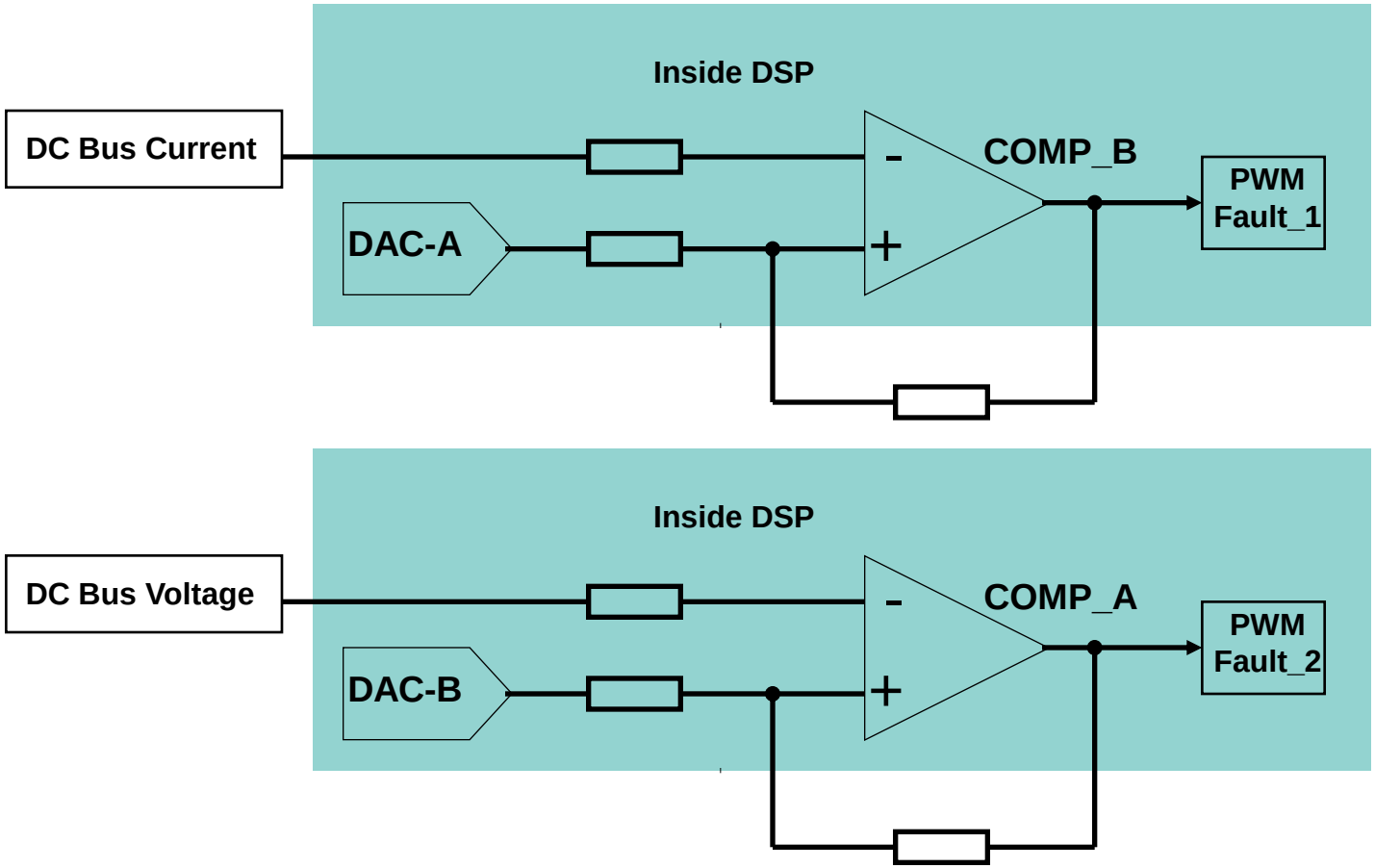


DAC and Comparator Module

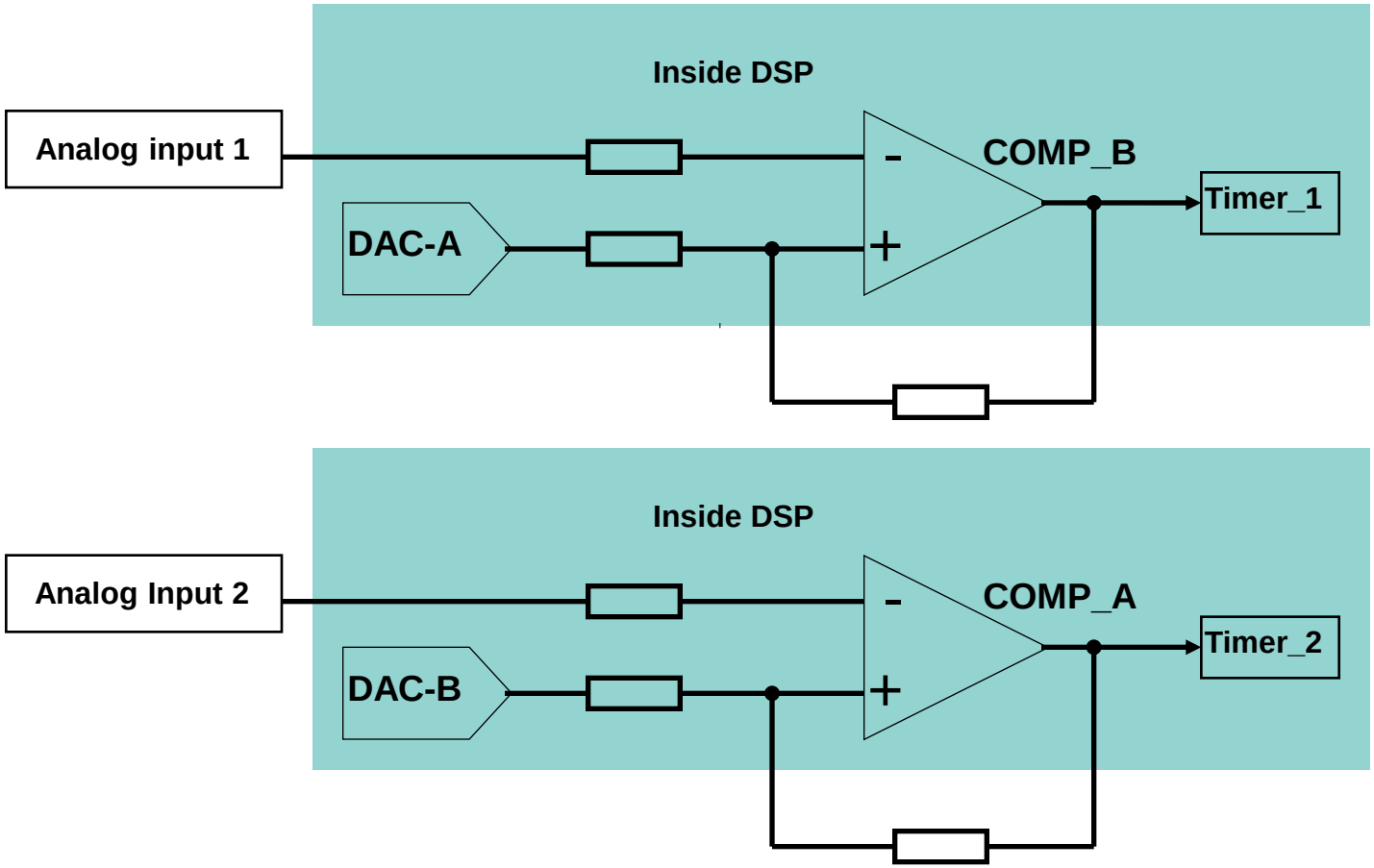


DAC and Comparator Application

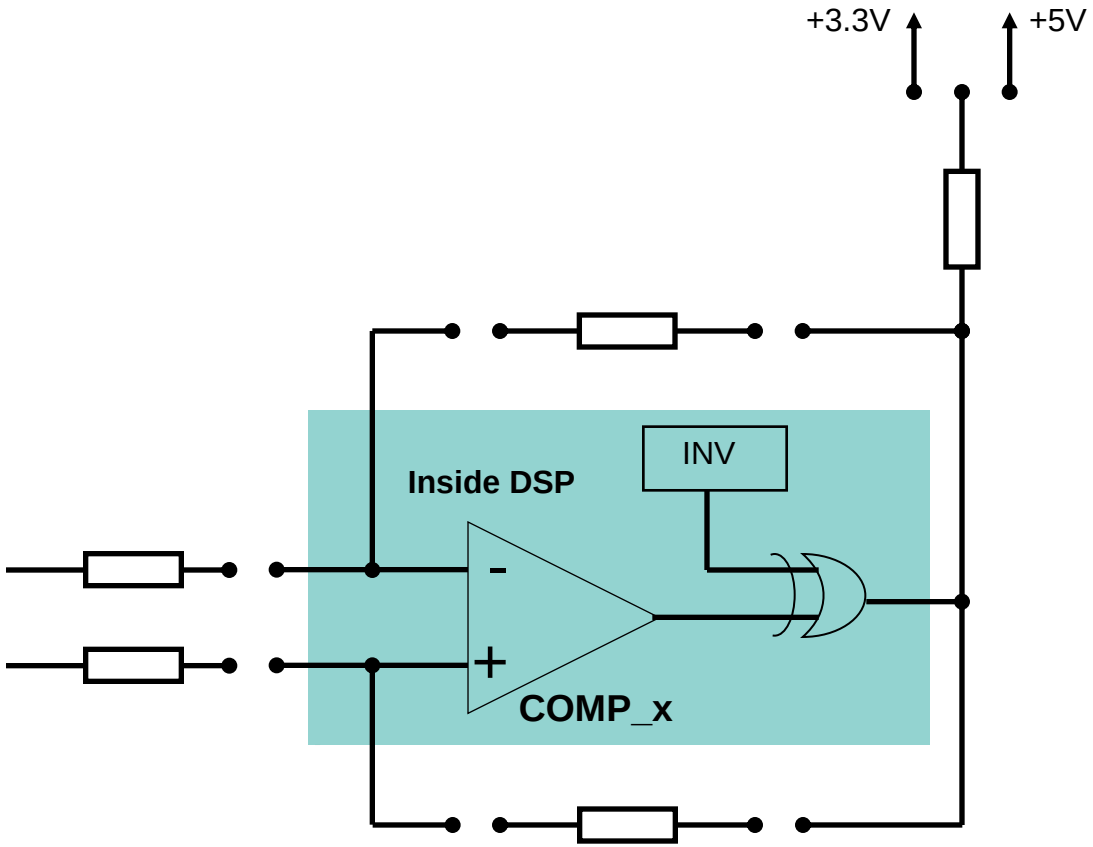
- Fault signal detection for Motor Control, UPS and SMPS



DAC and Comparator Application - Timer Triggering



Comparator with Hysteresis



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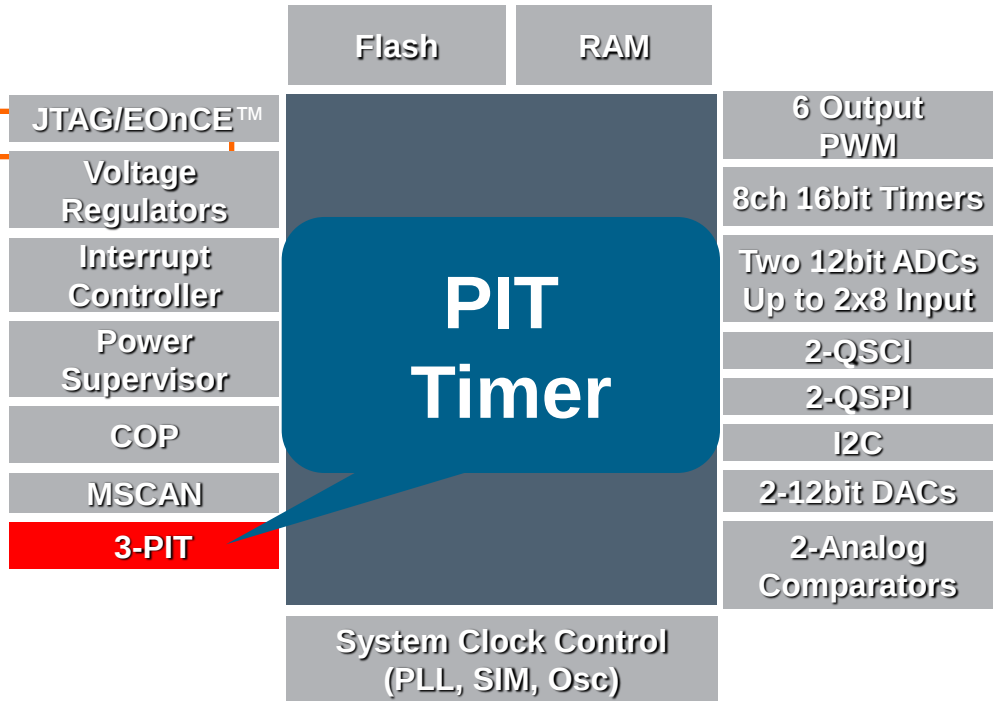
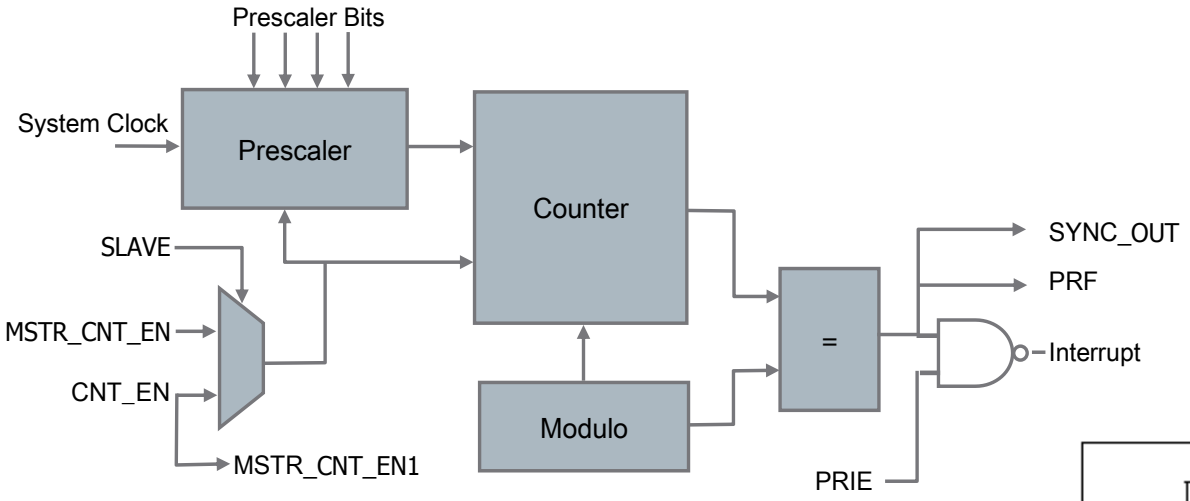


Programmable Interval Timer

- Three 16-bit general purpose up counter with a 4-bit prescaler
- Individually programmable time interval based on system clock source
- Counter roll-over generates interrupt request if roll-over interrupt is enabled
- Counter roll-over signal can be used as DAC conversion start signal.
- All PITs can be synchronized with PIT0
- Low Power Mode support

PIT Timer



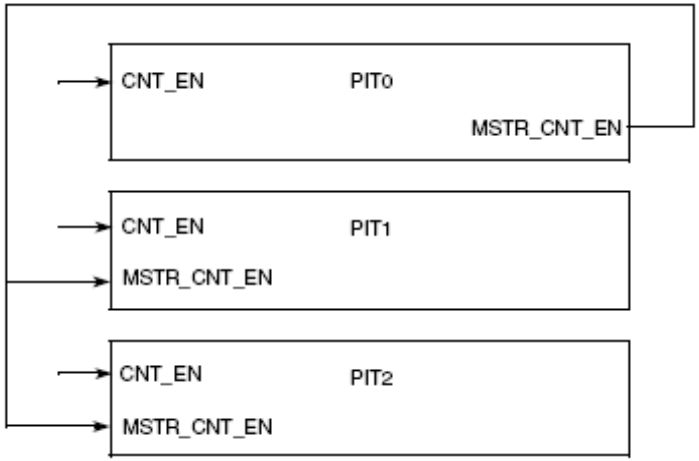


Figure 16-3. CNT_EN Connection Between Multiple PITs

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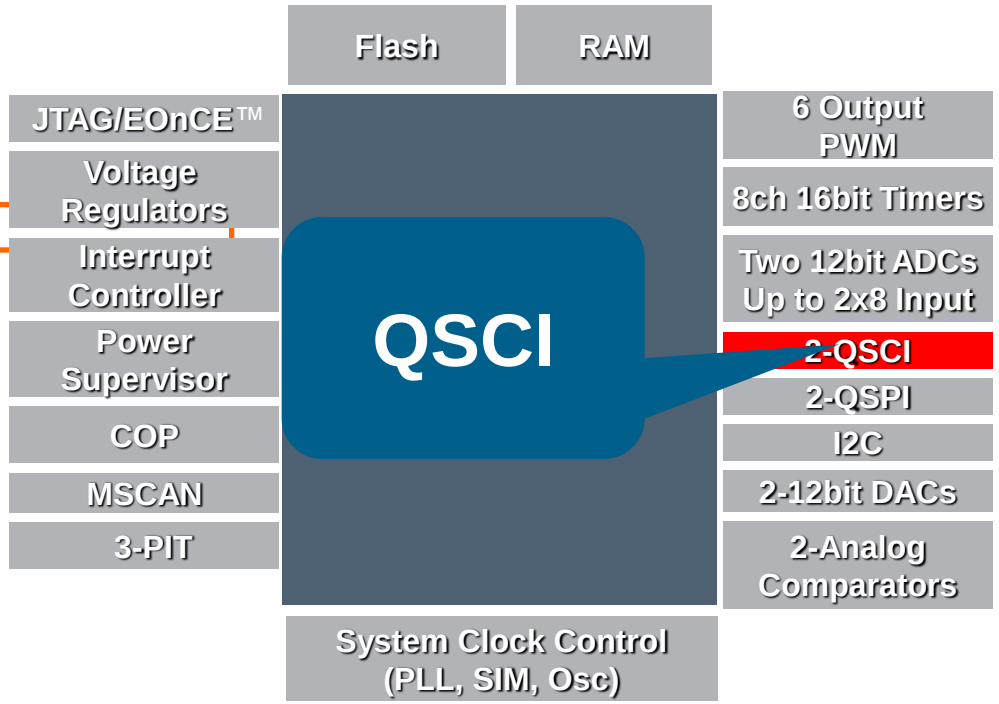
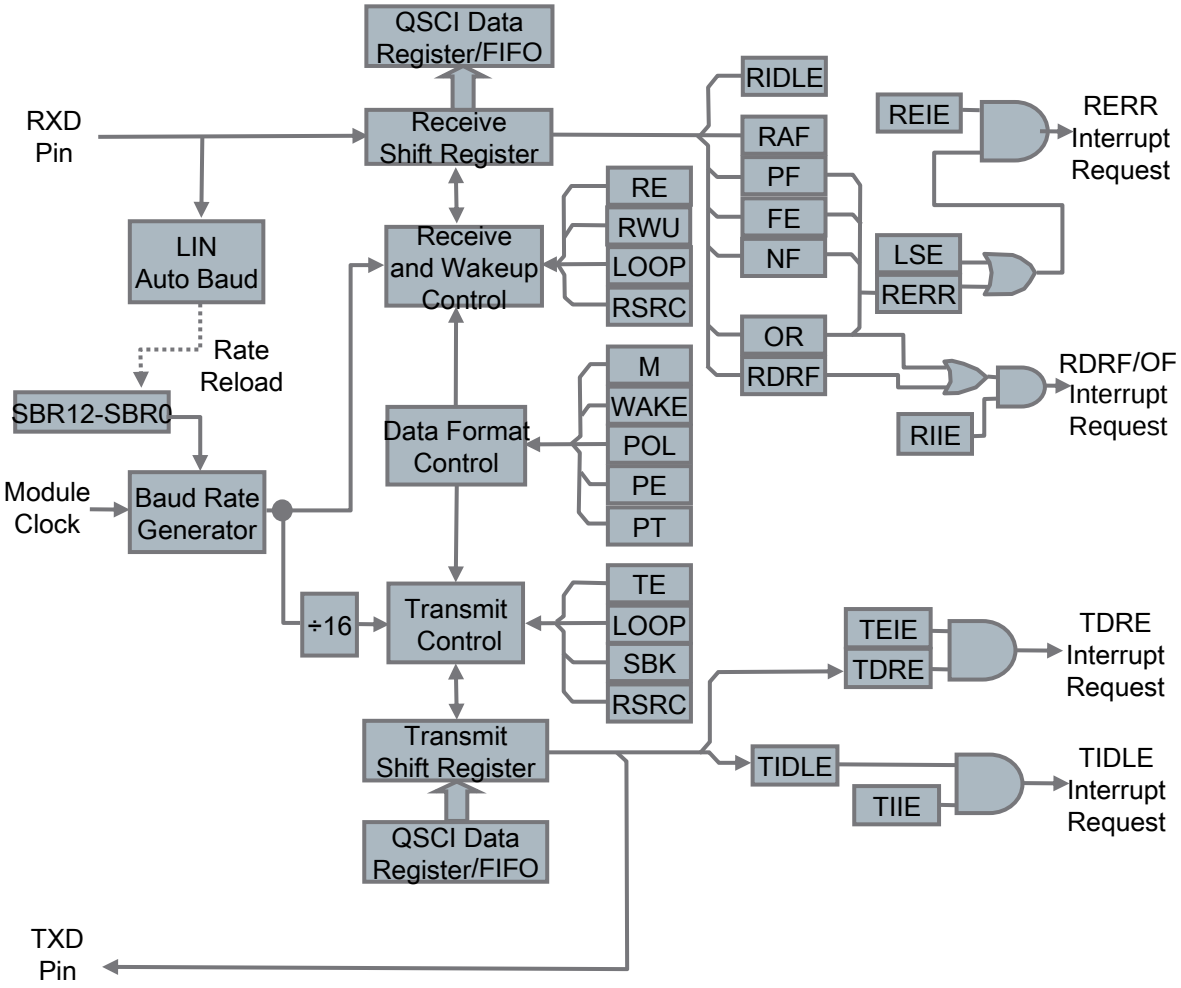


QSCI Communication Module

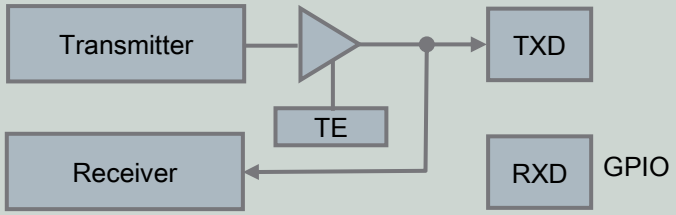
- Baud rates up to 2Mbps
- Full duplex operation provides simultaneous data transmit and receive
- Half duplex operation allows data transmit and receive via single wire.
- Separately enabled transmitter and receiver
- 13-bit baud rate selection
- Support LIN Slave Mode (LIN Auto Baud feature)
- Four-bytes-deep FIFOs on both TX and RX

QSCI Communication Module – Block Diagram

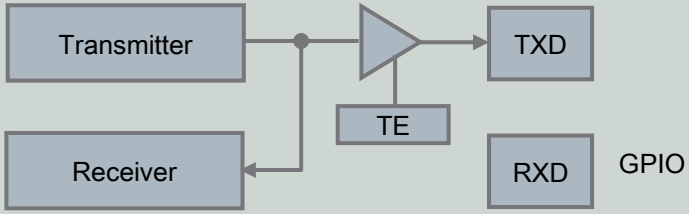


QSCI – Single-Wire & Loop Mode Operation

- Single-Wire Operation (LOOP = 1, RSRC = 1)



- Loop Operation (LOOP = 1, RSRC = 0)



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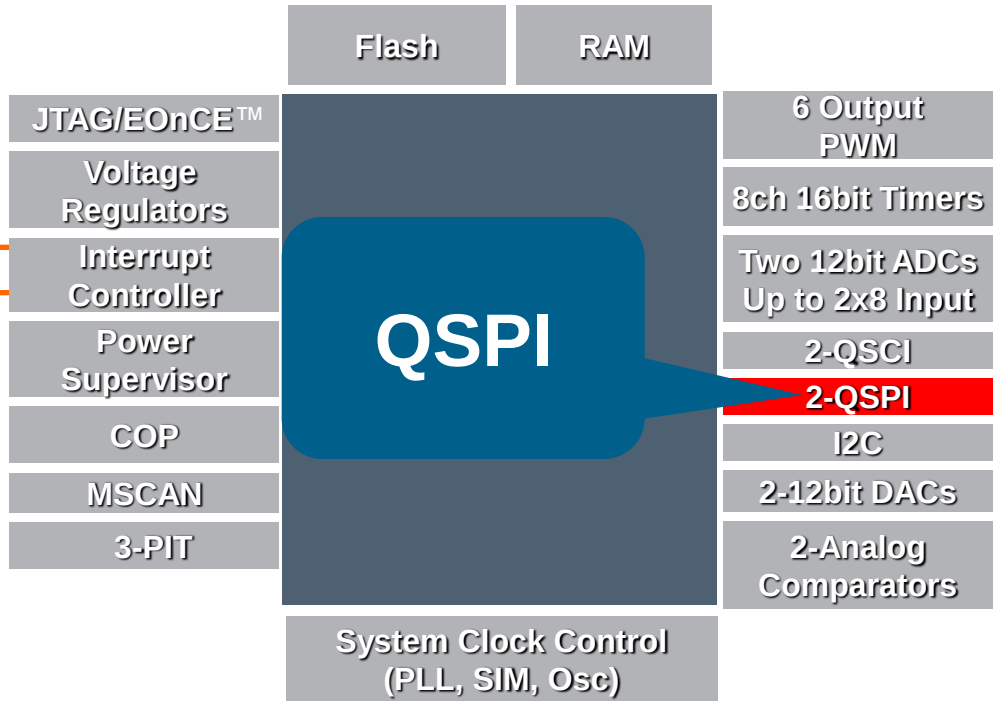
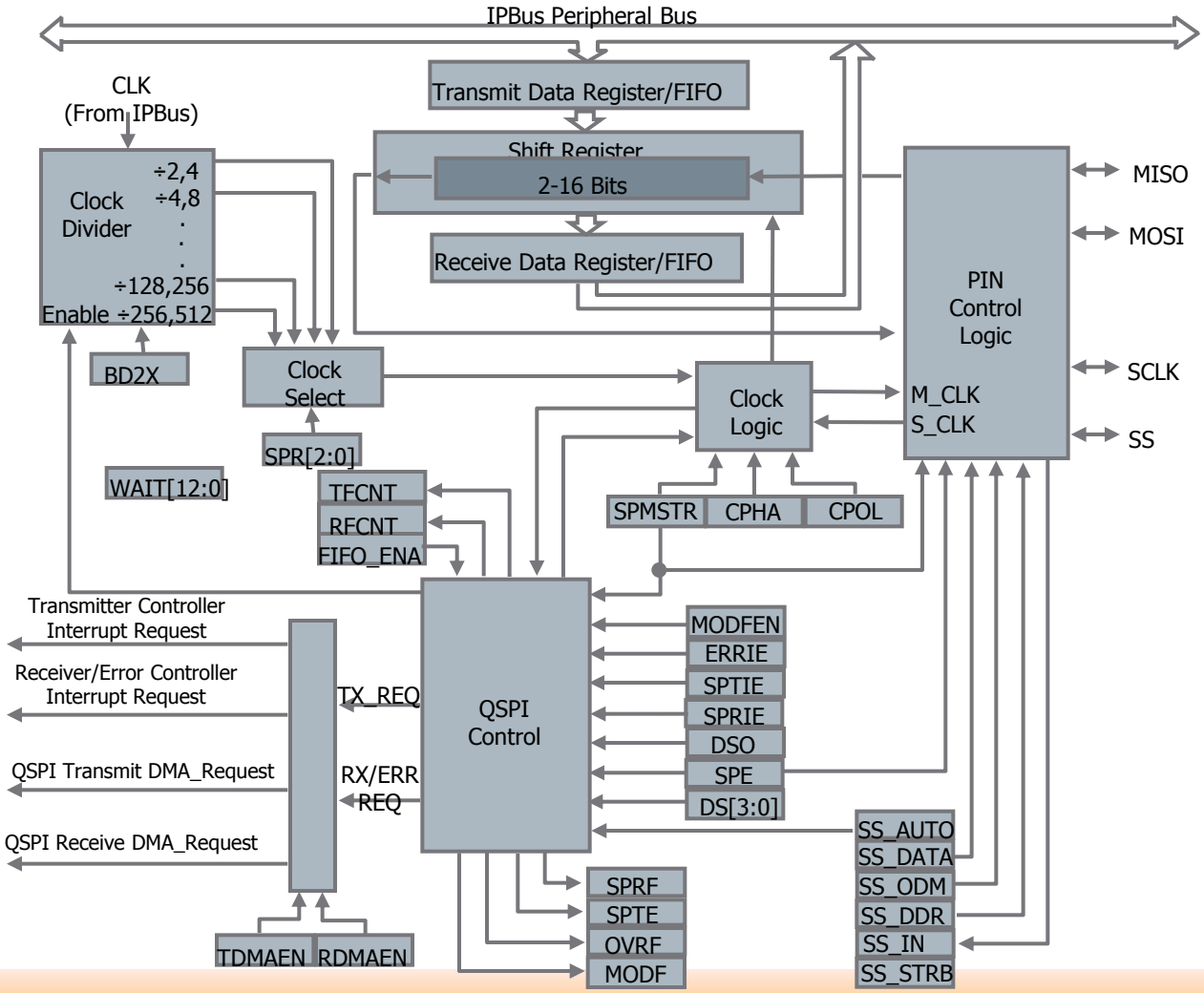


QSPI Communication Module

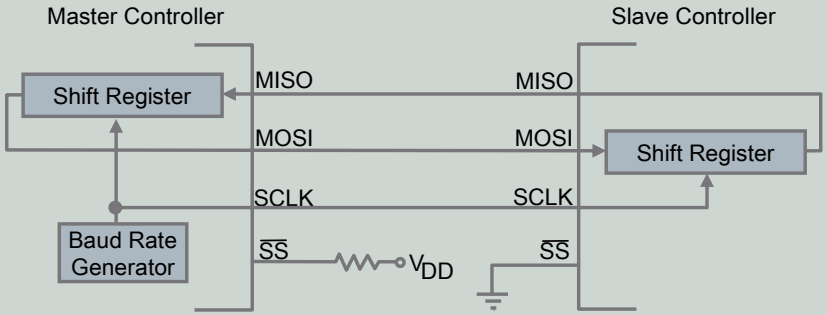
- Nine master mode frequencies (maximum = bus frequency ÷ 2)
- Maximum slave mode frequency < bus frequency ÷ 2
- Supports inter-processor communications in a multiple master system
- Full-Duplex Operation
- Double-buffered Operation with separate transmit and receive registers
- Programmable length transmissions, 2 to 16 bits
- Programmable transmit and receive shift order, MSB or LSB transmitted
- Four-Words-deep FIFOs on both TX and RX

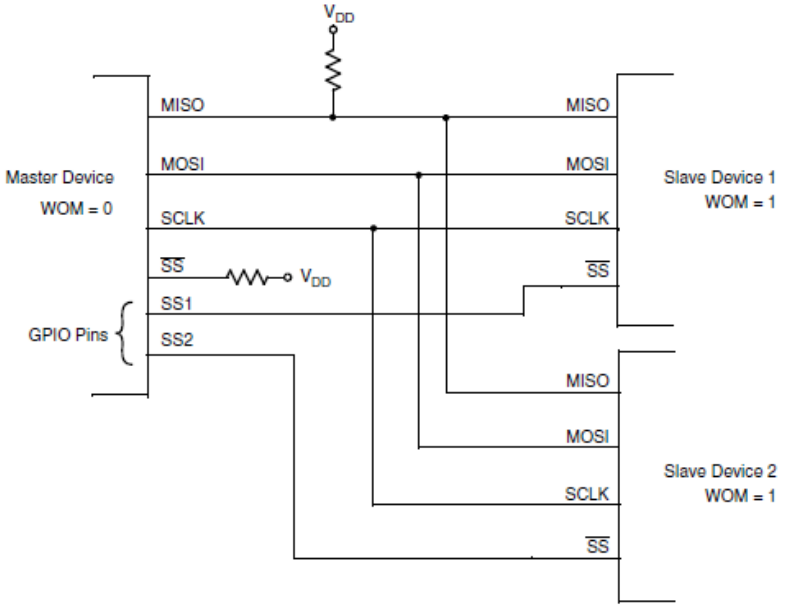
QSPI Communication Module – Block Diagram



QSPI Connection

- Full Duplex Master/Slave Connections





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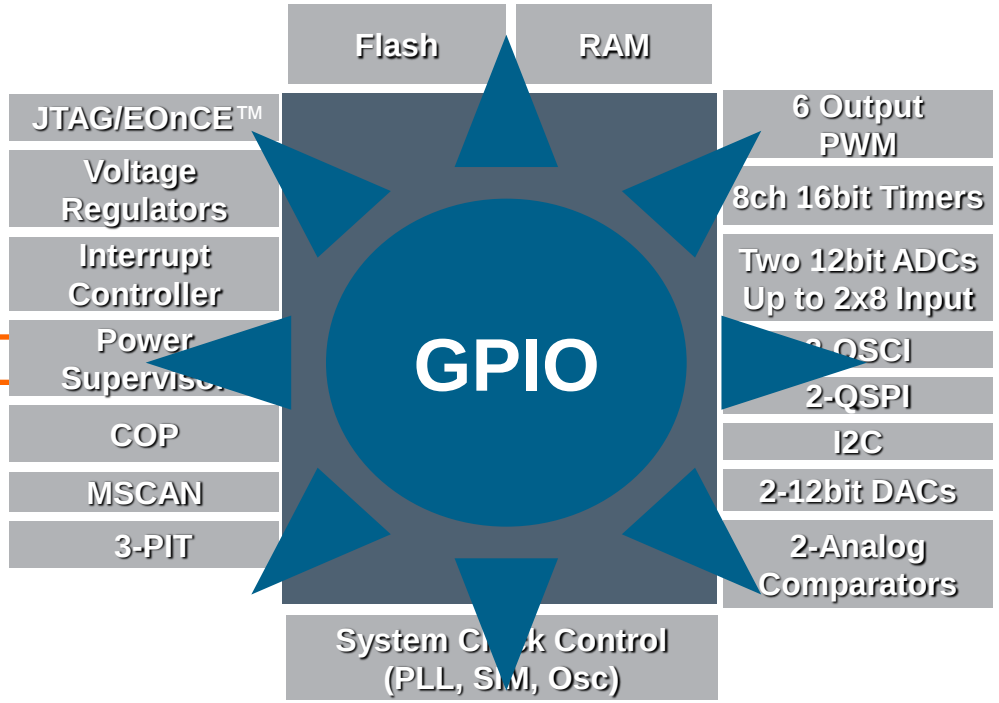
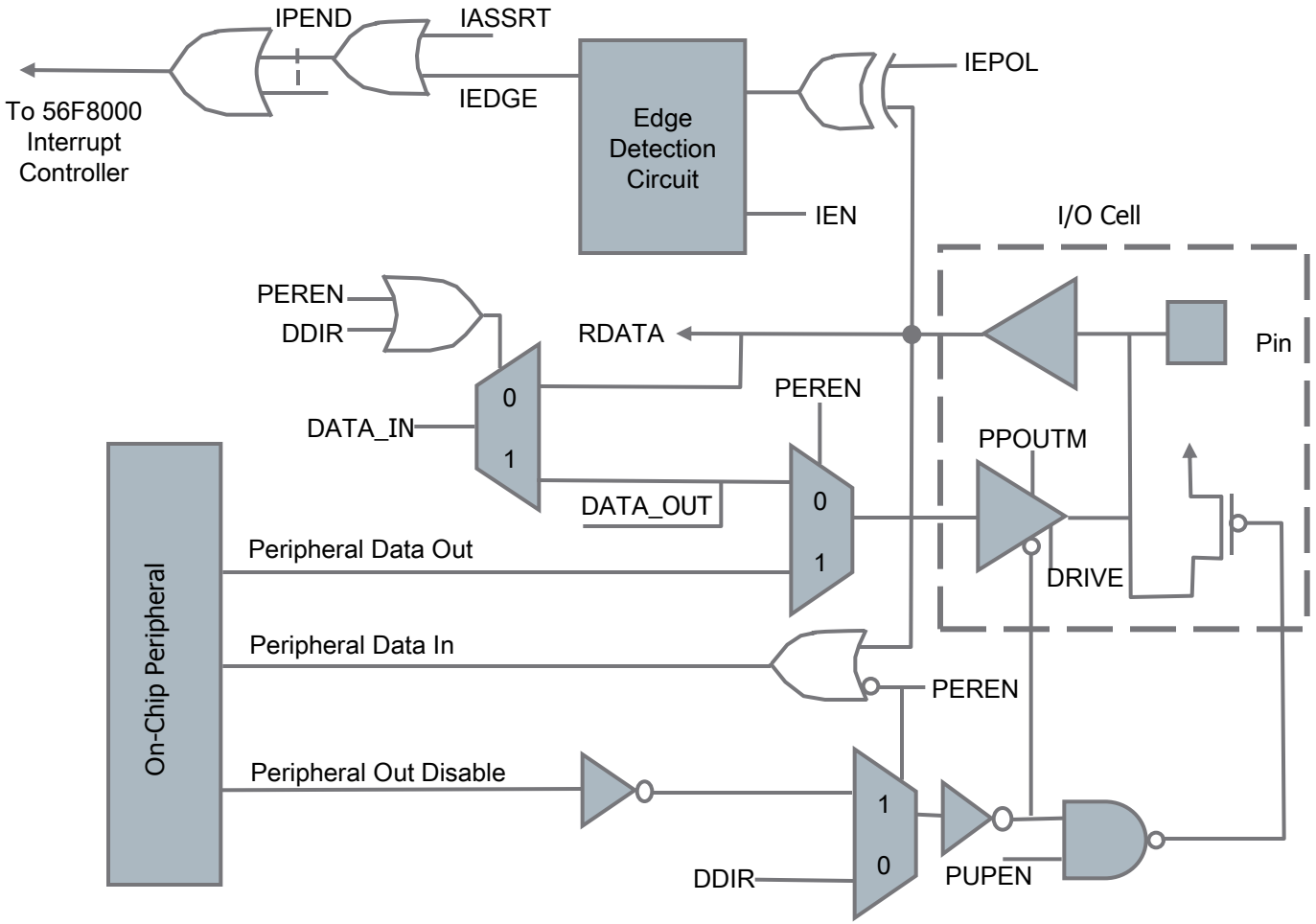


GPIO – General Purpose Input Output

- ALL pins (except power and ground) are muxed with GPIO including ADC inputs and JTAG pins
- Individual control for each pin to be in either Peripheral or GPIO mode
- 5 V tolerant
- Individual input or output direction control
- *Two output modes*
  - *Push-Pull mode*
  - *Open Drain mode*
- Individual pull-up enable control
- Optimized for use with the keypad interface with push-pull I/O
- Can monitor pad logic value even when GPIO is not enabled using the RAWDATA register
- Edge Sensitive Interrupt Assert Capability
- Interrupts can be generated by hardware or software
- Two output current drive strength modes
  - *4mA or 8mA*

GPIO – Block Diagram



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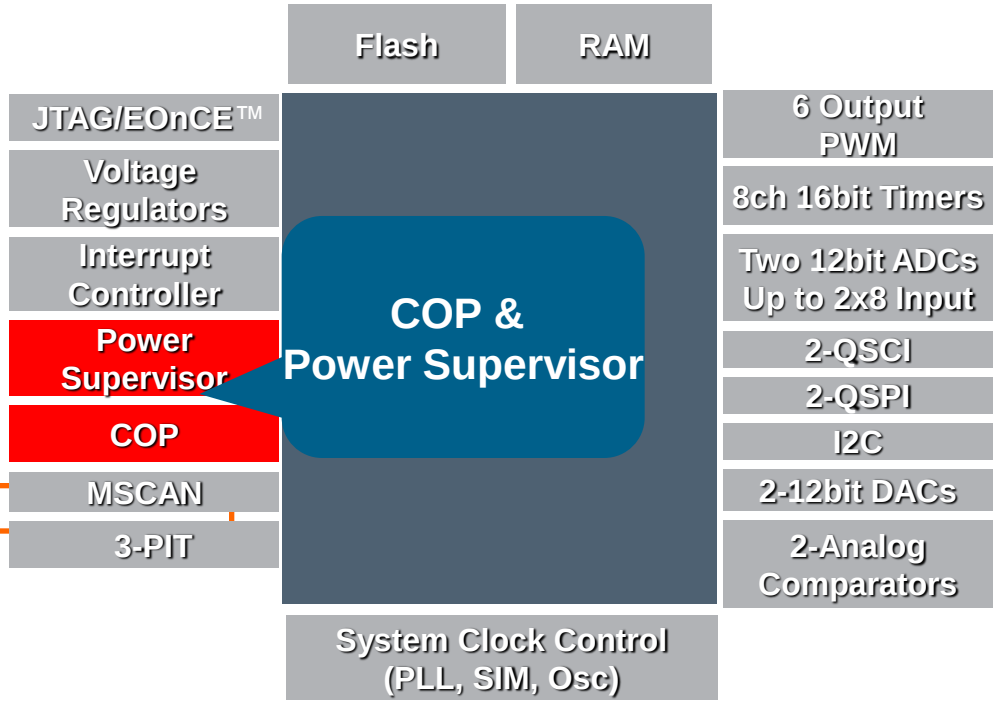


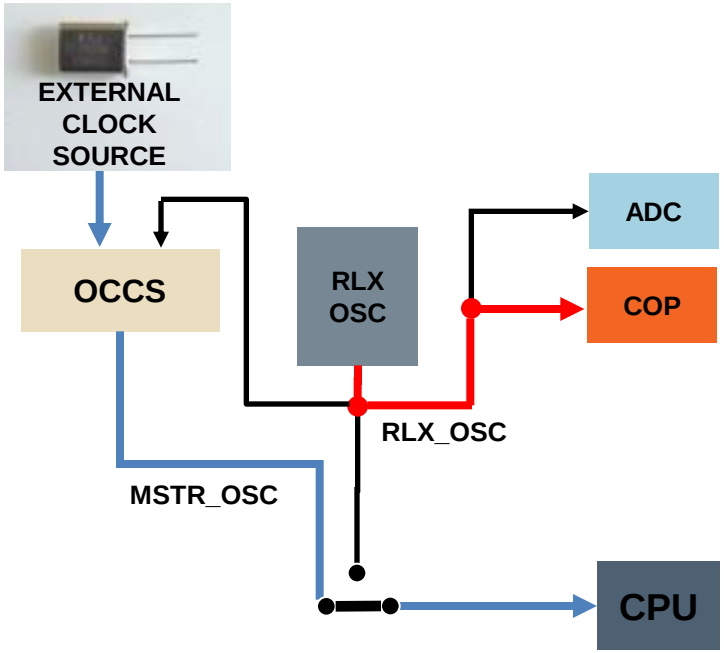
COP and Power Supervisor

- **Computer Operating Properly**
  - Free-running down counter that resets the device once the terminal count has been reached
  - Can be used as a mechanism for recovering from errant software.
  - Has an associated reset vector in the interrupt vector table
  - Allows COP Resets to be handled differently than Hardware or Software Resets.
  - Features write-protectible registers for added protection.
  - Capable of selecting different clock sources to prevent primary clock failure caused safety concerns
  - The service procedure consists of writing $5555 followed by $AAAA to the CNTR register.

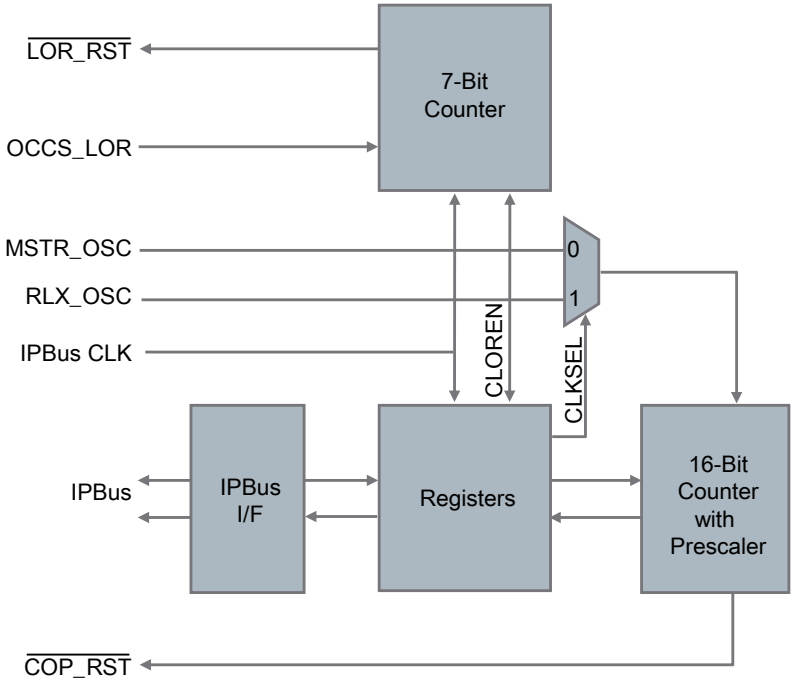
- **Power Supervisor**
  - Holds device in reset until there is enough voltage (VDD > 1.8V) for on-chip logic to operate at the oscillator frequency
    - *Precludes any problems associated with false restart*
  - Low Voltage detectors generate high-priority interrupts
    - *Two low voltage detect signals used to initiate a software controlled shutdown when the supply voltage drops below acceptable either 2.2V or 2.7V levels*
  - Eliminates need for external power monitor

COP Basics

- Independently clocked watchdog



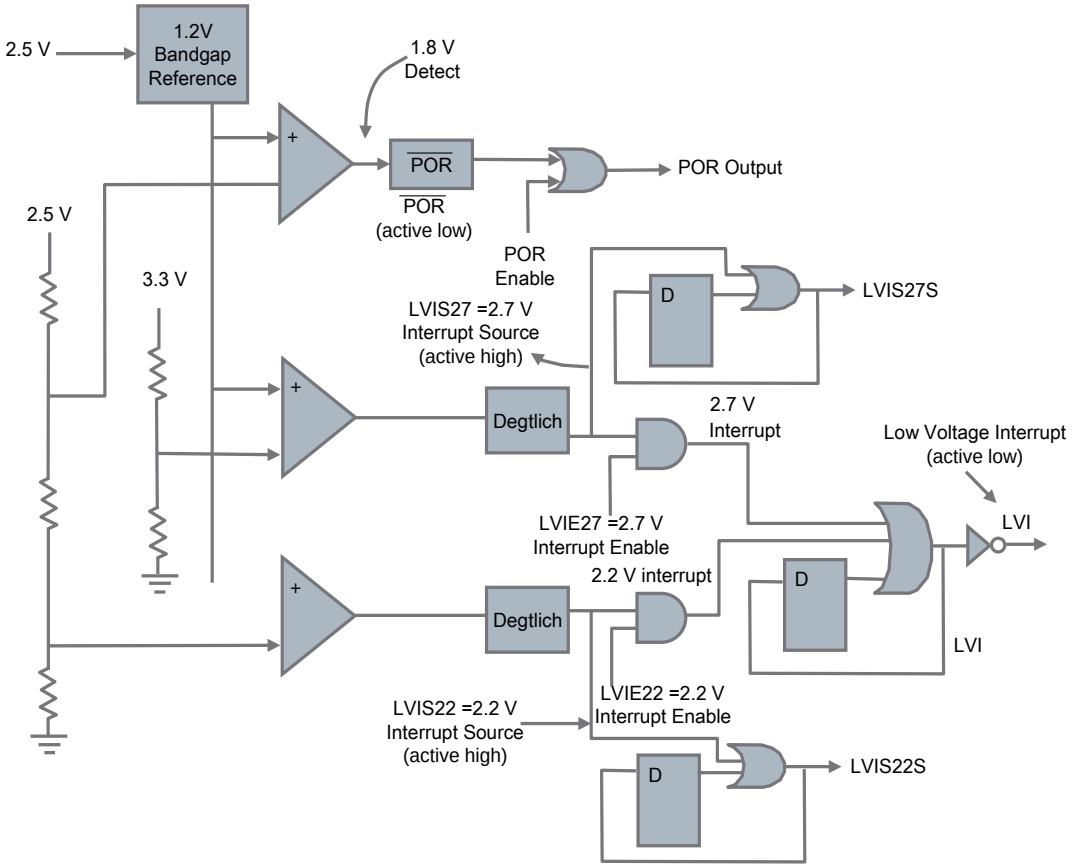
- Block diagram



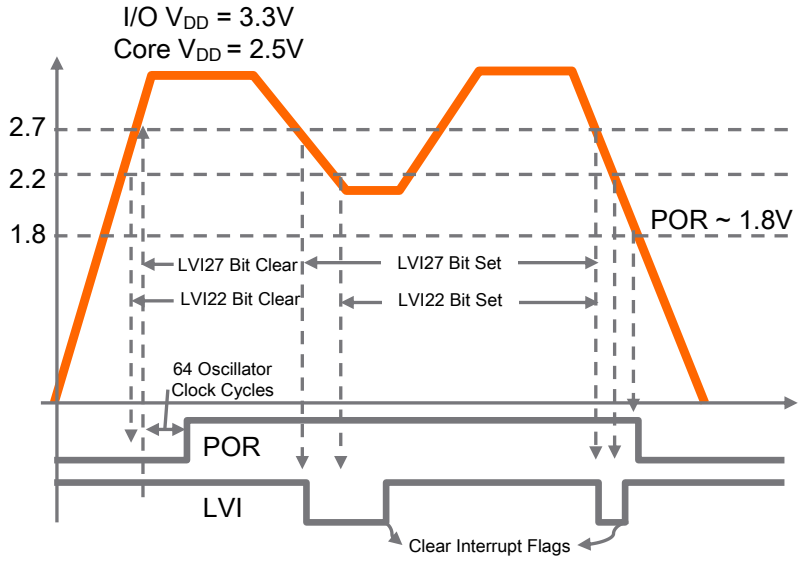
- **Option to use independent RC relaxation oscillator (RLX_OSC) for COP**
- **CPU is clocked from MSTR_CLK (External Clock Source)**
- **COP can be clocked from MSTR_CLK or RLX_OSC**
- **If OCCS selects RLX_OSC for MSTR CLK, then both COP and CPU CLKS are the same source**

Power Supervisor - Block Diagram

- Block Diagram



- Power Supervisor Operation



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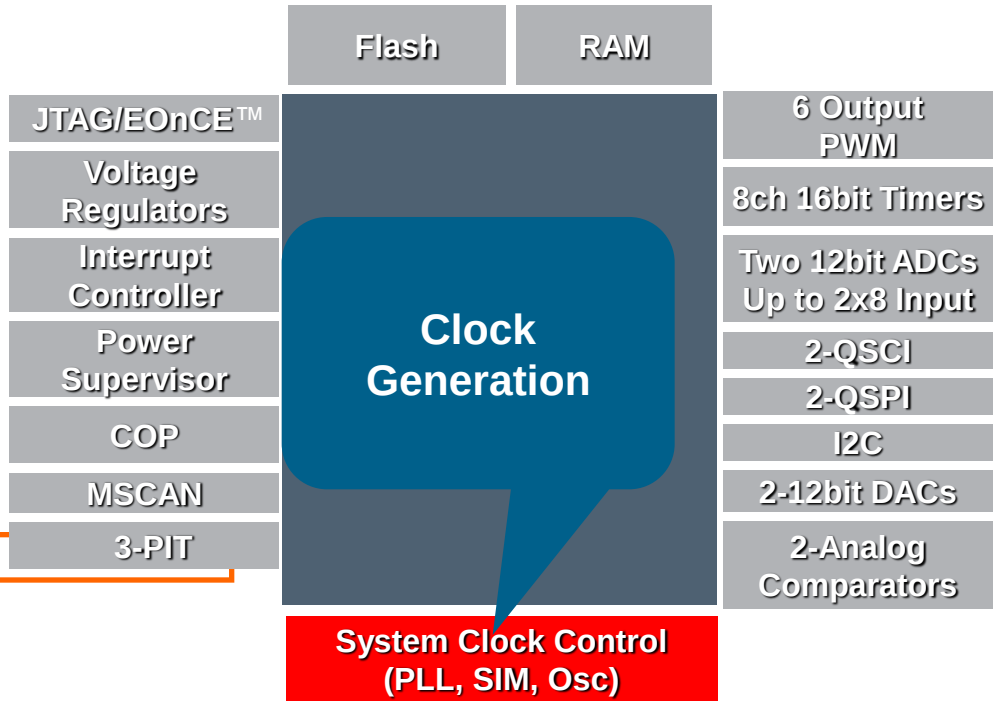
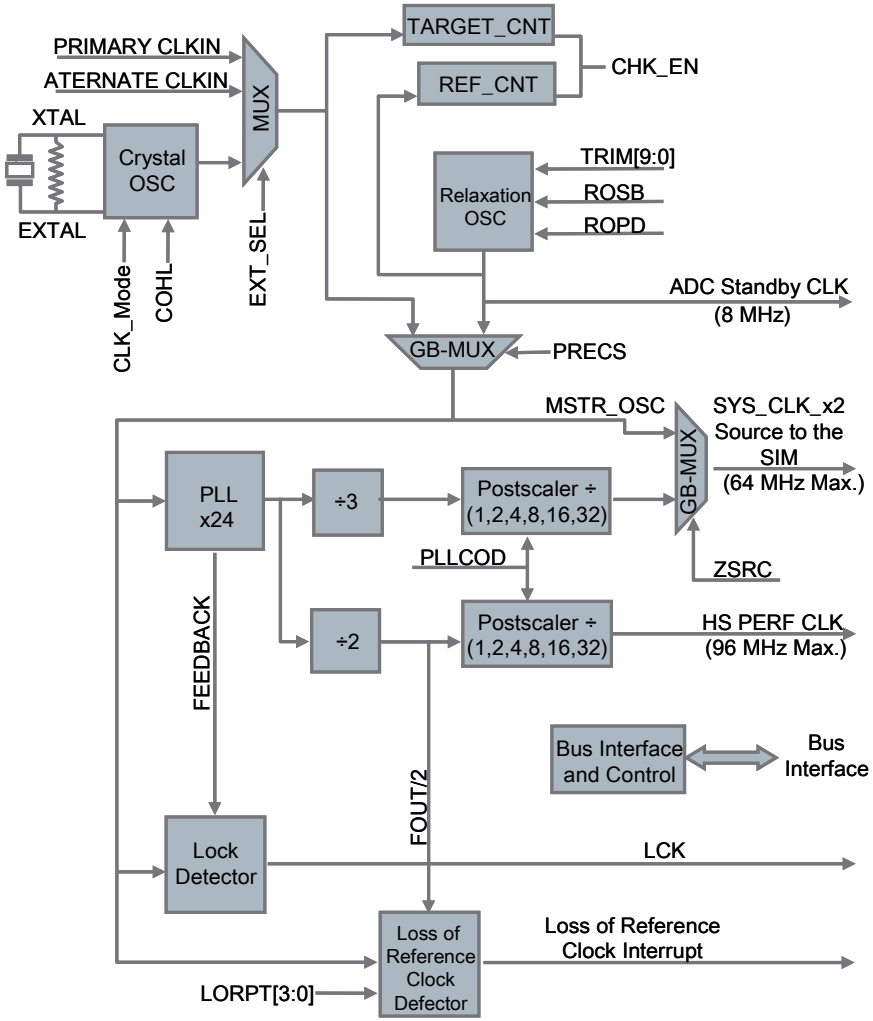


PLL and Clock Generation

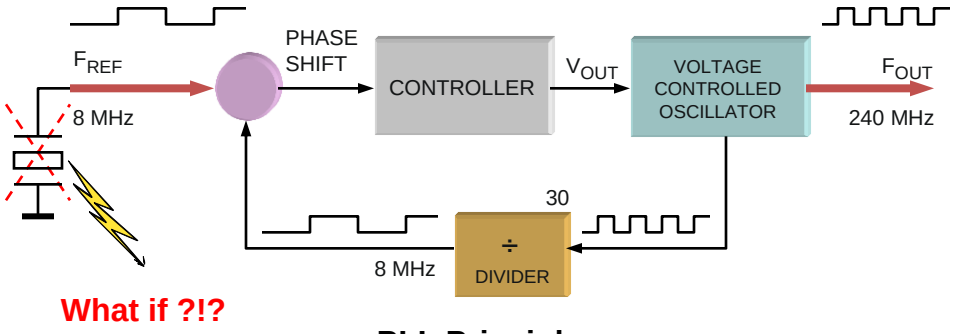
- On Chip Clock Synthesis (OCCS)
- Clock Source
  - *On Chip Relaxation Oscillator*
  - *External Clock*
- Ability to power down internal relaxation oscillator or crystal oscillator
- Ability to put the internal relaxation oscillator into a standby mode
- Generates interrupt
  - *if either loss of clock*
  - *or loss of (PLL) lock*
  - *or both*
- Fixed System Clock generation
- 1,2,4,8,16,32 MHz
- 3,6,8,12,24,48,96 MHz
- Timer and PWM only
- System Integration Module (SIM)
- Advanced Clock Control for Low Power
- Timer, SCI, SPI, I2C, ADC, PWM enable/disable
- Provides 3× high speed clock to timer and PWM modules
- Timer clock enable/disable in STOP
- SCI clock enable/disable in STOP

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)	fosc	4	8	8	MHz
Internal reference relaxation oscillator frequency for the PLL	fosc		8		MHz
PLL output frequency2 (24 x reference frequency)	fop	96	192		MHz
Relaxation Oscillator output frequency Normal Mode Standby Mode	 fop		 8.05 200		MHz
Relaxation Oscillator stabilization time	troscs		1	3	ms
Variation over temperature 0°C to 105ºC			0 to +1	+/-2.0	%

PLL and Clock Generation - Block Diagram

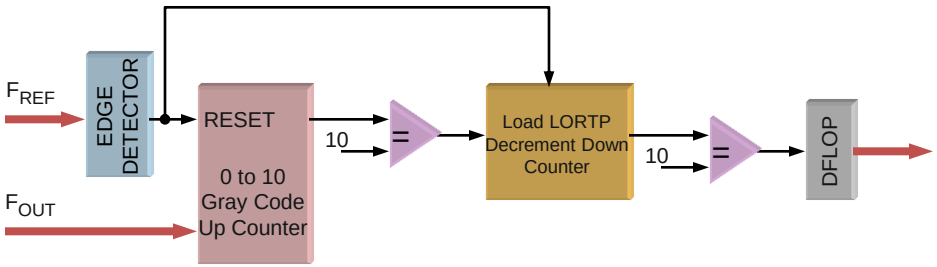


OCCS - Safety



What if ?!?

PLL Principle



Simplified Block Diagram, Loss of Reference Clock Detector

Interrupt	Source	Description
LOLI1	PLLSR	Lock 1 Interrupt
LOLI0	PLLSR	Lock 2 Interrupt
LOCI	PLLSR	Loss of Reference Clock Interrupt

Interrupt Summary

- ✓ **PLL Lock Detector**
- ✓ The detector starts two counters whose outputs are periodically compared. The input clocks to these counters are the VCO output clock divided by the value in the PLLDB field of the PLLCR, called feedback, and the PLL input clock.
- ✓ Feedback and FREF clocks are compared after 16, 32, and 64 cycles. If, after 32 cycles, the clocks match, the LCK0 bit is set to one. If, after 64 cycles of FREF, there are the same number of FREF clocks and feedback clocks, the LCK1 bit is also set. The LCK bit stay set until:
  - ✓ Clocks fail to match
  - ✓ When a new value is written to the PLLDB-factor
  - ✓ On reset caused by LCKON, PLL_ PDN
  - ✓ Chip_ level reset
- ✓ **Loss of Clock Detector**
- ✓ The loss of reference clock detector is designed to generate an interrupt when the reference clock to the PLL is interrupted.
- ✓ For instance, this might occur if the external crystal is suddenly physically damaged. An LOR interrupt should occur after LORTPx10xPLL-clock-time-periods.
- ✓ LOR detector, relying on the phase locked loop can continue running for a time after its reference clock has been disturbed. This provides time for detection of the problem and an orderly system shutdown.

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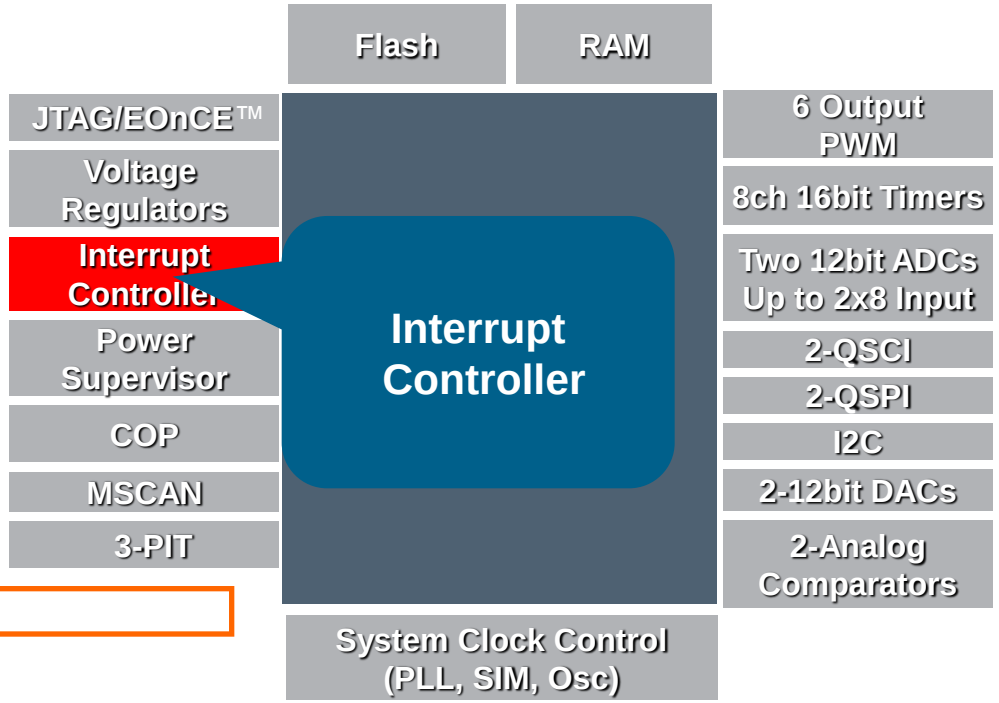
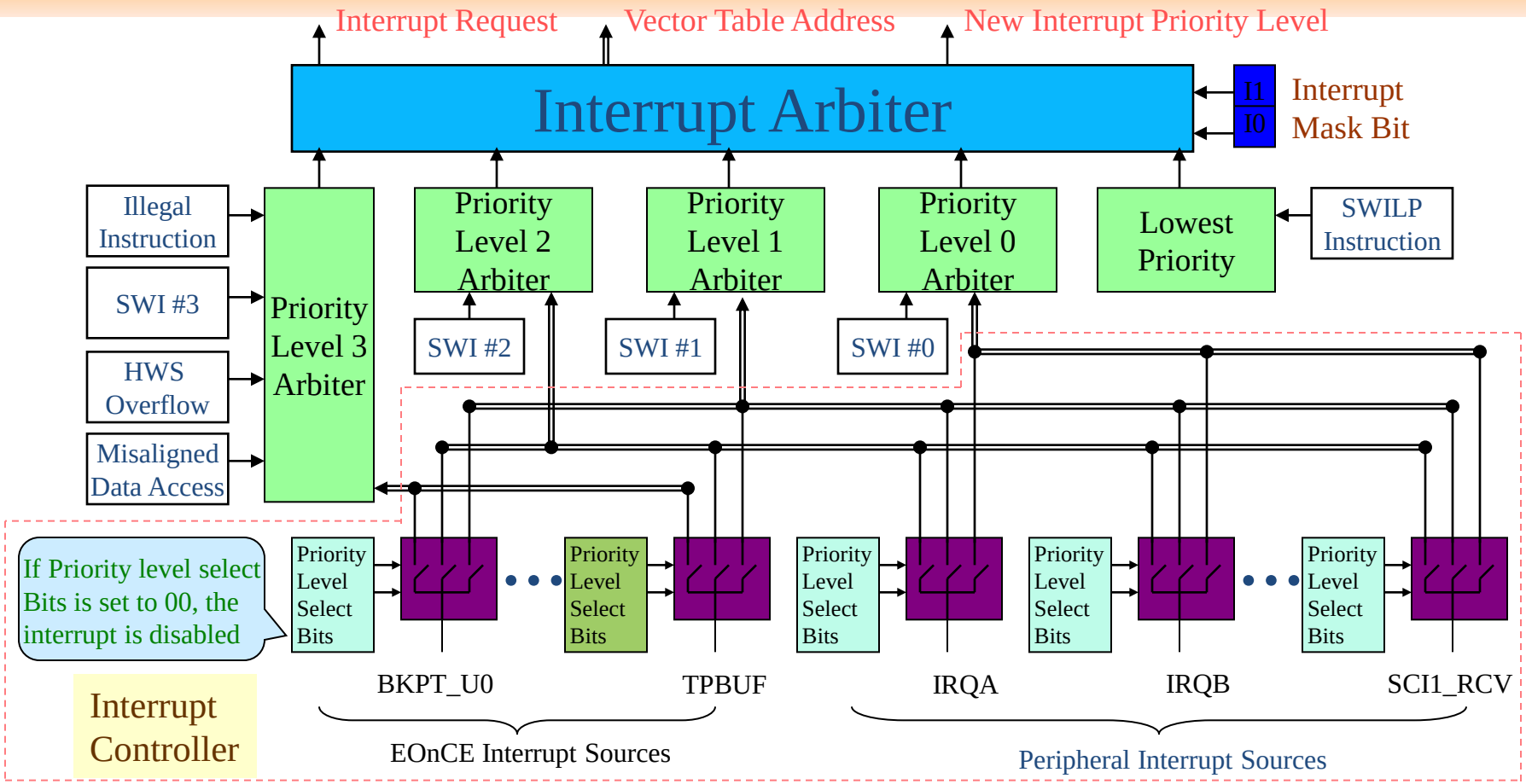


Interrupt Controller - ITCN

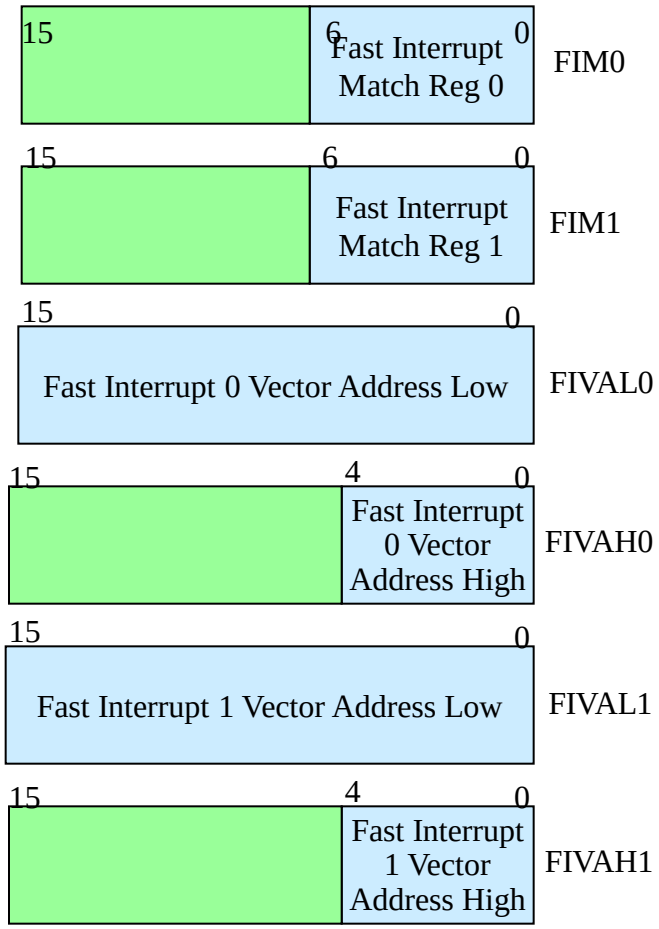
- Arbitrates peripheral interrupt requests
- Signals core when an interrupt of sufficient priority exists
- Provides ISR address to service each interrupt
- Relocatable Interrupt Vector Table
- Supports 128 interrupt sources
- Supports 5 interrupt priority levels with HW nesting
  - *Level 3 (highest) for core interrupts*
  - *Level 2, 1, and 0 for peripherals*
  - *Level -1 (lowest for SW interrupt)*
- Two programmable Fast Interrupts
  - *Available for level 2 interrupts*
  - *Dedicated context registers: R0, R1, N, M01, Y, FIRA, and FISR*
  - *Lower latency*
- Notification of SIM module to restart clocks out of Wait and Stop modes
- Drives initial address on the address bus after reset

Standard Interrupt - Basics



- EOnCE Interrupt Sources can be assigned to priority level 3, 2, and 1.
- Peripheral Interrupt sources can be assigned to priority level 2, 1, and 0.
- Any interrupt sources can interrupt Lowest-Priority Software Interrupt (SWILP interrupt).

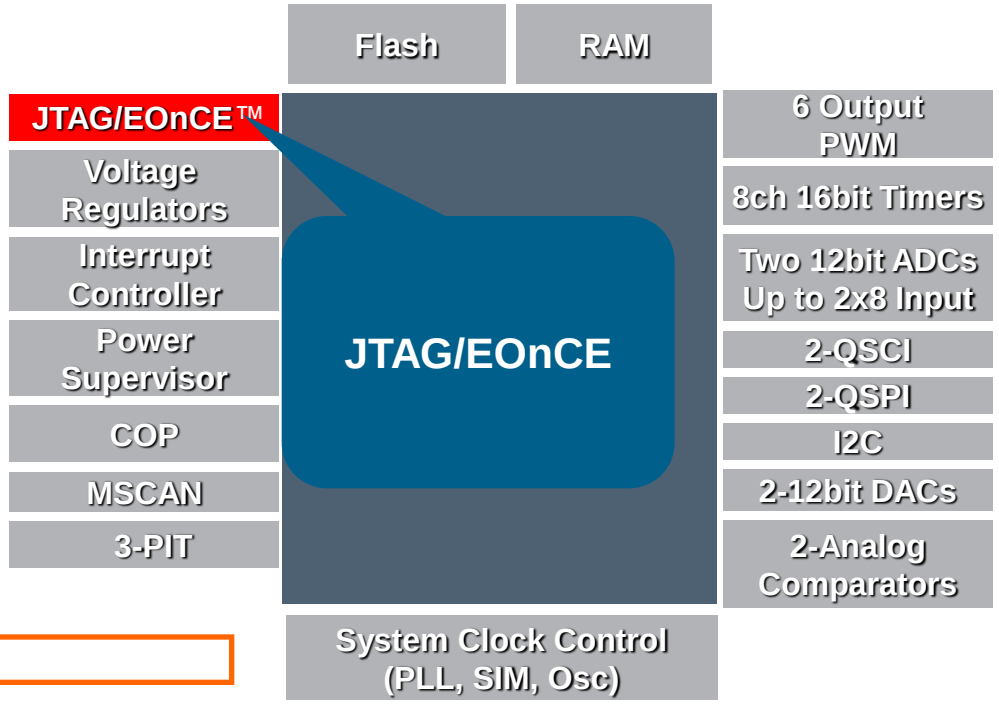
Fast Interrupt - Basics



- Two Fast Interrupt Match Registers (FIM0, FIM1) in 568000 declare which two IRQs will be Fast Interrupts
- Fast Interrupts vector directly to a service routine based on values in the Fast Vector registers without having to go to Vector table
- Interrupt sources used as fast interrupts must be set to priority level 2
- Fast Interrupt 0, declared in FIM0 has priority over fast interrupt 1.
- The first instruction words in a fast ISR cannot contain an instruction that accesses program memory
- The following instructions are not allowed in first four instructions of a fast ISR
  - JSR, BSR, RTS, RTSD, RTI, RTID
  - BRA, BRAD, Bcc, JMP, JMPD
  - STOP, WAIT, DEBUGHT
  - DEBUGEV when programmed to halt the core
  - SWI, SWI #n, SWILP, ALLGNSP
  - REP, DO, DOSLC

• MC56F8023/56F8025/56F8036/56F8037

- Flash Memory
- Pulse Width Modulator
- Quad Timer
- Analog to Digital Converter
- Digital to Analog Converter
- Analog Comparator
- PIT Timer
- MSCAN Module
- QSCI Module
- QSPI Module
- I2C Module
- General Purpose I/O (GPIO)
- COP and Power Supervisor
- PLL and Clock Generation Module
- Interrupt Controller (ITCN)
- Debugging Unit



Debugging Unit

- Frequency of operation SYS_CLK/8 (4MHz)
- Accessed through a common IEEE JTAG interface
- EOnCE allows access to registers, memories and on-chip peripherals
- Retains debug control in target system
- System Level Debugging at one of 3 levels:
- Non-intrusive Real-time Debug
- Minimally Intrusive Real-time Debug
- Breakpoint and Step Mode - Core is halted
- Data Upload / Download through the JTAG port
- Advanced Breakpoint Capability
- Trace one or more Instructions
- Change of Flow Buffer
- Event Viewing through a terminal
- Resources accessible through JTAG or through the Core
- All JTAG Pins are muxed wit GPIOs

Thank you