EVROPSKÁ UNIE
MINISTERSTVO ŠKOLSTVÍ, MLÁDEŽE A TĚLOVÝCHOVY
OP Vzdělávání pro konkurenceschopnost
VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

Mikroprocesorová technika v aplikacích řízení elektrických pohonů

Ing. Jaroslav Lepka
Ing. Pavel Grasblum, Ph.D.

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Tato prezentace je spolufinancována Evropským sociálním fondem a státním rozpočtem České republiky.

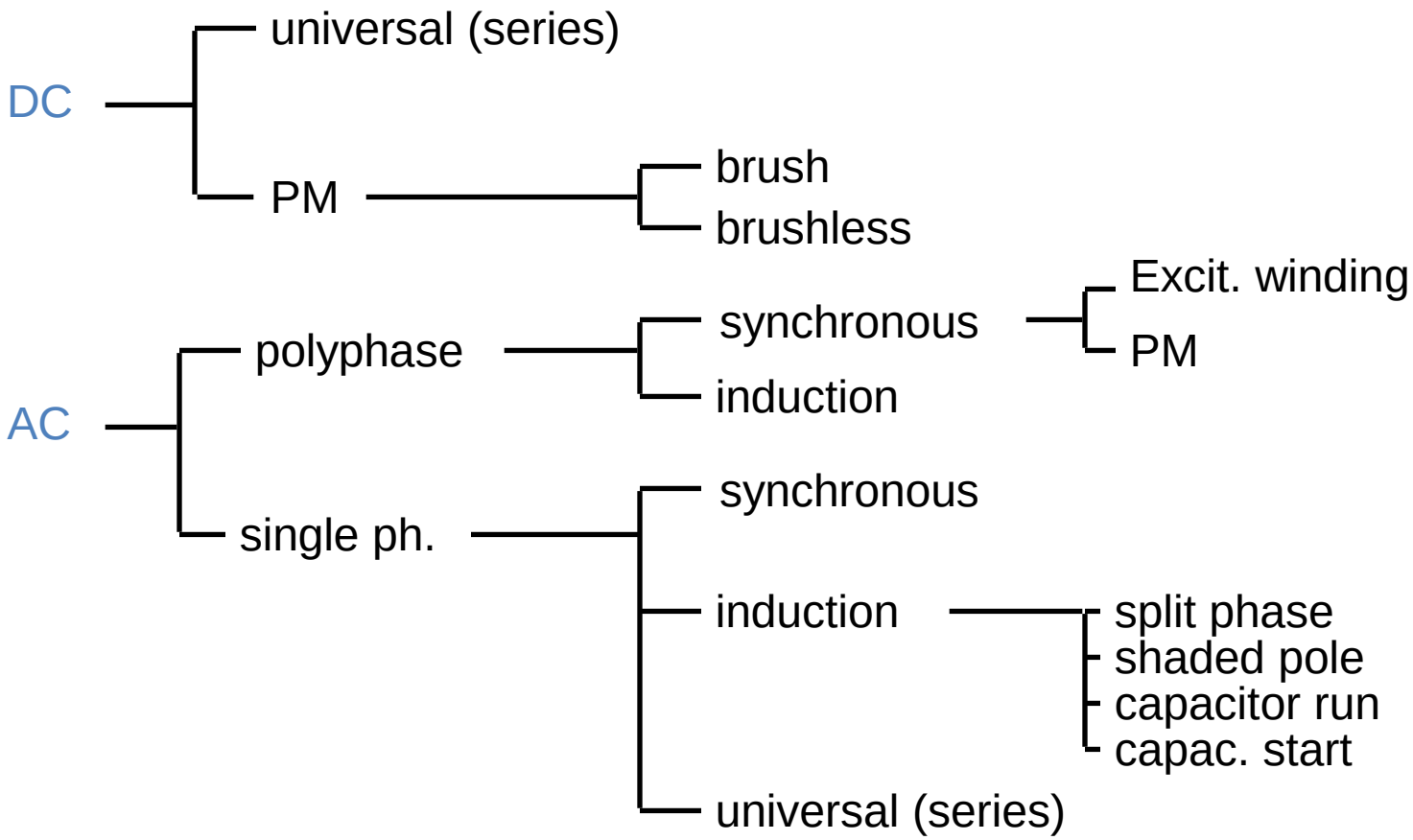
Agenda

- Separately exited DC motor
- Basic Terms
- PWM Modulation techniques for DC and BLDC drives
- BLDC Motor Theory
- Microcontroller MC56F8006

Agenda

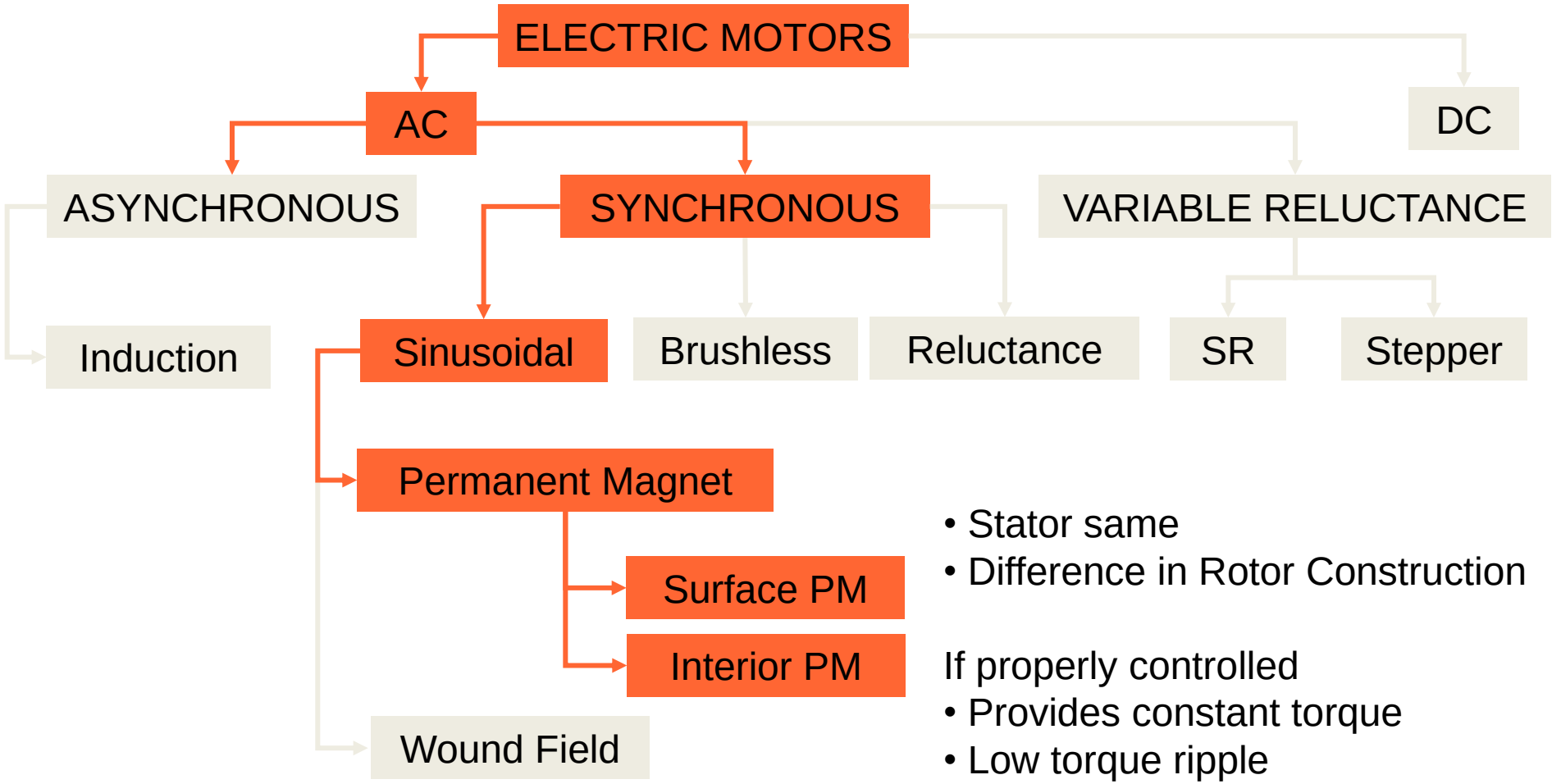
- Separately exited DC motor
  - Motors clasification
  - Separately excited DC motor theory
- Basic Terms
- PWM Modulation techniques for DC and BLDC drives
- BLDC Motor Theory
- Microcontroller MC56F8006

Electric Motor Type Classification



Stepper & Switched Reluctance

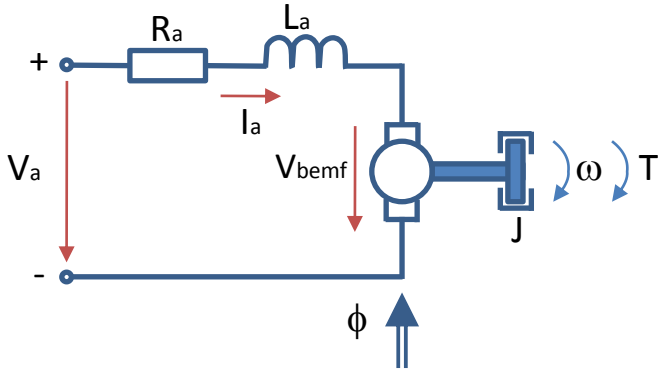
Electric Motor Type Classification



- Stator same
- Difference in Rotor Construction

If properly controlled
- Provides constant torque
- Low torque ripple

Separately Excited DC Motor



Equation describing dynamics of electric circuit

$$V_a = R_a \cdot I_a + L_a \cdot \frac{dI_a}{dt} + V_{bemf}$$

State equations – motor dynamics

$$\frac{dI_a}{dt} = \frac{1}{L_a} \cdot \left(V_a - R_a \cdot I_a - V_{bemf}\right)$$

$$\frac{d\omega}{dt} = \frac{1}{J} \cdot \left(T - T_L\right)$$

Steady state operation

$$V_a = R_a \cdot I_a + V_{bemf}$$

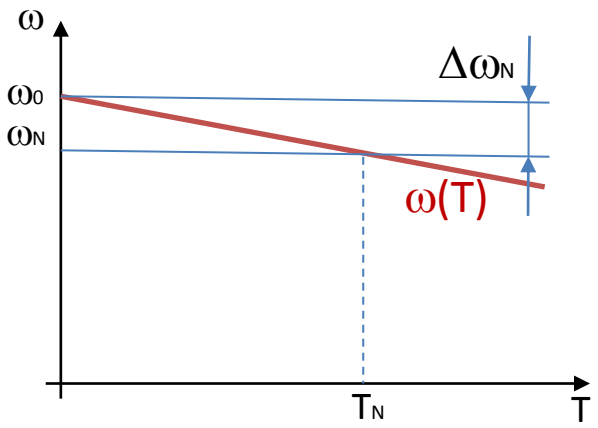
$$\omega = \frac{V_a}{c \cdot \phi} - \frac{R_a}{\left(c \cdot \phi\right)^2} \cdot T$$

$$\omega_{0N} = \frac{V_{aN}}{c \cdot \phi}$$

$$\Delta\omega_N = \frac{R_a}{\left(c \cdot \phi\right)^2} \cdot T$$

$$V_{bemf} = c \cdot \phi \cdot \omega$$

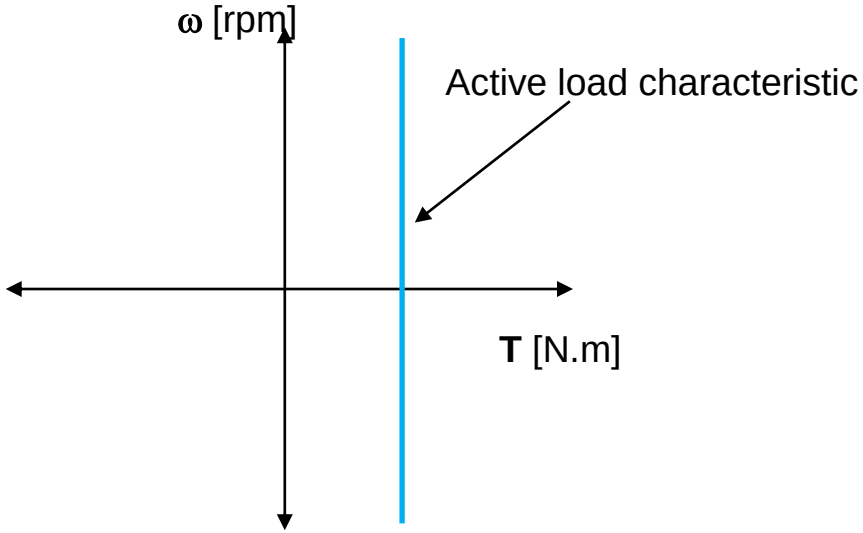
$$T = c \cdot \phi \cdot I_a$$



Agenda

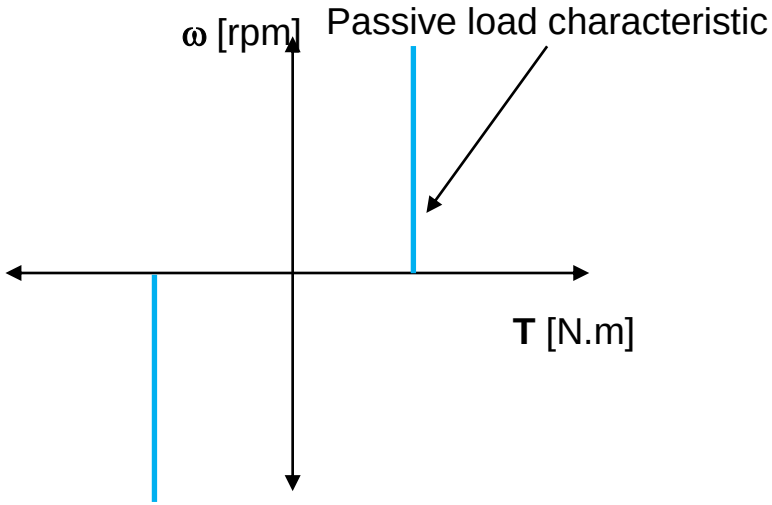
- Separately exited DC motor
- Basic Terms
  - Operational Characteristic of the Drive
  - Unipolar versus Bipolar Switching
  - Independent versus Complementary Switching
  - Edge versus Centre Aligned PWM
- PWM Modulation techniques for DC and BLDC drives
- BLDC Motor Theory
- Microcontroller MC56F8006

Mechanical Characteristics of the Motor Load

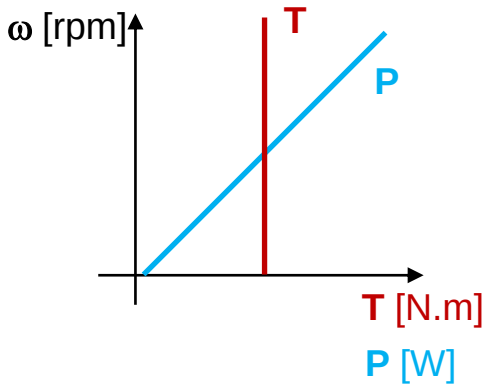


- Active load characteristic
  - Mechanisms with change in the potential energy
  - When the speed changes the direction the active load remains unchanged – sign of torque is unchanged
  - Typically – springs, lifts, crane, etc.

- Passive load characteristic
  - When the speed changes the direction the passive load changes direction as well – sign of torque changes
  - Typically – fans, friction, machining, etc.



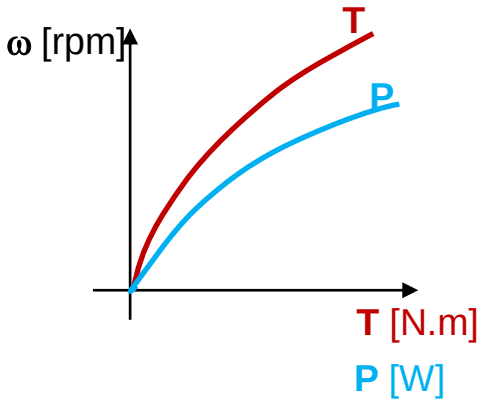
Example of Mechanical Characteristics of Motor Loads



Mechanical characteristics of a crane

$$T = \operatorname{sgn}\omega \cdot c_1$$

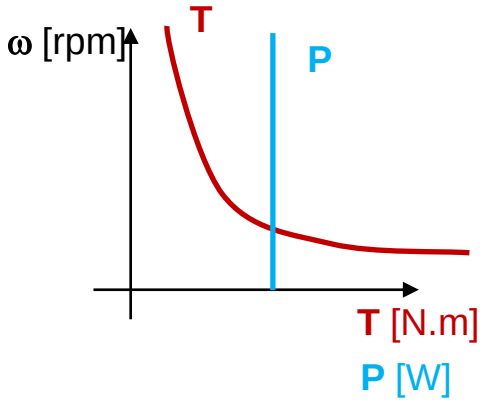
$$P = T \cdot \omega = \operatorname{sgn}\omega \cdot c_1 \cdot \omega$$



Mechanical characteristics of a fan

$$T = \operatorname{sgn}\omega \cdot c_2 \cdot \omega^2$$

$$P = \operatorname{sgn}\omega \cdot c_2 \cdot \omega^3$$

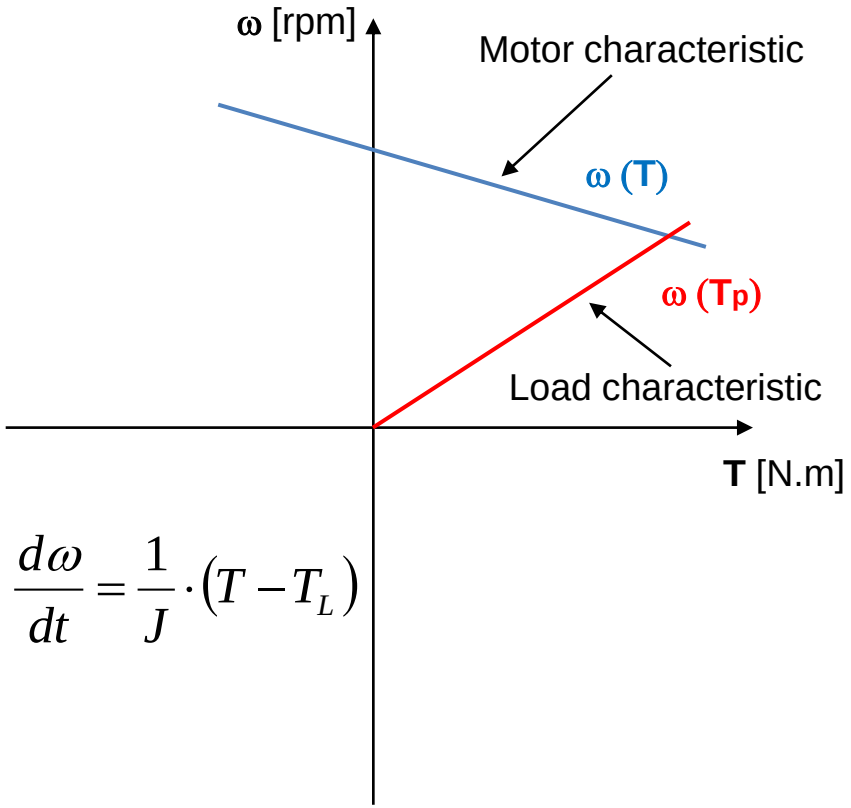


Mechanical characteristics of a reeler

$$T = \operatorname{sgn}\omega \cdot c_3 \cdot \frac{1}{\omega}$$

$$P = \operatorname{sgn}\omega \cdot c_3 = const$$

Drive Operation



$$\frac{d\omega}{dt} = \frac{1}{J} \cdot (T - T_L)$$

- Mode of drive operation
  - Acceleration

$$T(\omega) - T_L(\omega) > 0$$

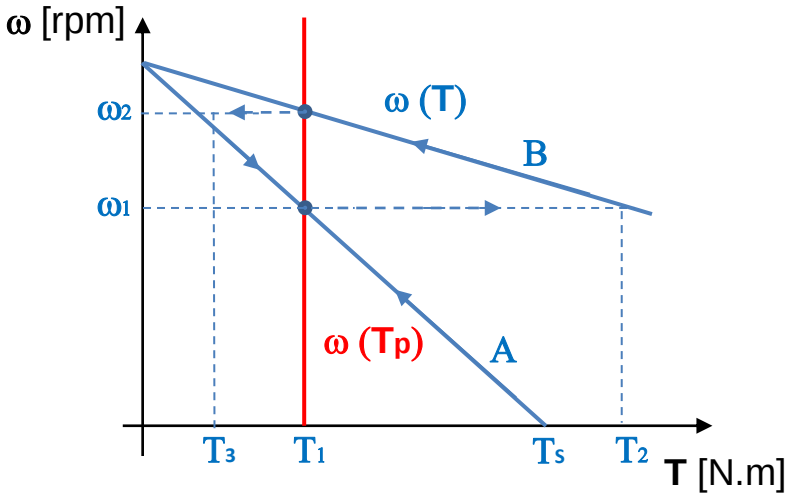
  - Deceleration

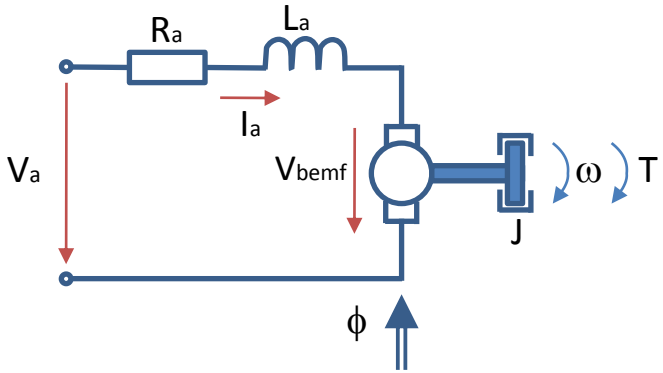
$$T(\omega) - T_L(\omega) < 0$$

  - Steady sate
    - Point of intersection between motor characteristic and Load characteristic

$$T(\omega) - T_L(\omega) = 0$$

Operational Characteristic of the Drive





$$\frac{d\omega}{dt} = \frac{1}{J} \cdot (T - T_L)$$

$$\omega = \frac{V_a}{c \cdot \phi} - \frac{R_a}{(c \cdot \phi)^2} \cdot T$$

$$\omega_{0N} = \frac{V_{aN}}{c \cdot \phi}$$

Operational Characteristic of the Drive

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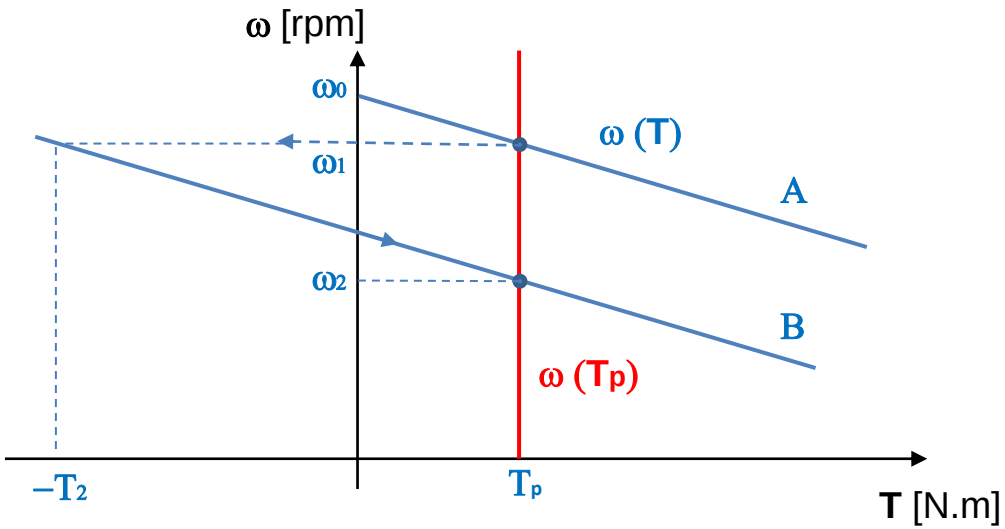
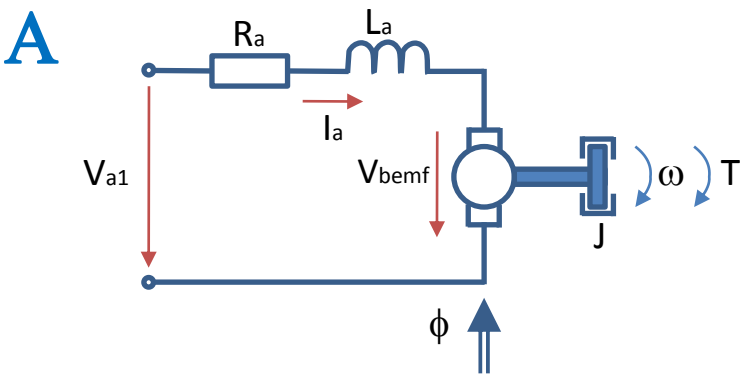
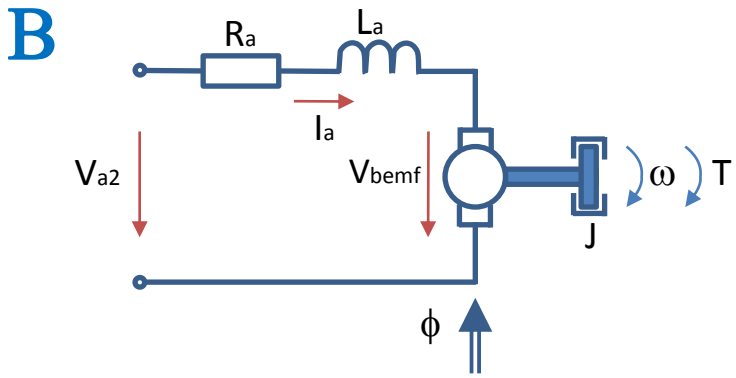
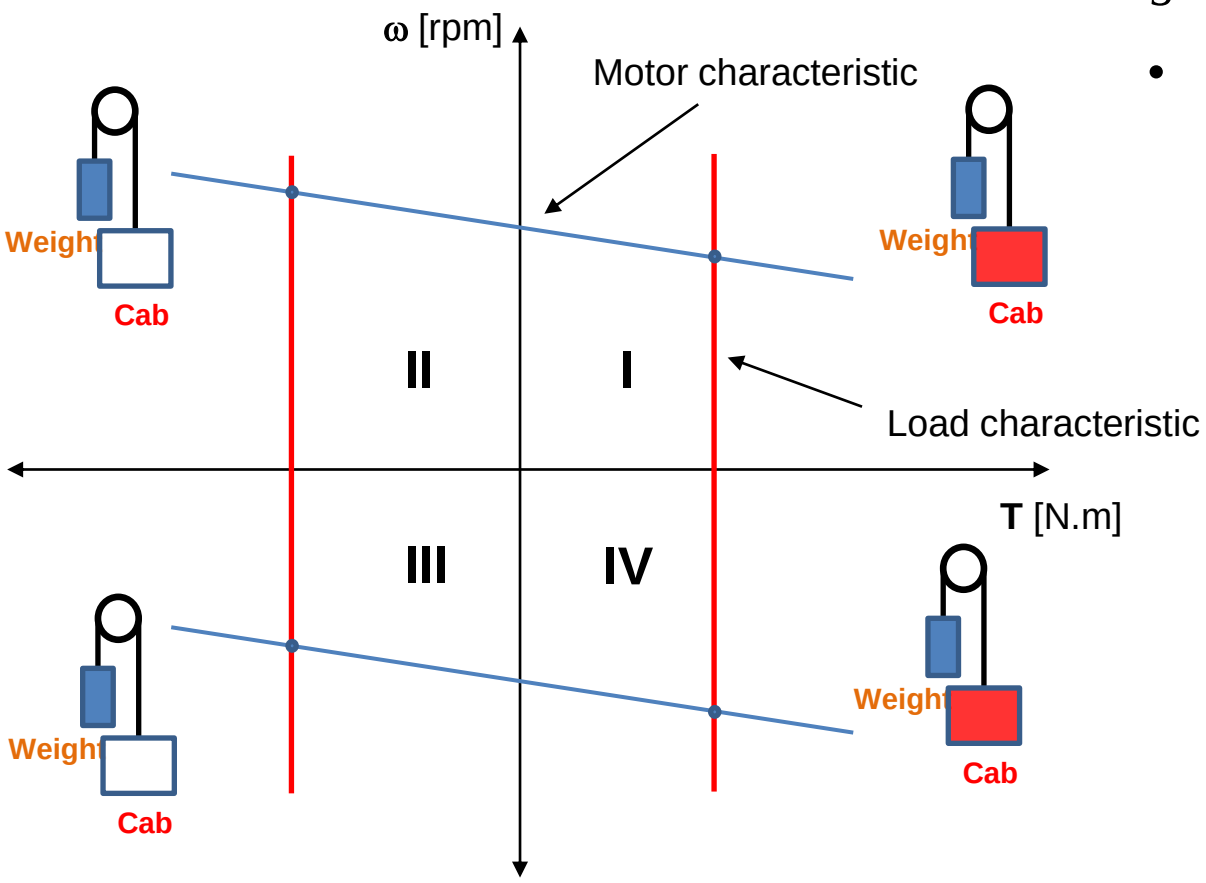






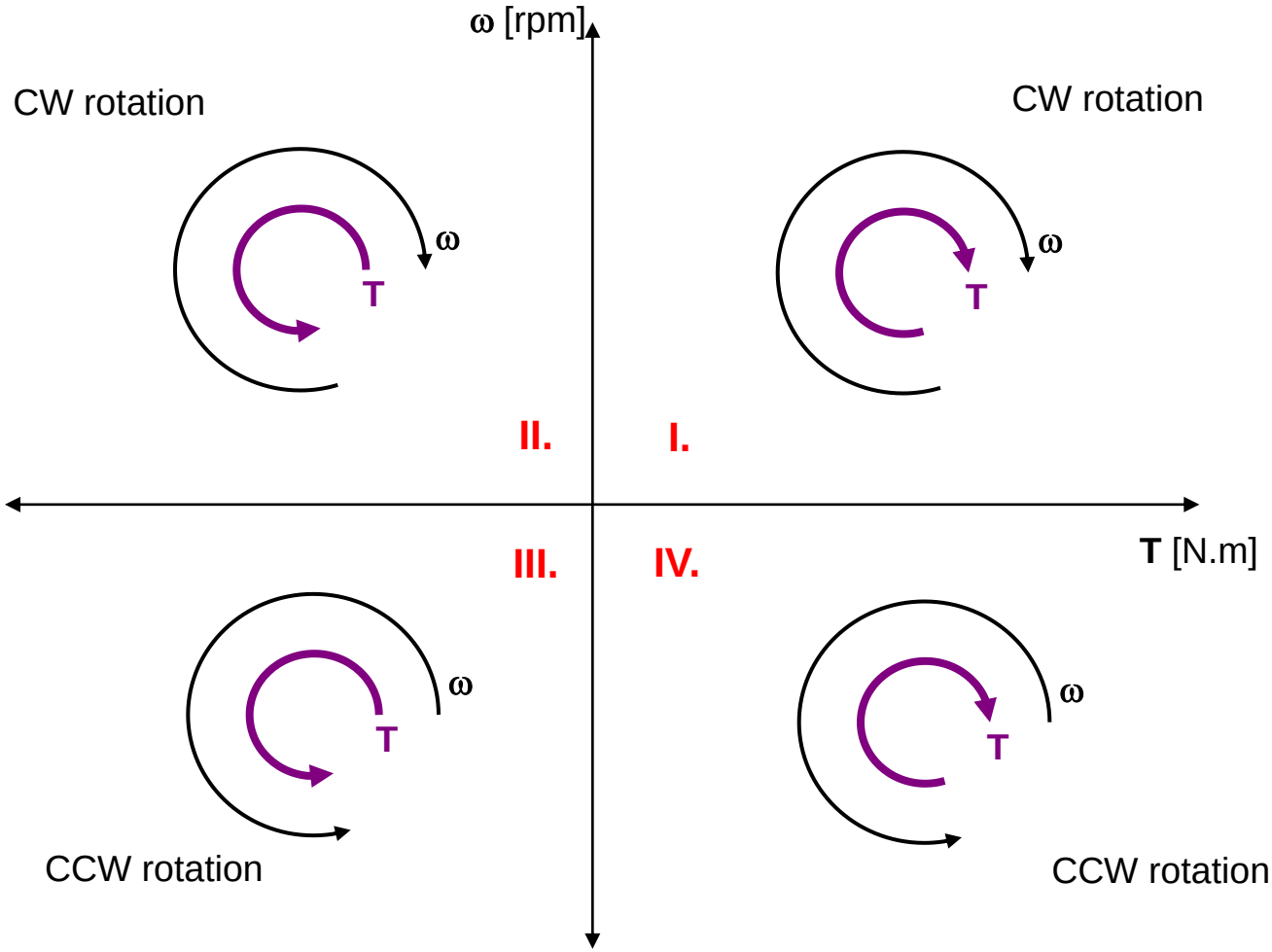
Operational Characteristic of the Drive



$$Weight = Elevator\_cage + \frac{1}{2} Load$$

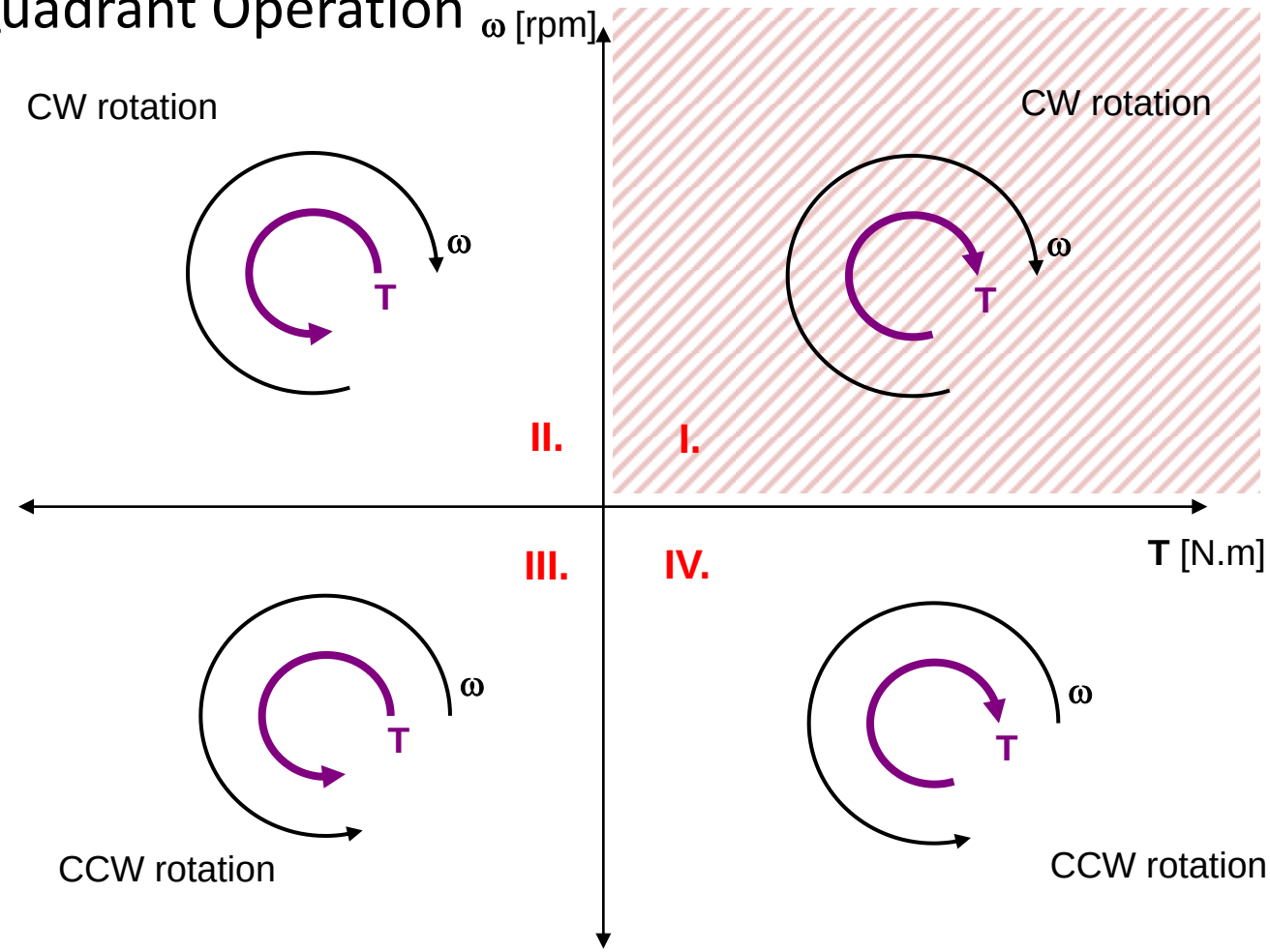
- Modes of drive operation
  - I. quadrant
    - Motor mode
    - Lift-up - full elevator cage
  - III. quadrant
    - Motor mode
    - Move-down - empty elevator cage
  - II. quadrant
    - Generator mode
    - Lift-up – empty elevator cage
  - IV. quadrant
    - Generator mode
    - Move-down - full elevator cage

Operational Characteristic of the Drive



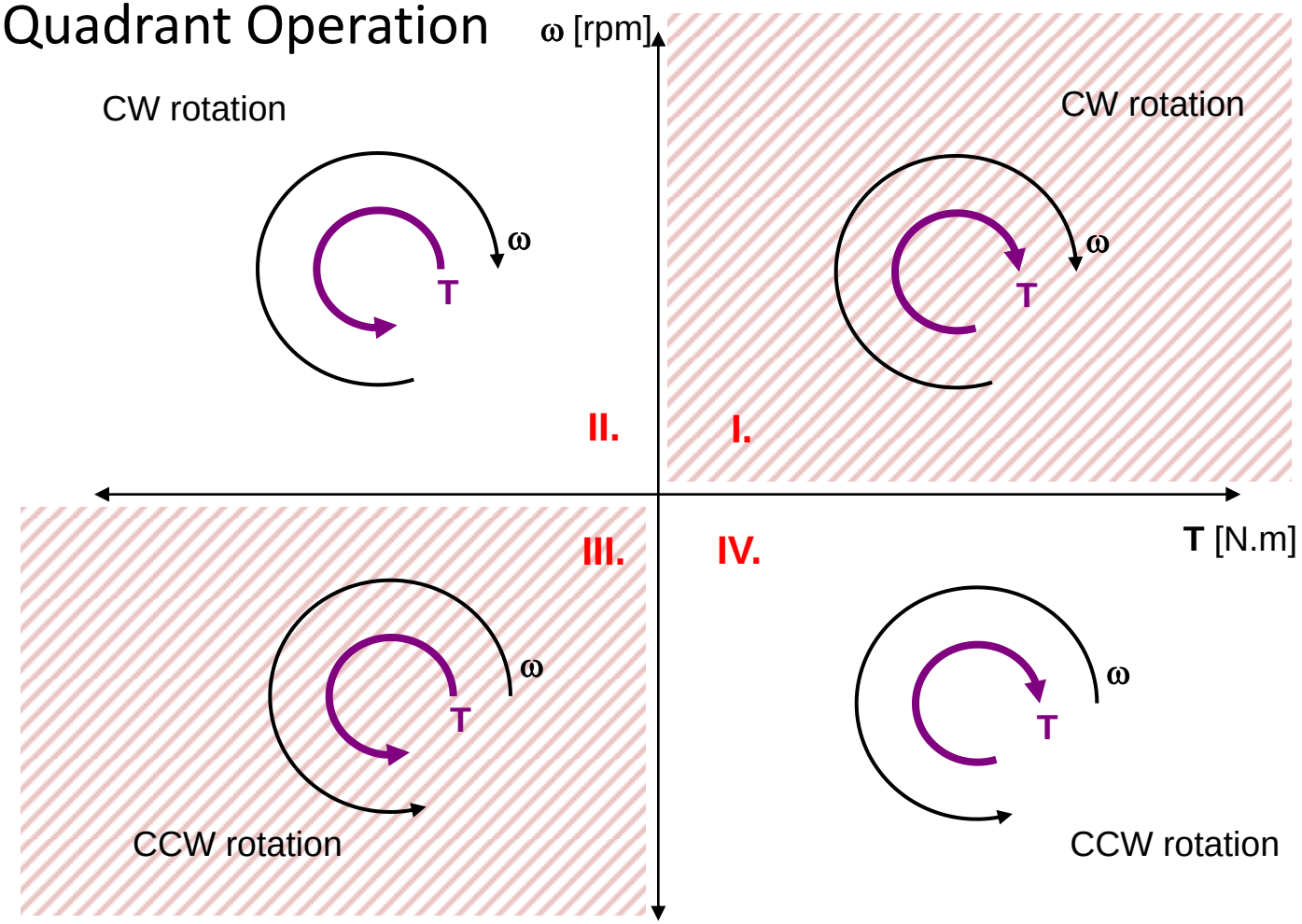
Operational Characteristic of the Drive

- Single Quadrant Operation



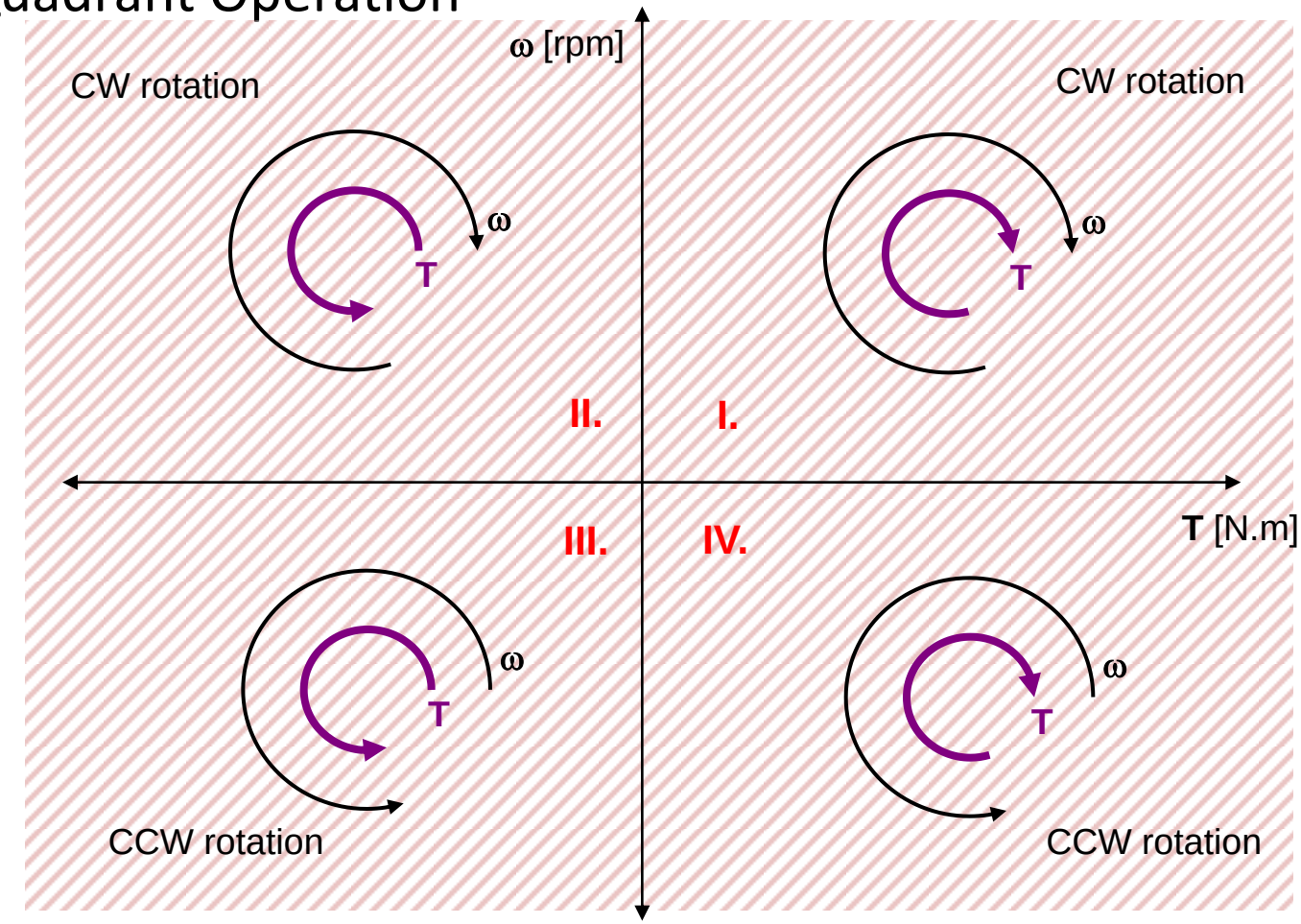
Operational Characteristic of the Drive

- Two Quadrant Operation



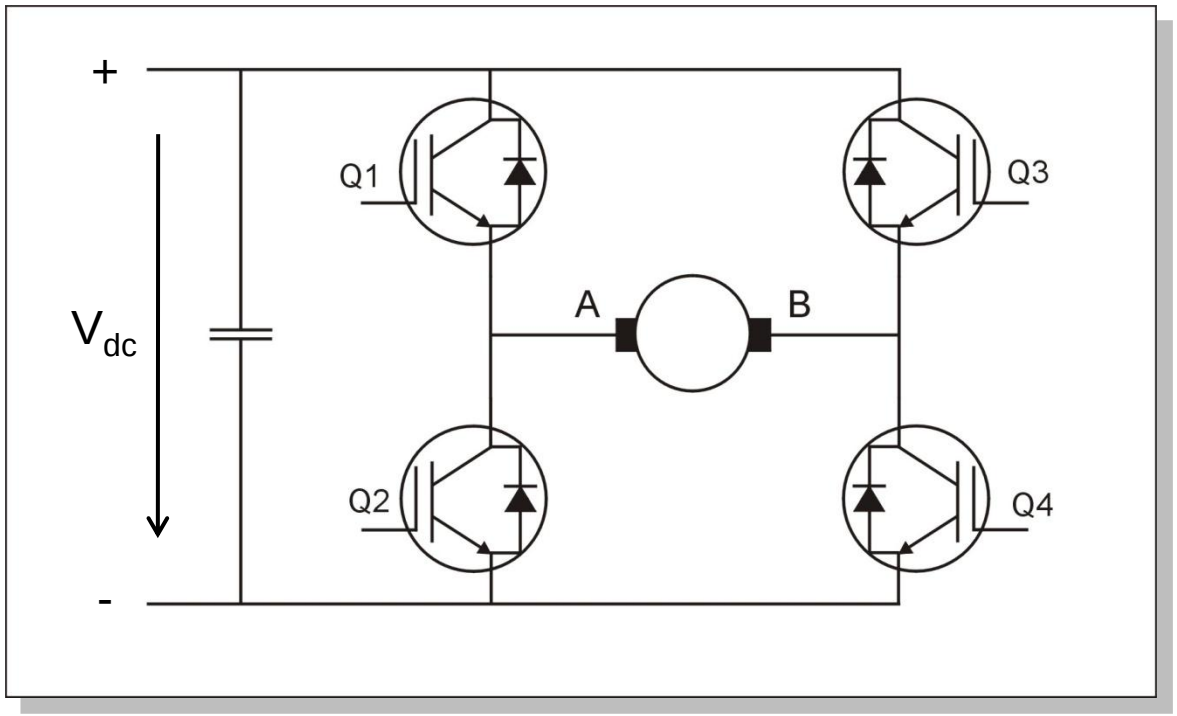
Operational Characteristic of the Drive

- Four Quadrant Operation



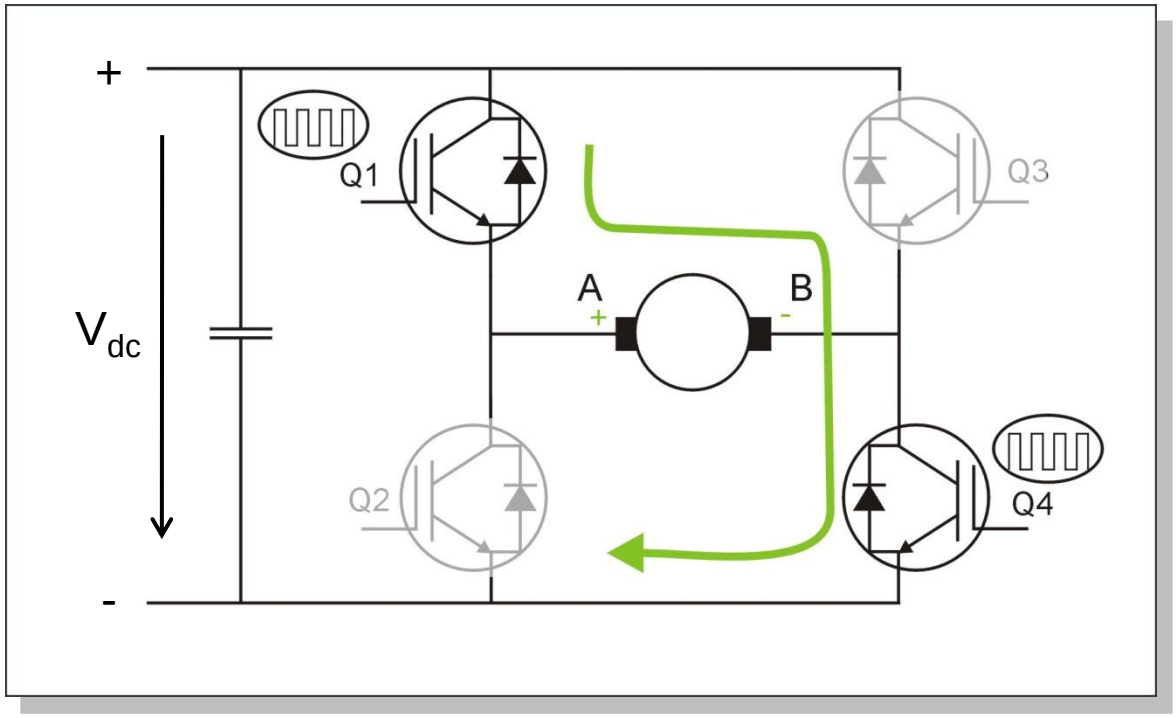
Unipolar versus Bipolar Switching

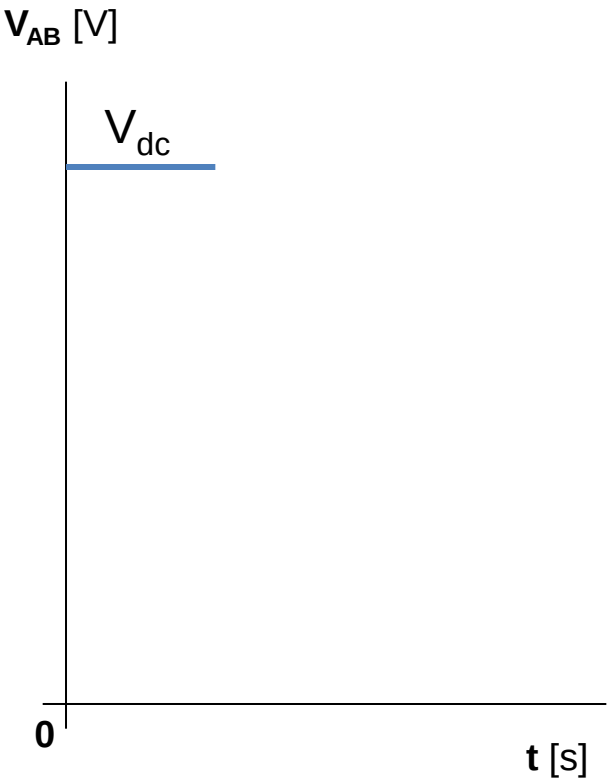
- The terms “unipolar” and “bipolar” are related to how a motor can see voltage on its terminals.



Unipolar versus Bipolar Switching

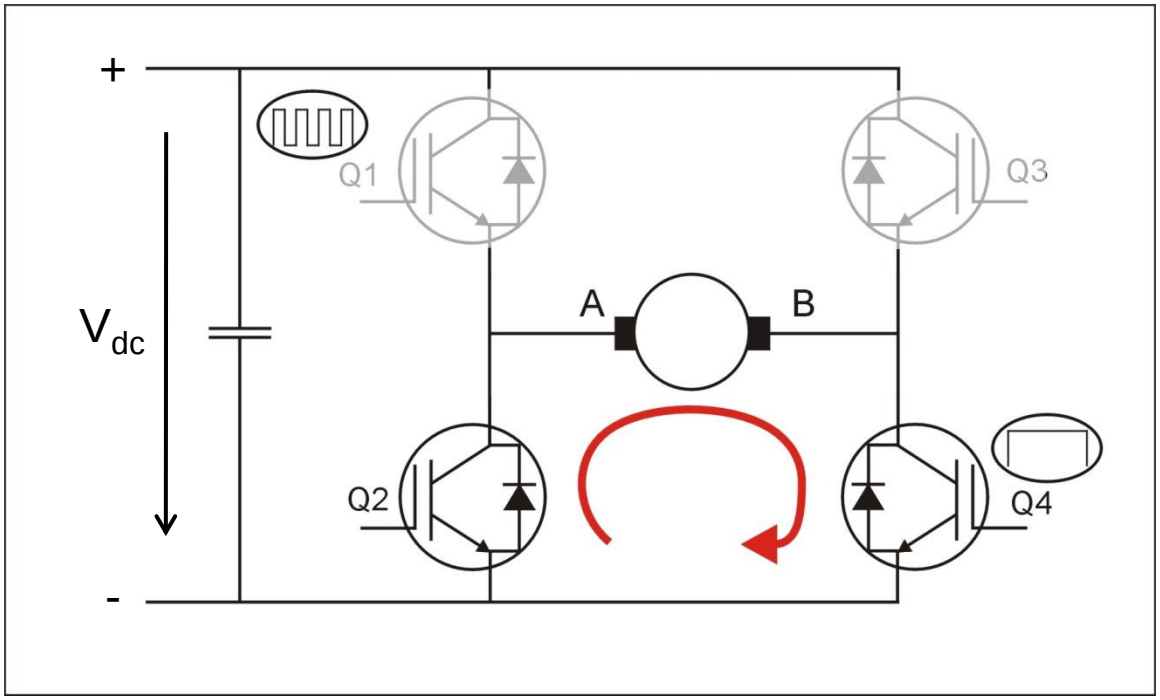
- Unipolar switching

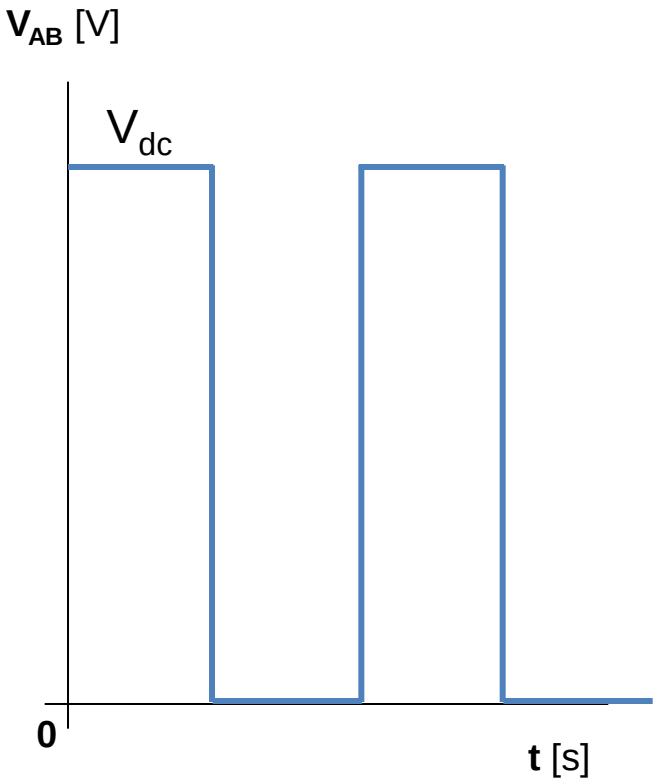




Unipolar versus Bipolar Switching

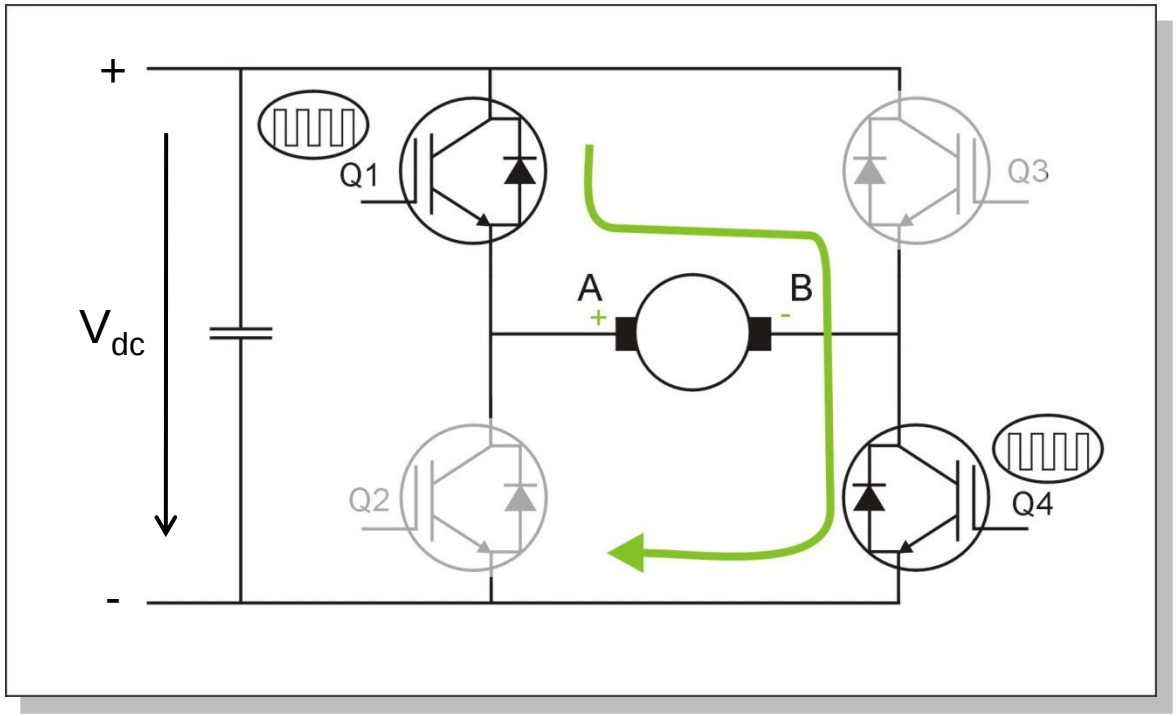
- Unipolar switching

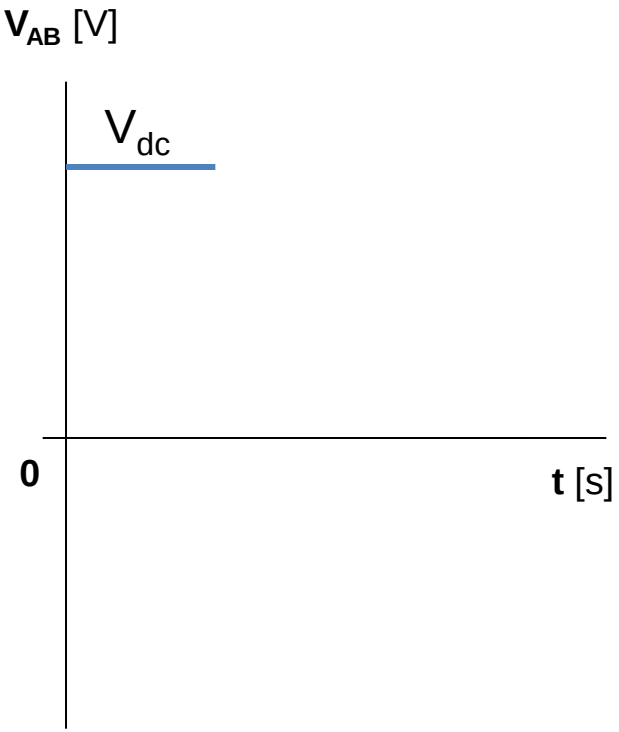




Unipolar versus Bipolar Switching

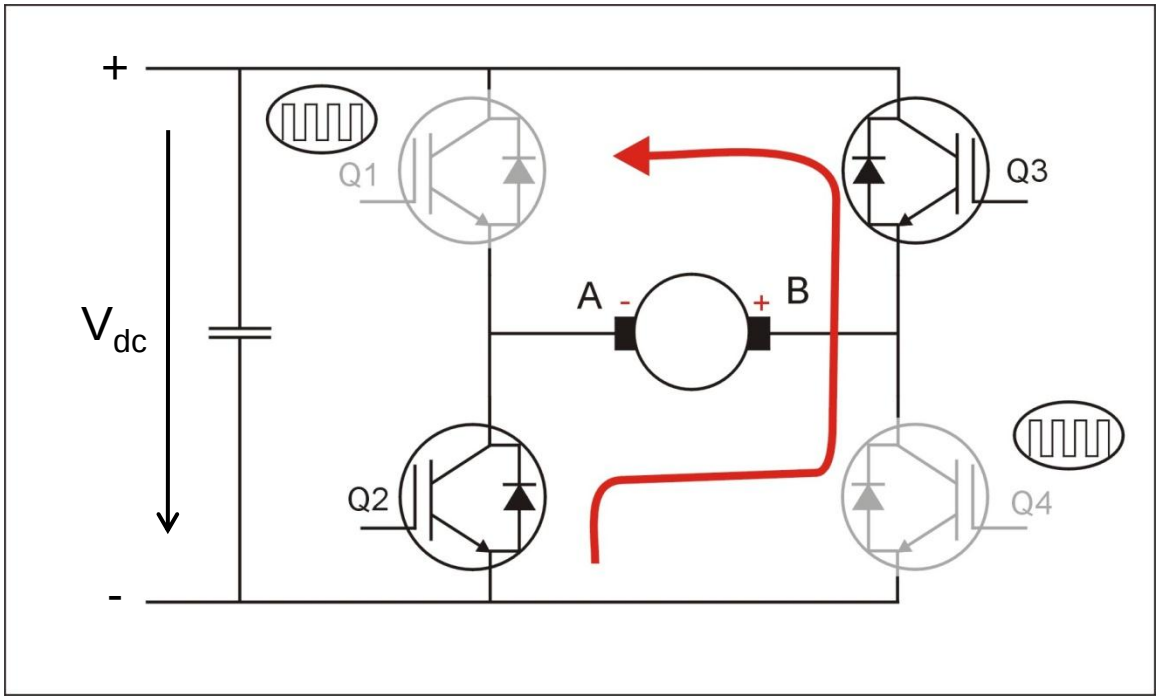
- Bipolar switching

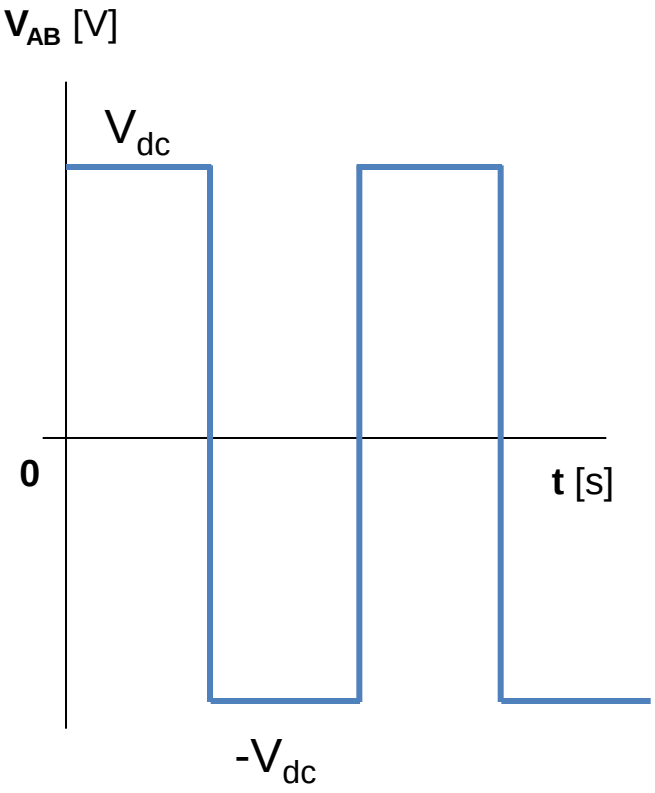




Unipolar versus Bipolar Switching

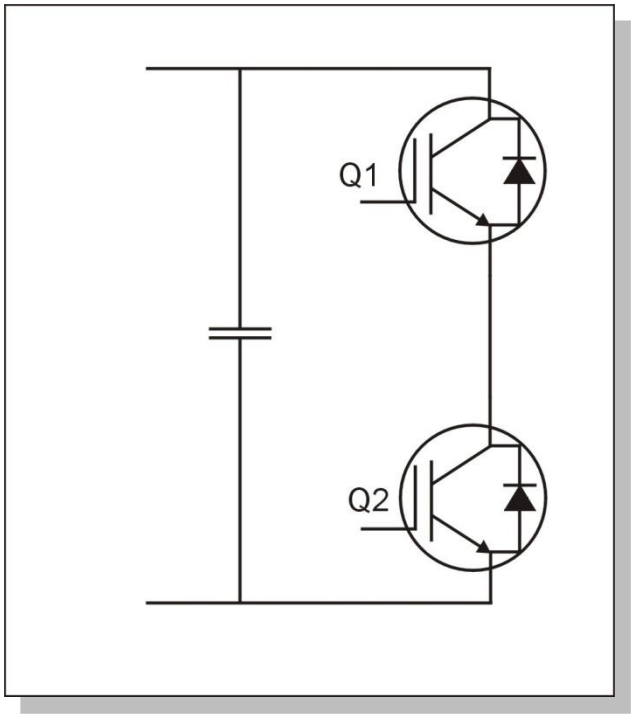
- Bipolar switching





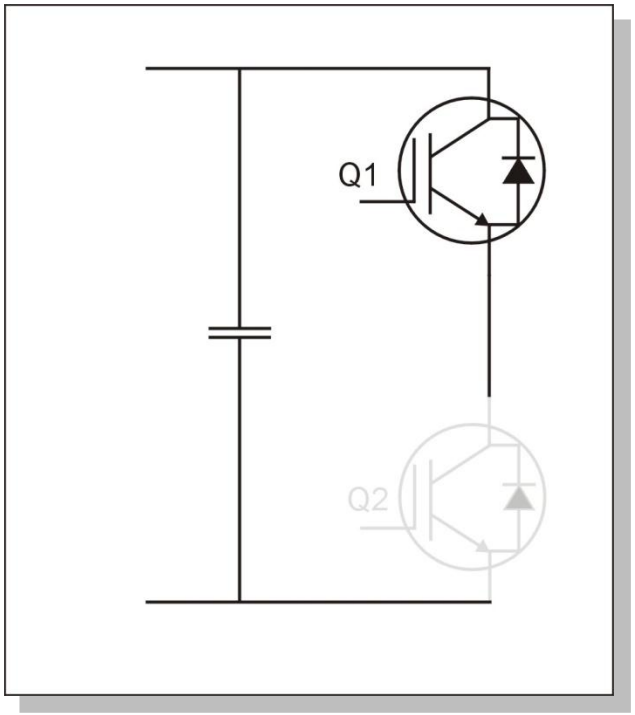
Independent versus Complementary Switching

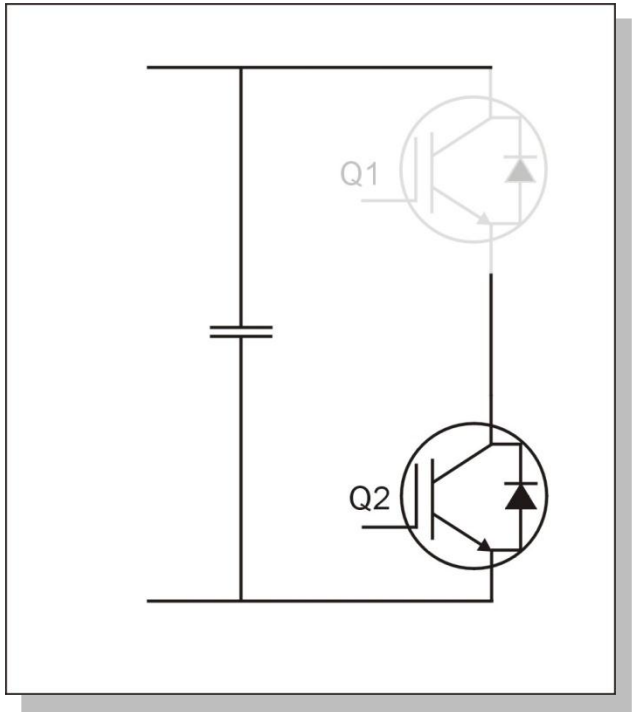
- The terms “independent” and “complementary” are related to how the transistors are switched in one phase.



Independent versus Complementary Switching

- Independent switching

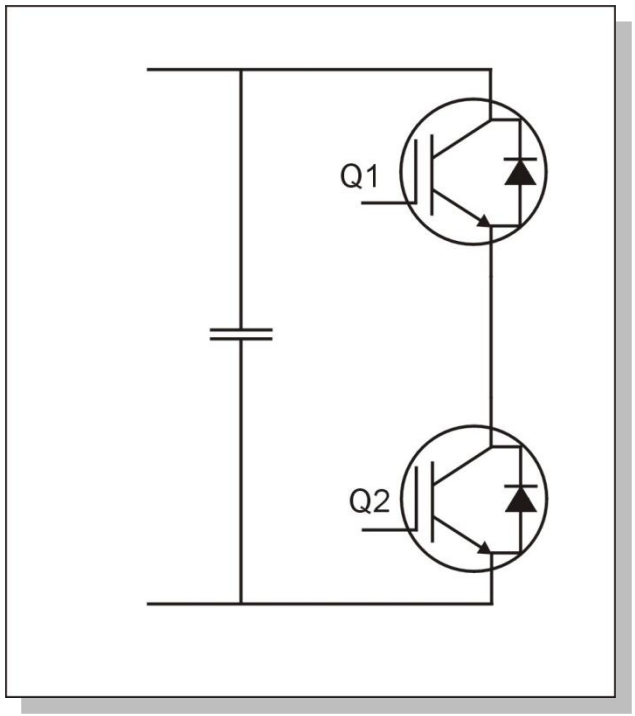




The top or bottom transistor is switched during whole period.

Independent versus Complementary Switching

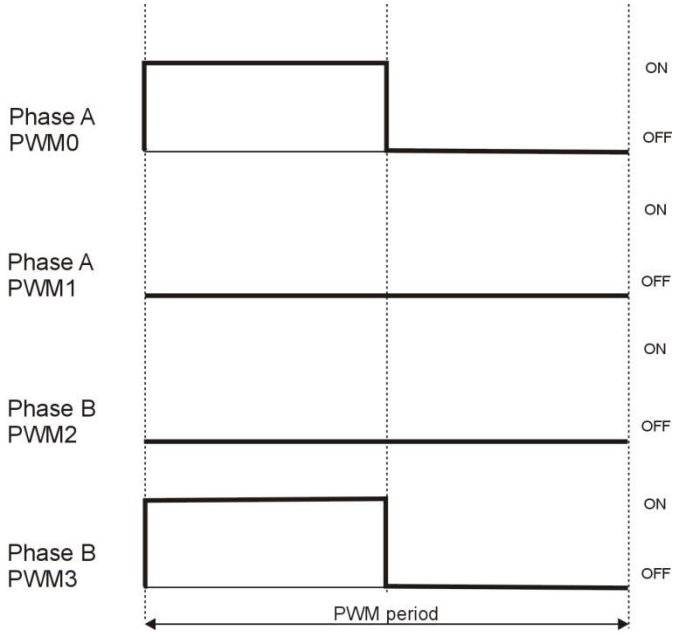
- Complementary switching



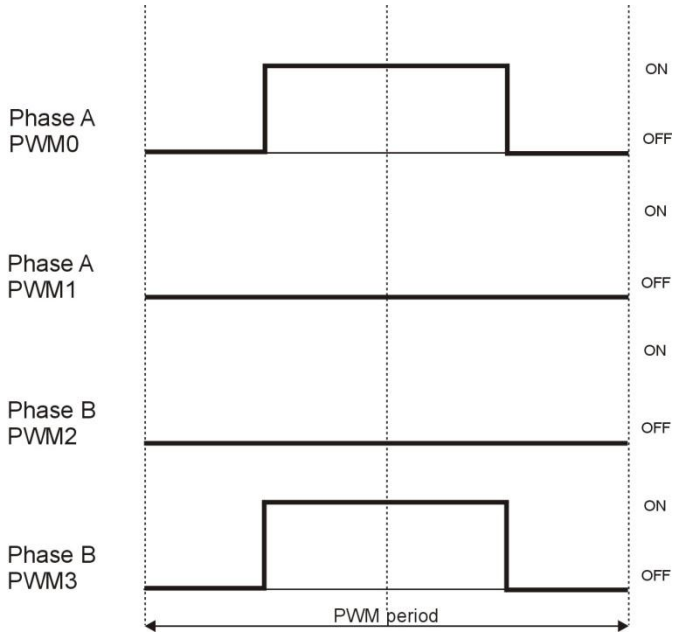
Both transistor are switched in complementary manner during whole period

Edge versus Center Aligned PWM

- The term “Edge/Center Aligned PWM” is related to how the PWM pulse is aligned within PWM period



Edge Aligned PWM



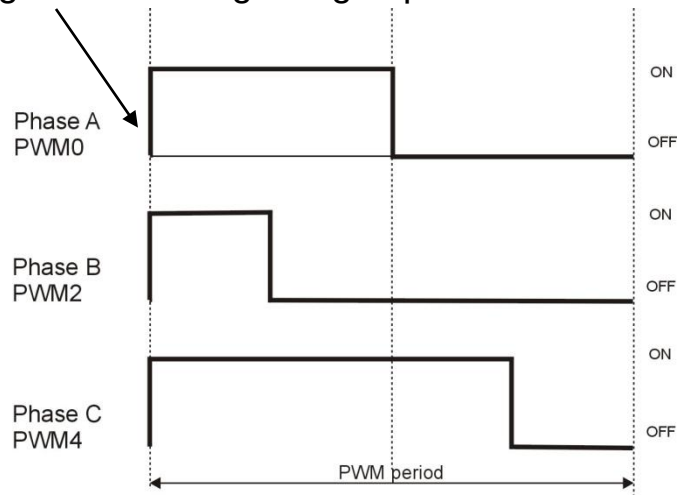
Center Aligned PWM

Doesn’t make sense for DC and BLDC motors from EMI and EMC point of view

Edge versus Center Aligned PWM

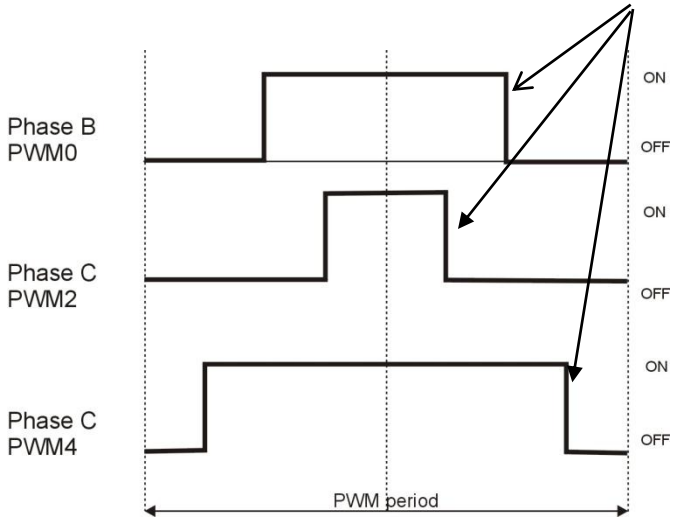
- Sinusoidal PWM Generation

High noise at beginning of period



Edge Aligned PWM

Edges spread over whole period



Center Aligned PWM

Center Aligned PWM is better from EMI and EMC point of view for sinusoidal generation

Note: Complementary channels PWM1/3/5 not shown.

Agenda

- Separately exited DC motor
- Basic Terms
- PWM Modulation techniques for DC and BLDC drives
  - DC Motors – Single Quadrant Operation
    - Single Switch and Freewheeling Diode
  - DC and BLDC Motors – 2 & 4 Quadrant Operation
    - H-Bridge & 3-Phase Bridge
    - Independent Bipolar Switching
    - Independent Unipolar Switching
    - Complementary Bipolar Switching
    - Complementary Unipolar Switching
    - Independent/Complementary Unipolar Switching
- BLDC Motor Theory
- Microcontroller MC56F8006

Pulse Width Modulation Technique

- DC Motors – Single Quadrant Operation
  - Single Switch and Freewheeling Diode
- DC and BLDC Motors – 2 & 4 Quadrant Operation
  - H-Bridge & 3-Phase Bridge
    - Independent Bipolar Switching
    - Independent Unipolar Switching
    - Complementary Bipolar Switching
    - Complementary Unipolar Switching
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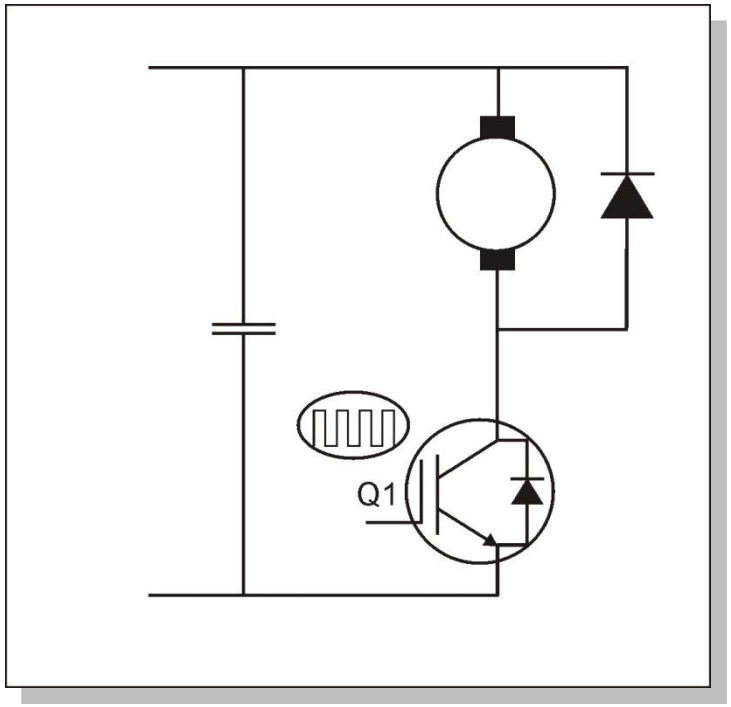
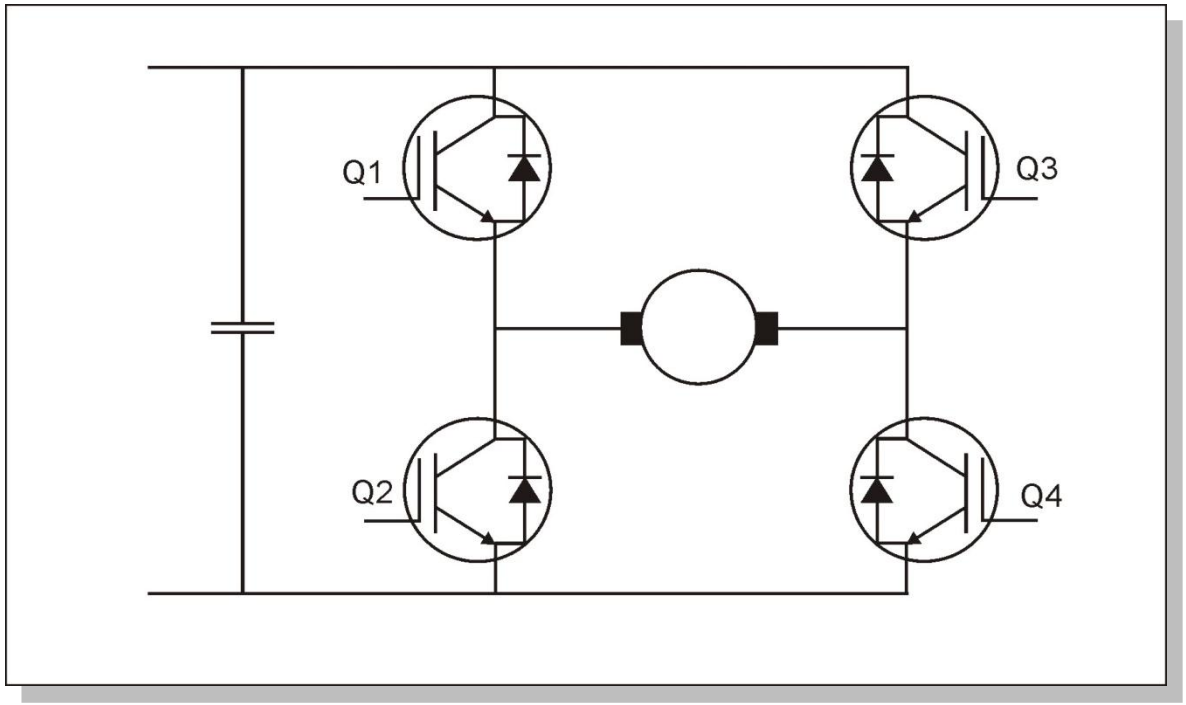
Pulse Width Modulation Technique

- DC Motors – Single Quadrant Operation
  - Single Switch and Freewheeling Diode



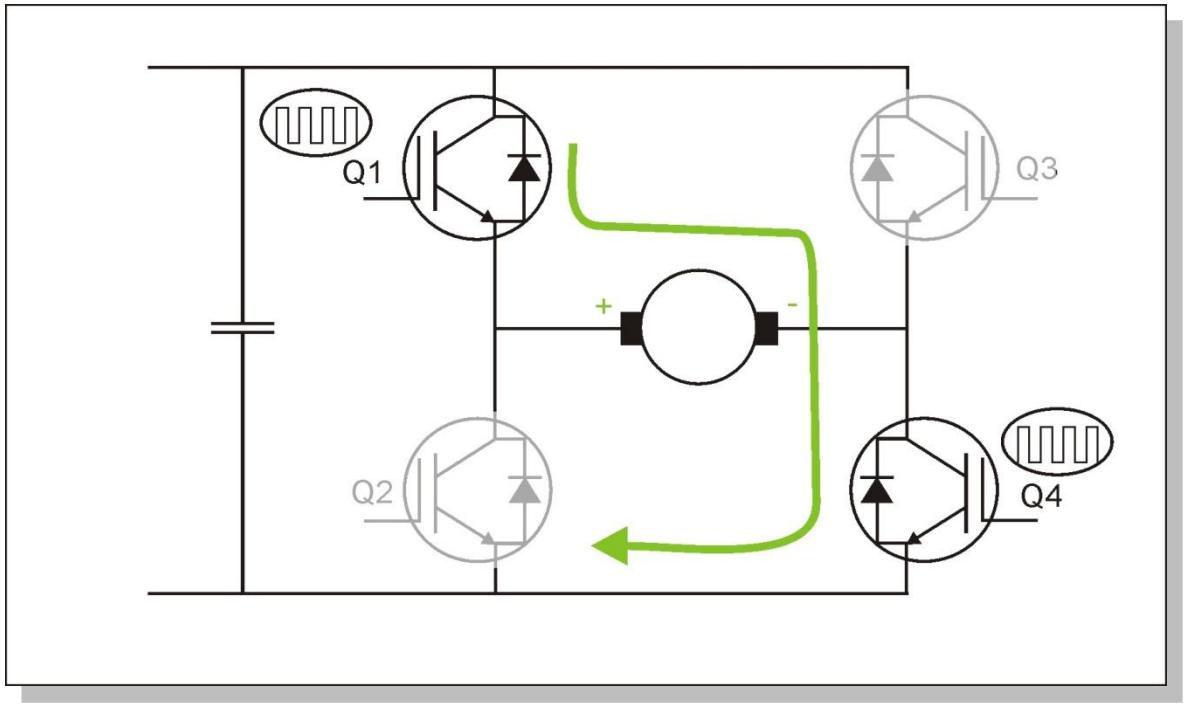
Pulse Width Modulation Technique

- DC and BLDC Motors – 2 Quadrant Operation
  - Independent Bipolar Switching



Pulse Width Modulation Technique

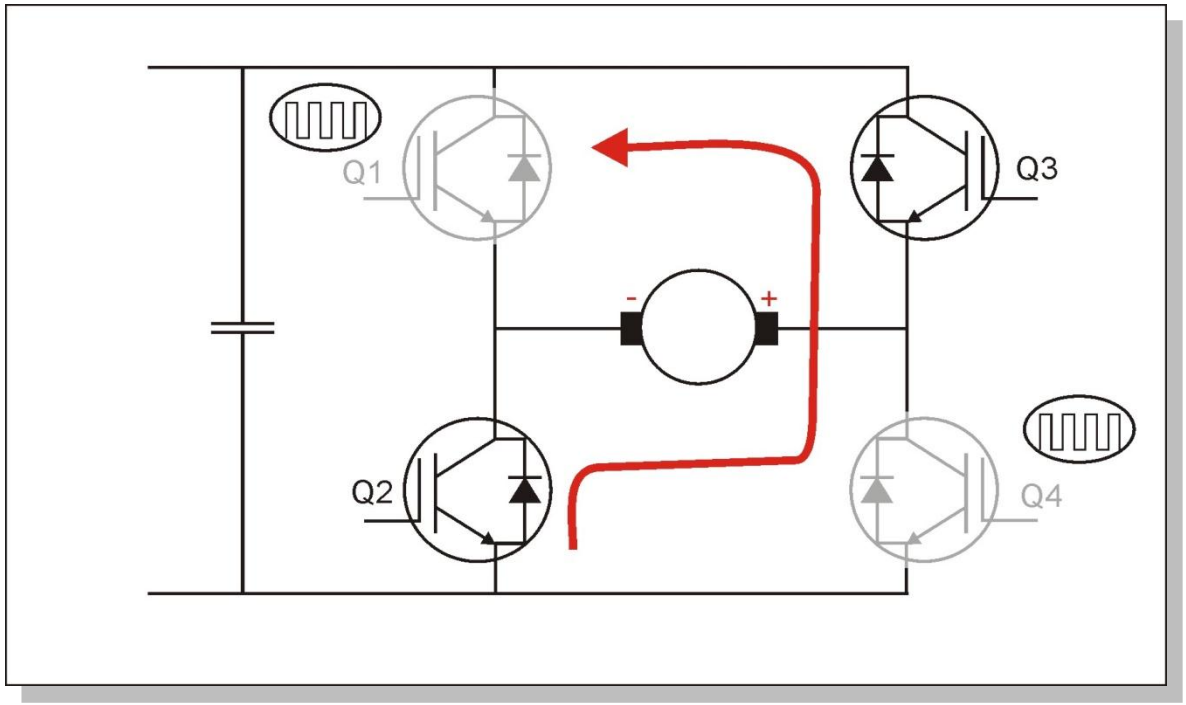
- DC and BLDC Motors – 2 Quadrant Operation
  - Independent Bipolar Switching – Acting Transistors



Q1=Q4=PWM

Pulse Width Modulation Technique

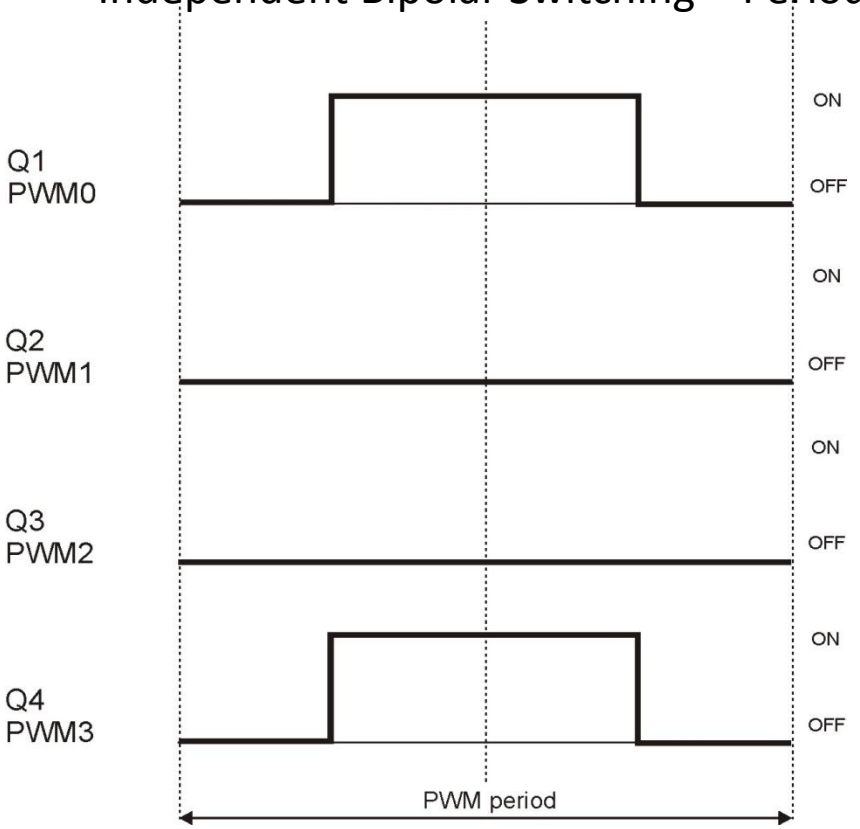
- DC and BLDC Motors – 2 Quadrant Operation
  - Independent Bipolar Switching – Freewheeling Diodes



Q1=Q4=PWM

Pulse Width Modulation Technique

- DC and BLDC Motors – 2 Quadrant Operation
  - Independent Bipolar Switching – Period Details



Advantages

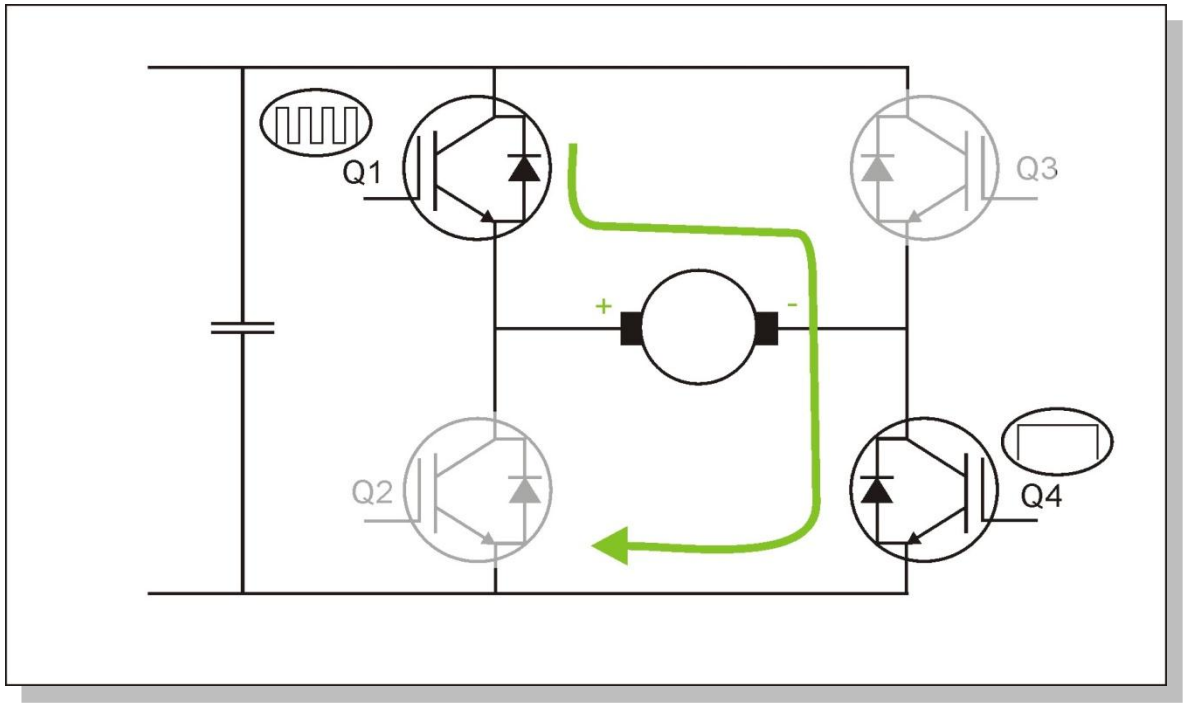
- Simple implementation
- Do not need deadtime

Disadvantages

- Dramatic change in system parameters as current transitions between discontinuous and continuous modes.
- Motor exhibits low torque in discontinuous current mode.
- 0 – 100% duty cycle for full speed range means minimal pulse width required to provide BEMF or current sensing.
- Higher switching loses comparing to unipolar independent switching

Pulse Width Modulation Technique

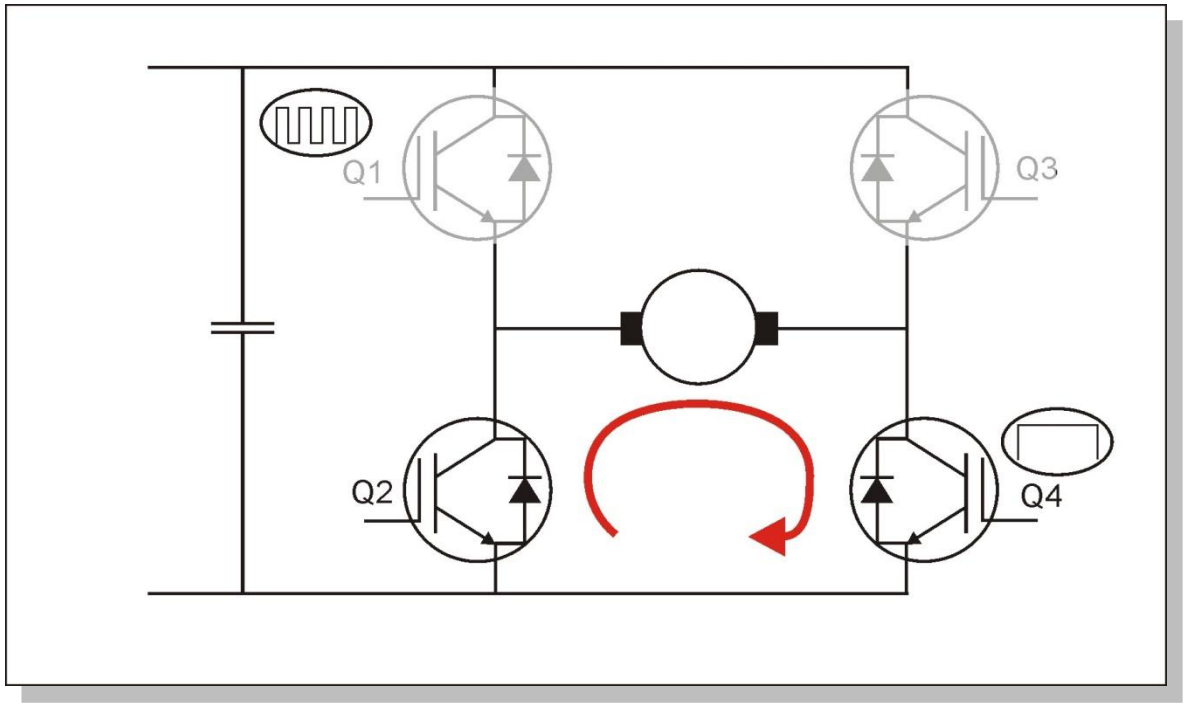
- DC and BLDC Motors – 2 Quadrant Operation
  - Independent Unipolar Switching – Acting Transistors



Q1=PWM; Q4=ON

Pulse Width Modulation Technique

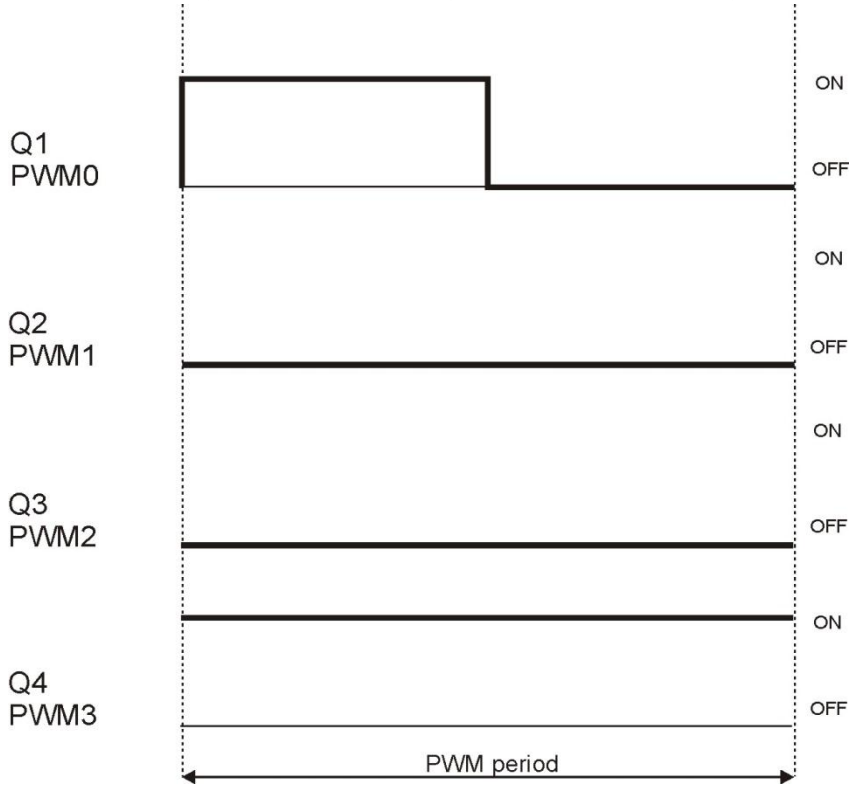
- DC and BLDC Motors – 2 Quadrant Operation
  - Independent Unipolar Switching – Freewheeling Diodes



Q1=PWM; Q4=ON

Pulse Width Modulation Technique

- DC and BLDC Motors – 2 Quadrant Operation
  - Independent Unipolar Switching – Period Details



Advantages

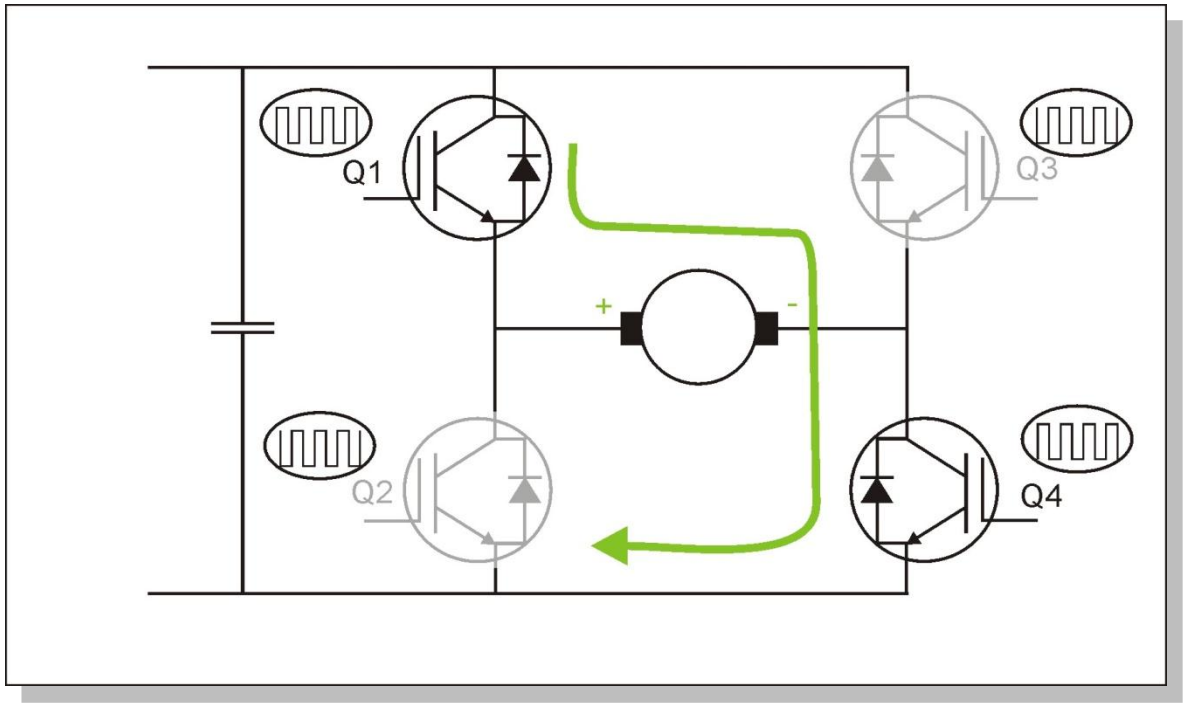
- Simple implementation
- Do not need deadtime
- 3 PWM channels + 3 GPIO enough for implementation
- Excellent motor behavior (motor exhibits good torque, even at low speeds).
- Lower switching loses

Disadvantages

- 0 – 100% duty cycle for full speed range means minimal pulse width required to provide BEMF or current sensing.

Pulse Width Modulation Technique

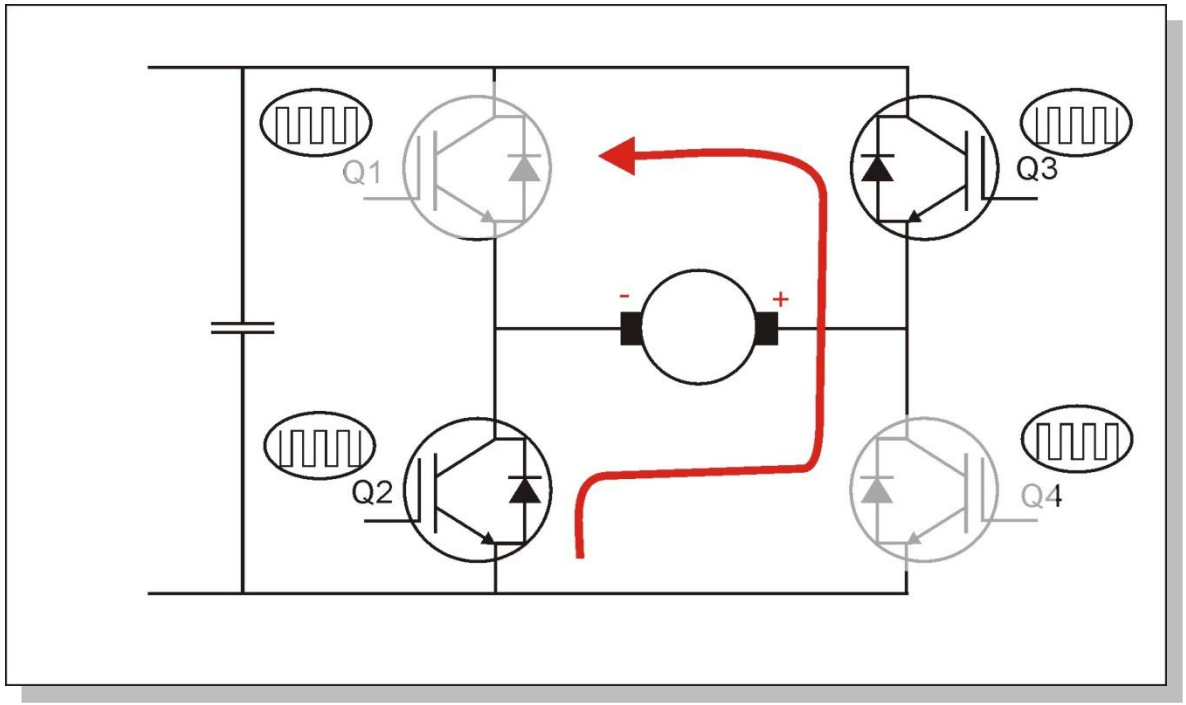
- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Bipolar Switching (I.Q) – Acting Transistors



Q1=Q4=PWM; Q2=Q3=$\overline{Q1}$

Pulse Width Modulation Technique

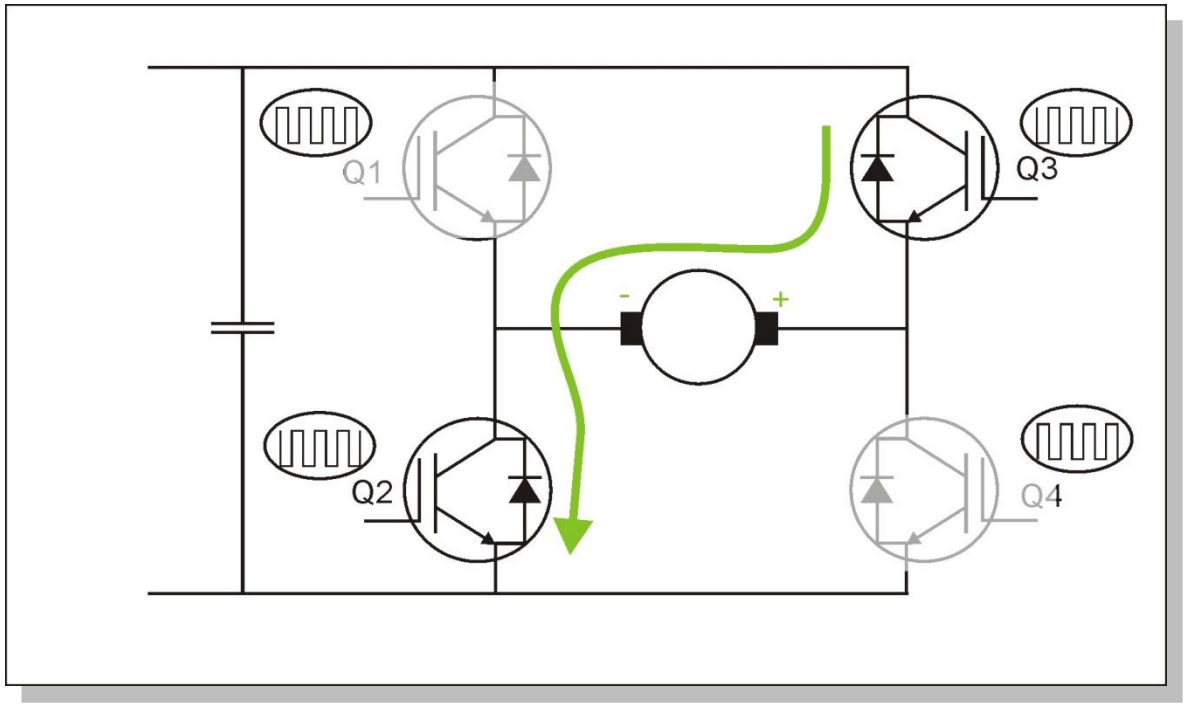
- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Bipolar Switching (I. Q) – Freewheeling Diodes



Q1=Q4=PWM; Q2=Q3=$\overline{Q1}$

Pulse Width Modulation Technique

- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Bipolar Switching (III.Q) – Acting Transistors



Q1=Q4=PWM; Q2=Q3=$\overline{Q1}$

Pulse Width Modulation Technique

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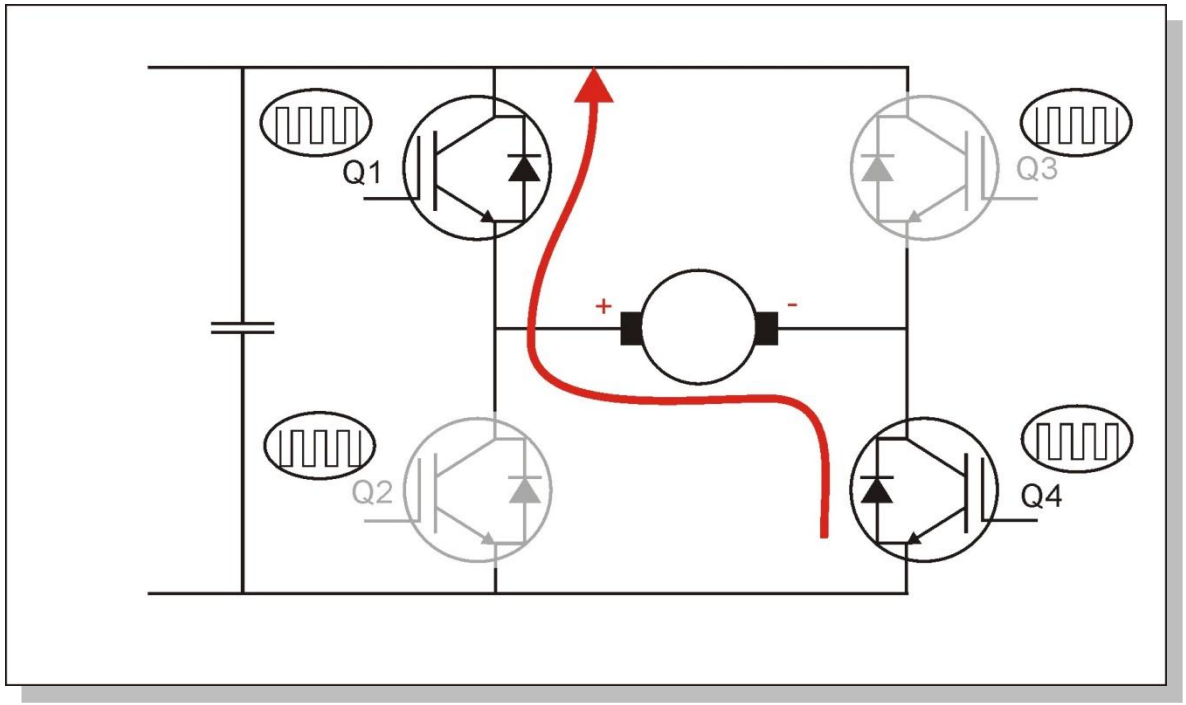
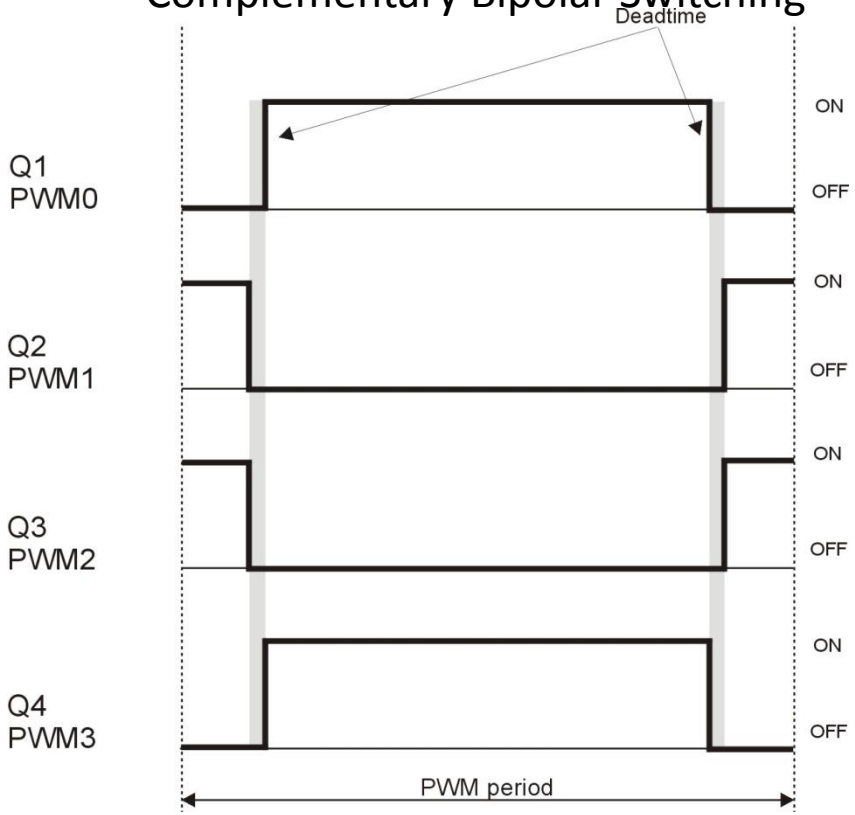
  - Complementary Bipolar Switching (III. Q) – Freewheeling Diodes



$Q1=Q4=PWM;\ Q2=Q3=\overline{Q1}$

Pulse Width Modulation Technique

- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Bipolar Switching – Period Details



Advantages

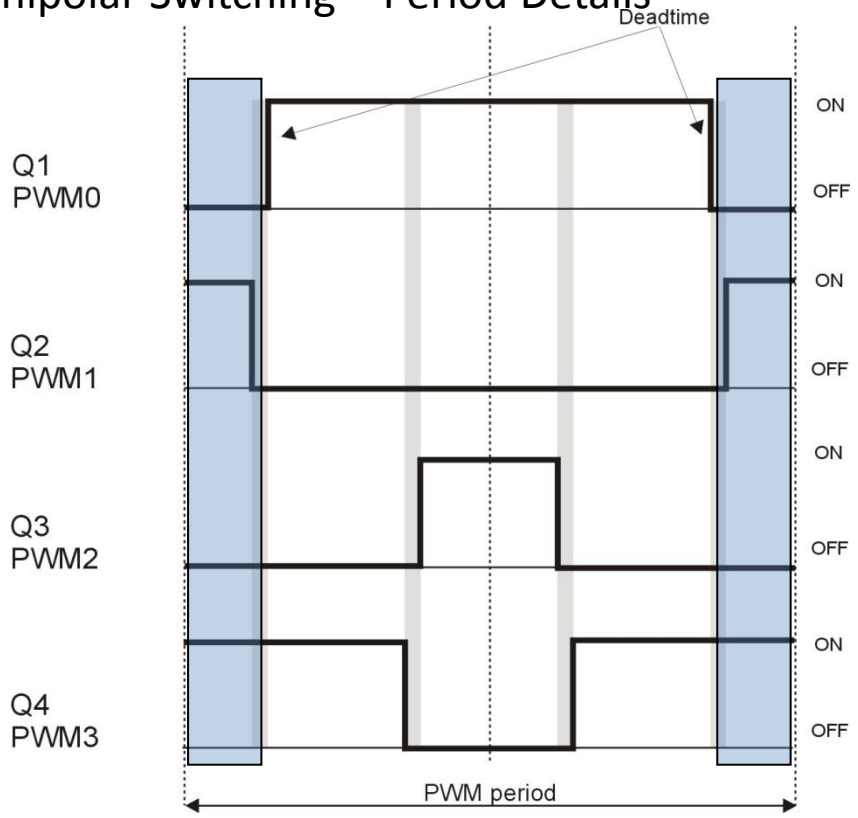
- Excellent motor behavior (motor exhibits good torque, even at low speeds).
- Full 4-Quadrant operation (Motoring and generating modes).

Disadvantages

- Complementary generation by SW or external MOSFET/IGBT driver
- Deadtime generation by SW or external MOSFET/IGBT driver
- Higher switching loses

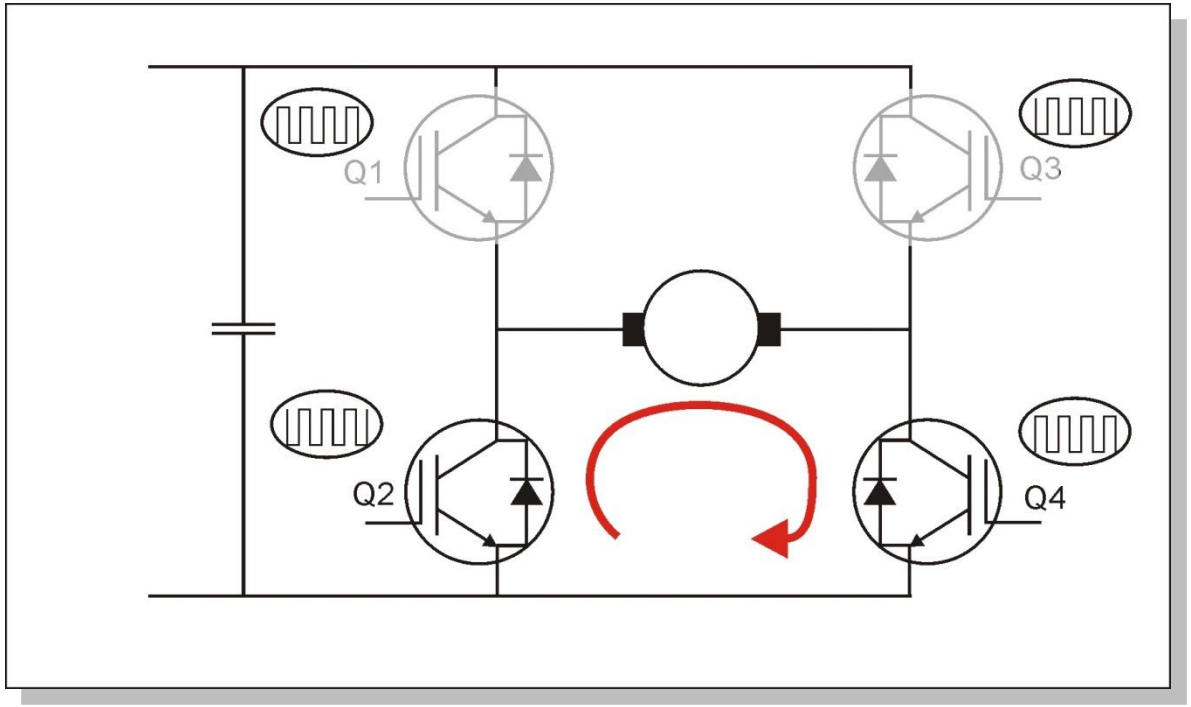
Pulse Width Modulation Technique

- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Unipolar Switching – Period Details



Pulse Width Modulation Technique

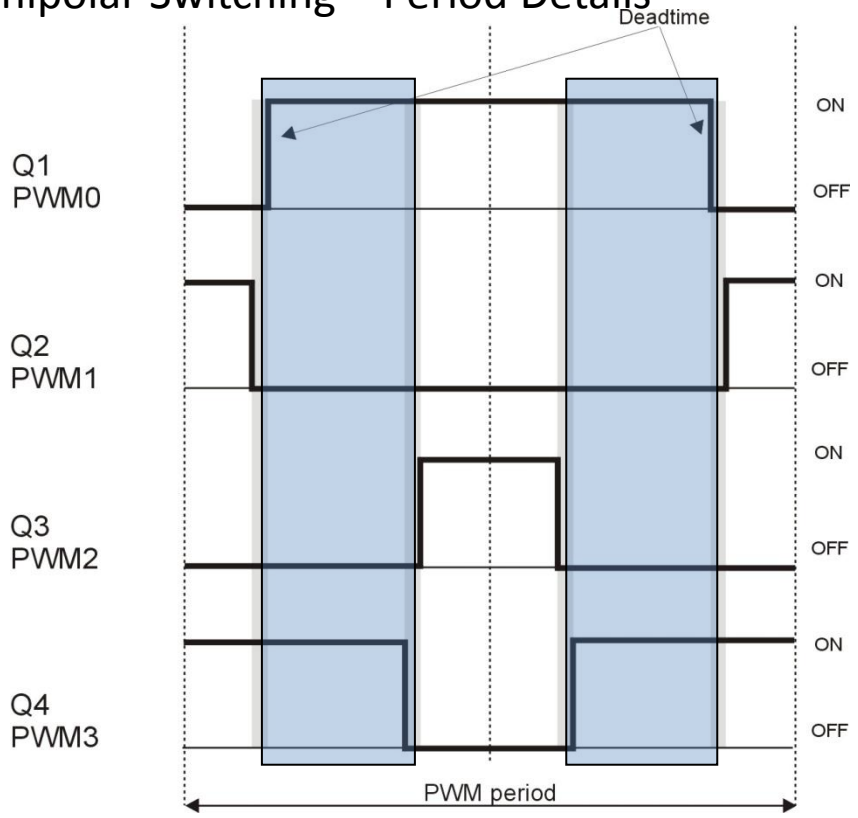
- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Unipolar Switching – Freewheeling Diodes



Q1= 50%$^{\pm}$DC; Q4=50%$^{\mp}$DC; Q2=$\overline{Q1}$; Q3=$\overline{Q4}$; *DC – duty cycle*

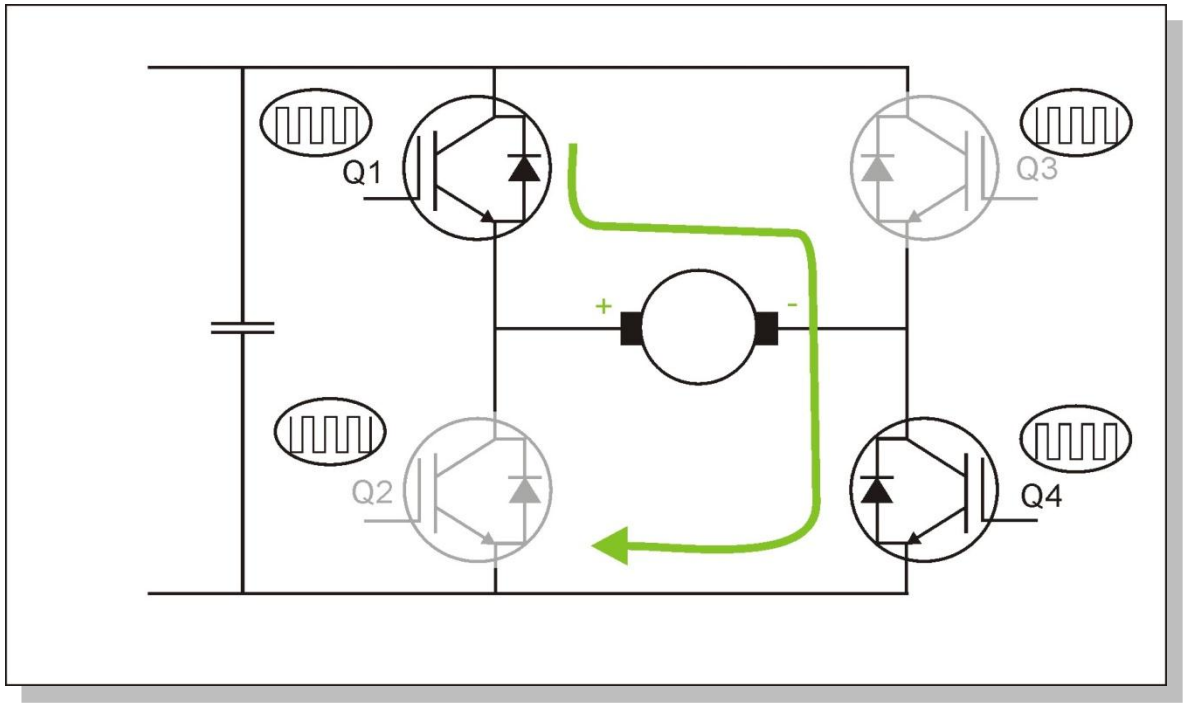
Pulse Width Modulation Technique

- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Unipolar Switching – Period Details



Pulse Width Modulation Technique

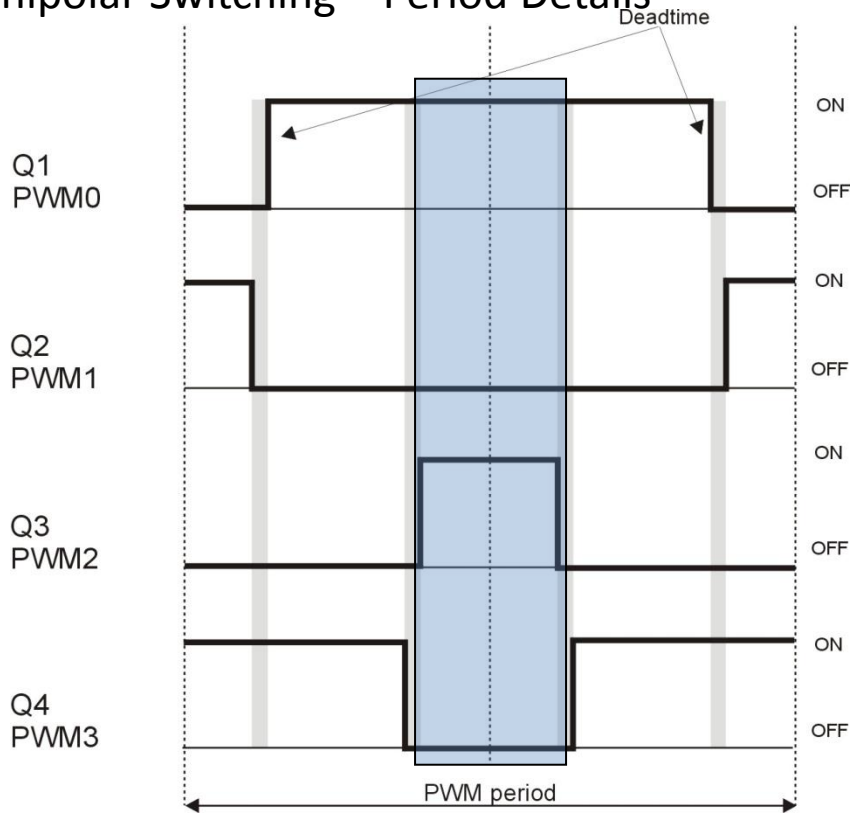
- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Unipolar Switching – Acting Transistors



Q1= 50%$^{\pm}$DC; Q4=50%$^{\mp}$DC; Q2=$\overline{Q1}$; Q3=$\overline{Q4}$; *DC – duty cycle*

Pulse Width Modulation Technique

- DC and BLDC Motors – 4 Quadrant Operation
  - Complementary Unipolar Switching – Period Details



Pulse Width Modulation Technique

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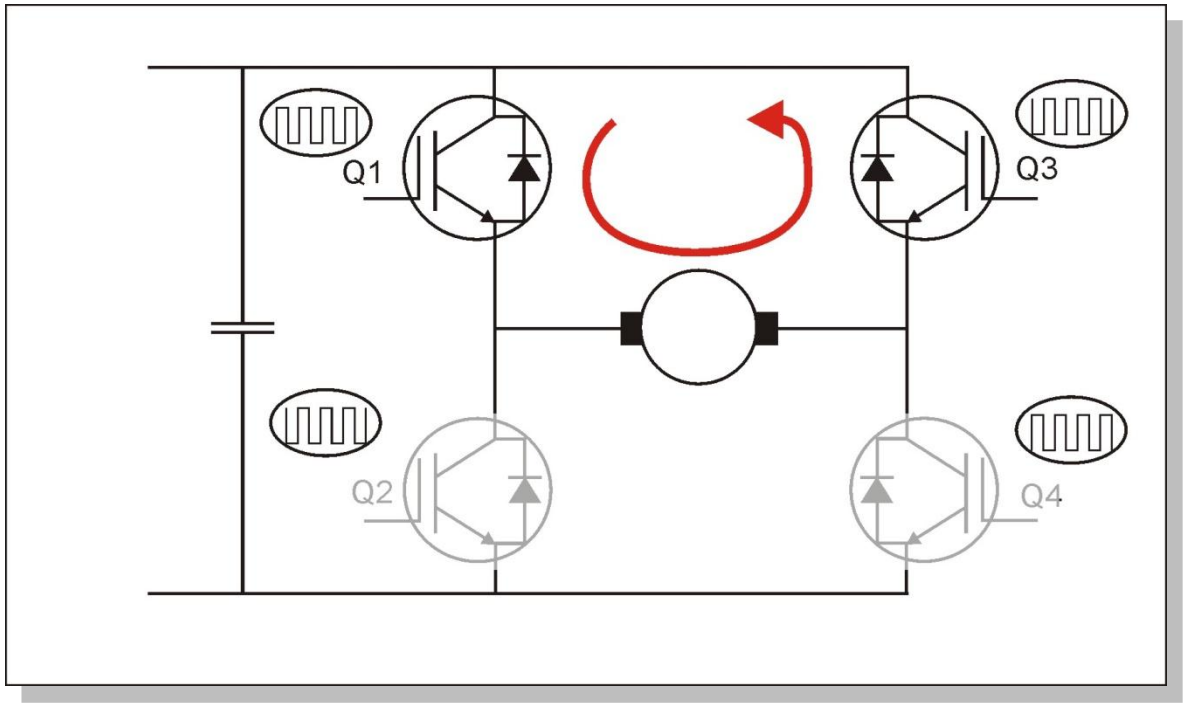
  - Complementary Unipolar Switching – Freewheeling Diodes



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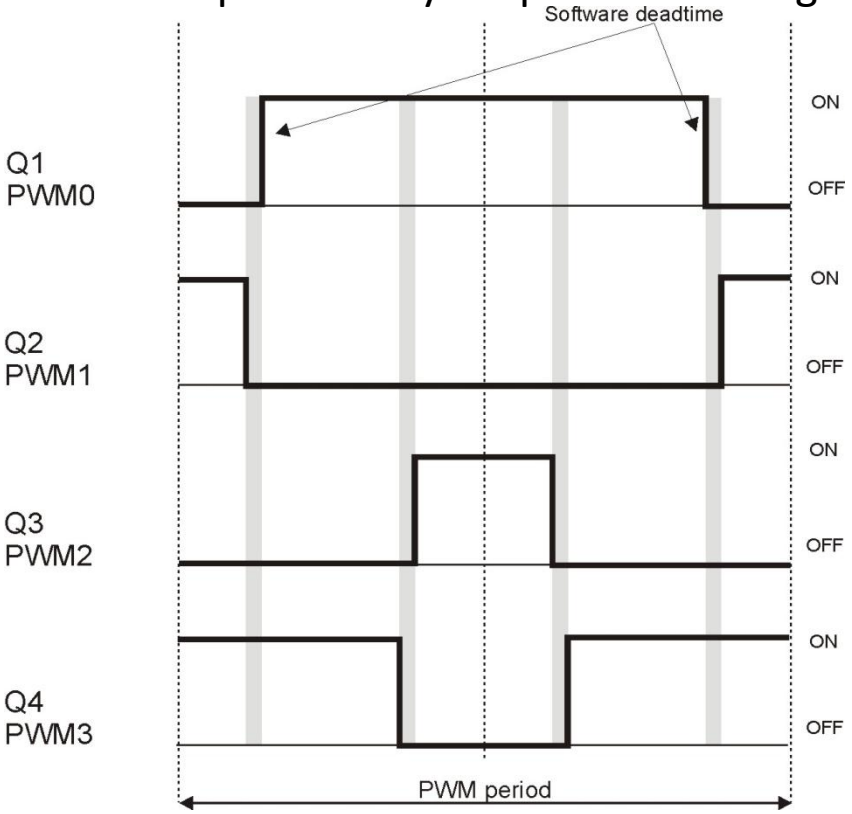


Advantages

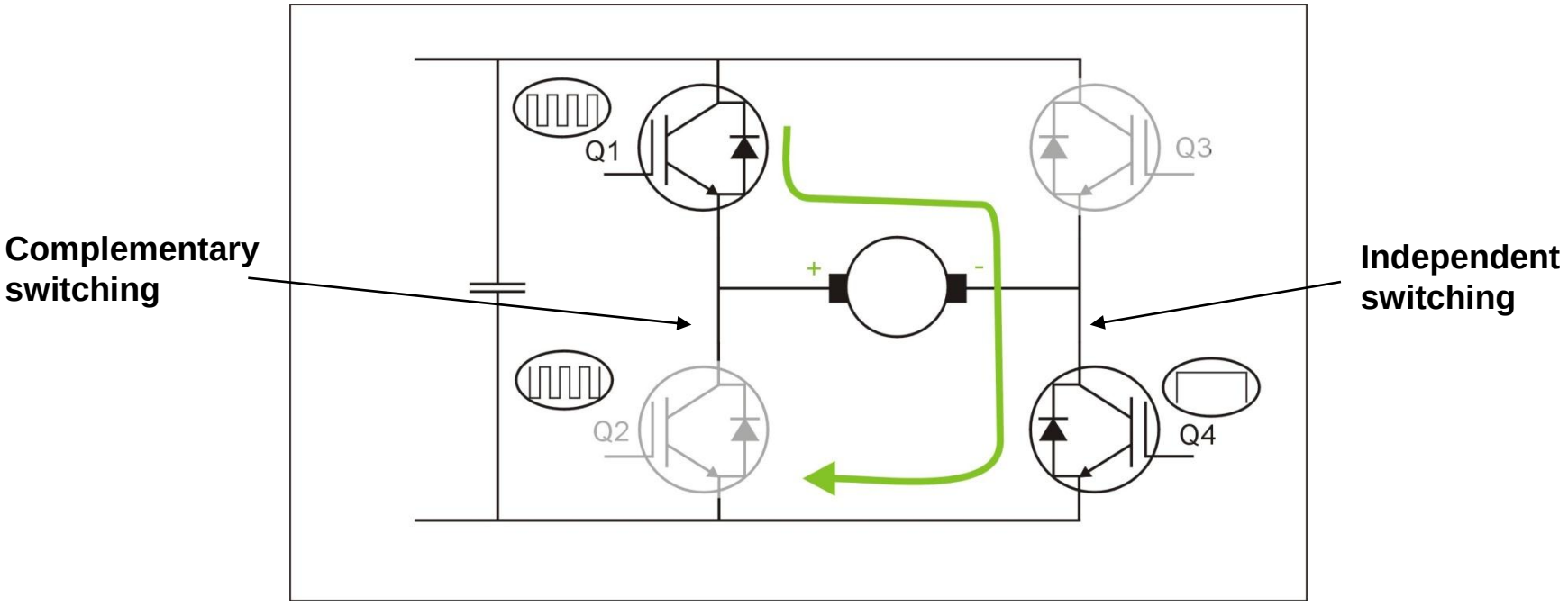
- Lowest current ripple
- Excellent motor behavior (motor exhibits good torque, even at low speeds).
- Full 4-Quadrant operation (Motor and generator modes).
- Lower switching loses

Disadvantages

- Complementary generation by SW or external MOSFET/IGBT driver
- Deadtime generation by SW or external MOSFET/IGBT driver
- 0 – 100% duty cycle for full speed range means minimal pulse width required to provide BEMF or current sensing.

Pulse Width Modulation Technique

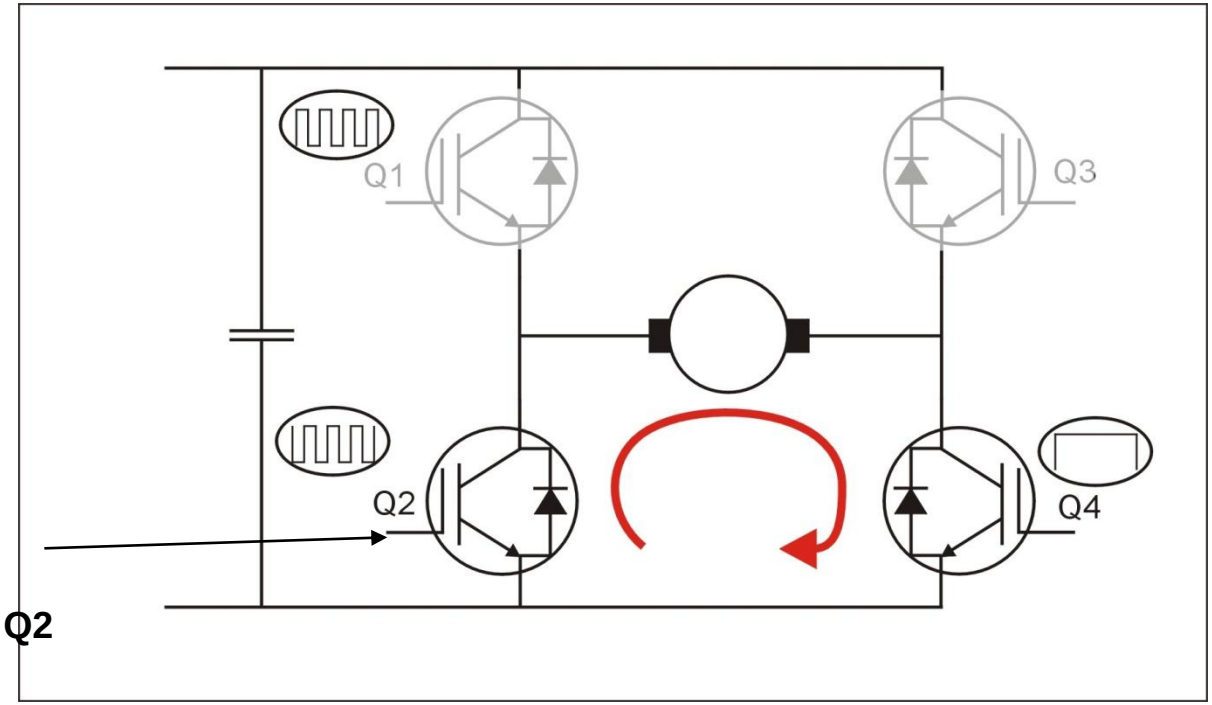
- DC and BLDC Motors – 2 Quadrant Operation
  - Independent/Complementary Unipolar Switching – MOSFETs only
  - Acting Transistors



Q1=PWM, Q2=$\overline{Q1}$; Q4=ON

Pulse Width Modulation Technique

- DC and BLDC Motors – 2 Quadrant Operation
  - Independent/Complementary Unipolar Switching – MOSFETs only
  - Freewheeling Transistors



Q2 on during freewheeling reduce loses in Q2

Q1=PWM, Q2=$\overline{Q1}$; Q4=ON

Pulse Width Modulation Technique - Summary

- 1/2/4 Quadrant Operation
  - Single Quadrant Operation
    - Single direction of rotation (DC motors only)
  - Two Quadrant Operation
    - Both direction of rotation
    - Can not work as generator (brake)
  - Four Quadrant Operation
    - Both direction of rotation
    - Can work as motor and generator as well

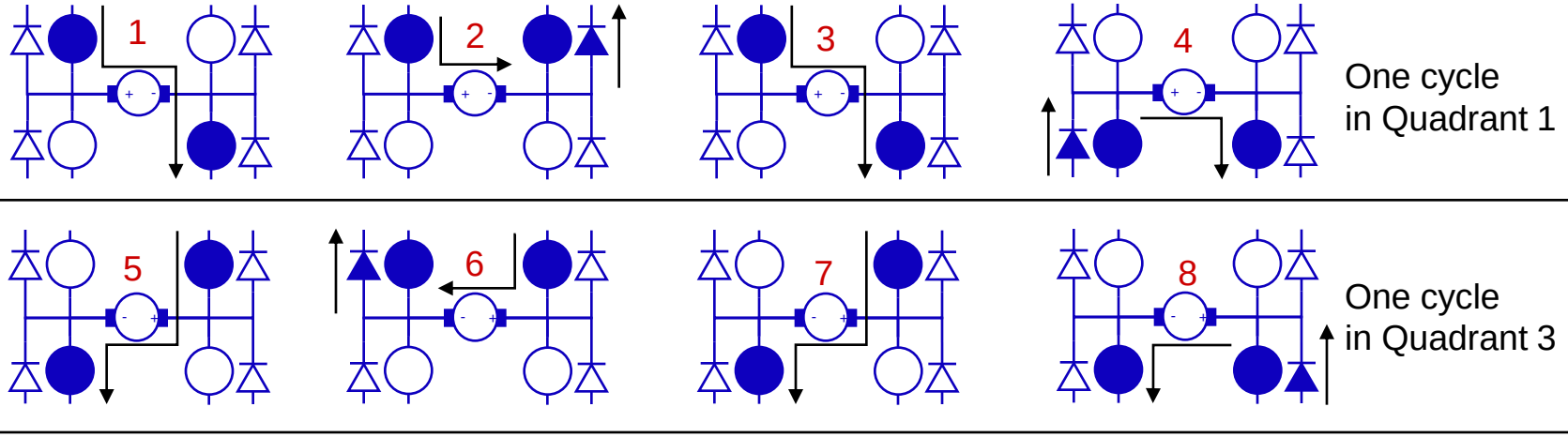
Pulse Width Modulation Technique - Summary

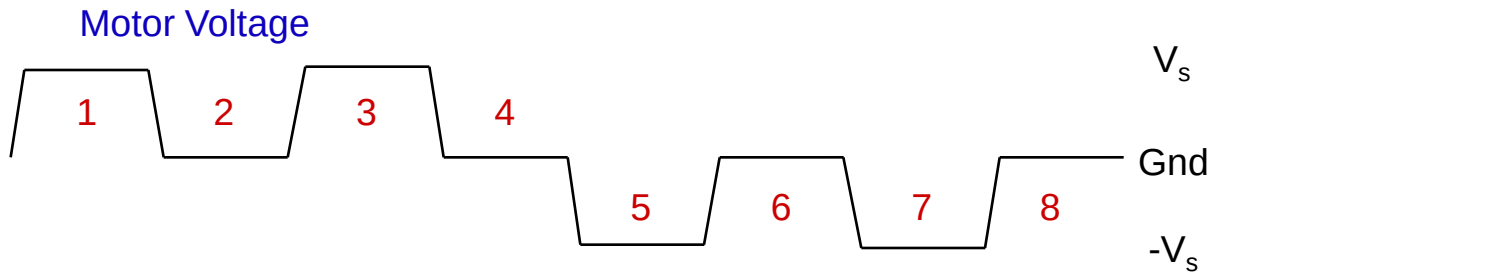
- Independent/Complementary switching
  - Independent
    - 2 quadrant operation only
    - do not need complementary and dead-time logic
  - Complementary
    - 4 quadrant operation
- Unipolar/Bipolar switching
  - Unipolar – lower loses, preferred
  - Bipolar – higher loses against to unipolar
- Edge/Center Aligned switching
  - Doesn't make sense for DC and BLDC motor
  - Center Aligned PWM reduce EMI noise

Pulse Width Modulation Technique - Summary

- PWM Techniques
  - Independent Bipolar PWM
    - Not recommended due to discontinuous current
  - Complementary Bipolar PWM
    - Use for 4 quadrant drives
  - Independent Unipolar PWM
    - Best choice for 2 quadrant drives
  - Complementary Unipolar PWM
    - Best choice for 4 quadrant drives
  - Independent/Complementary Unipolar PWM
    - Best choice for MOSFET H-bridge and 2 quadrant drive

Unipolar Switching Modes





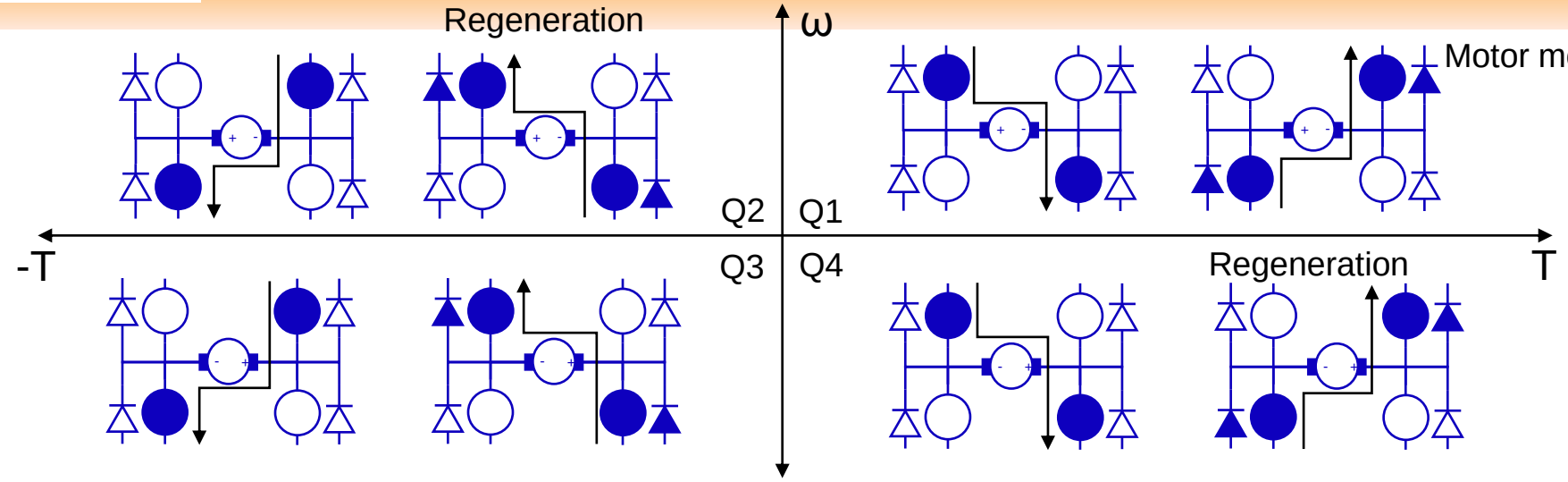
Advantages

Control in all 4 quadrants.
Motor PWM frequency doubled.

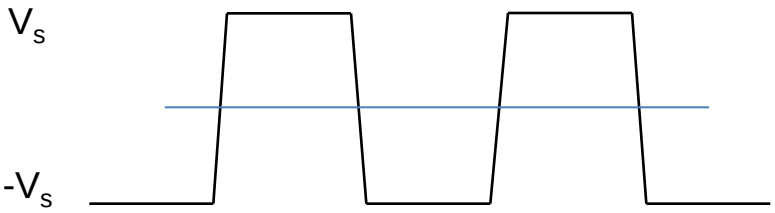
Disadvantages

Deadtime generation is now required between four PWM signals.
Requires center aligned PWMs.

Bipolar Switching Modes



Motor Voltage



Advantages

Full control in all 4 quadrants.
No current re-circulation to complicate current detection and limiting.

Disadvantages

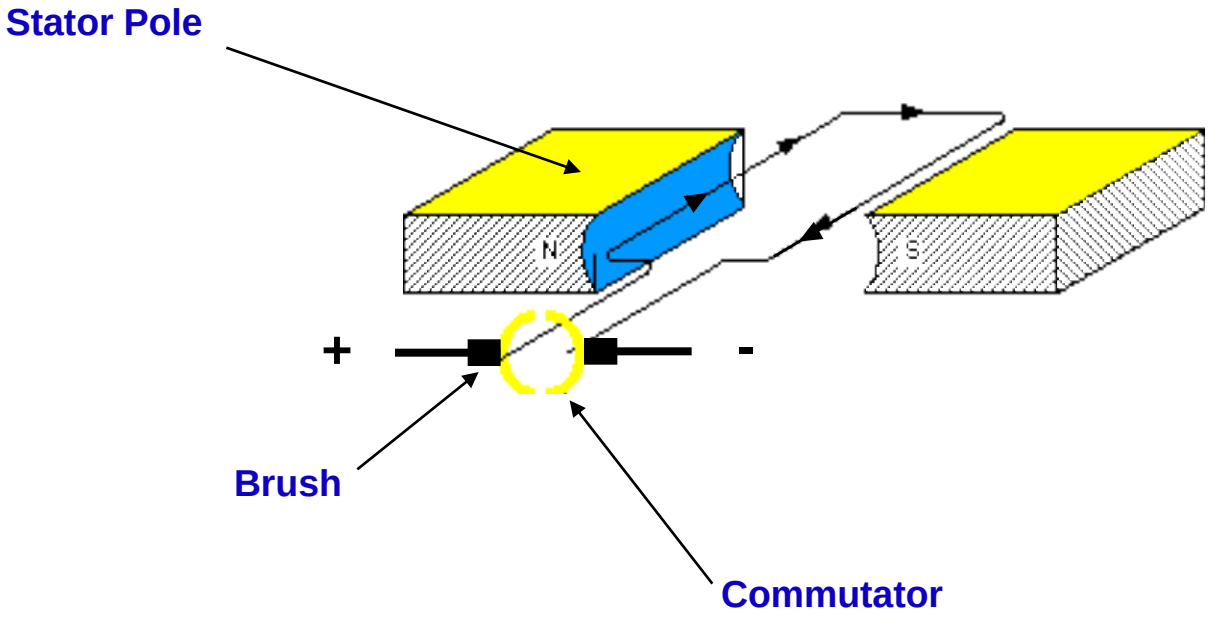
Deadtime generation is now required between two PWM signals.
ΔV seen by motor is 2Vs.

Agenda

- Separately exited DC motor
- Basic Terms
- PWM Modulation techniques for DC and BLDC drives
- BLDC Motor Theory
  - Brush DC Motor Principle
  - BLDC Motor Principle
  - Basic Control Techniques
  - BLDC versus PMSM motor
- Microcontroller MC56F8006

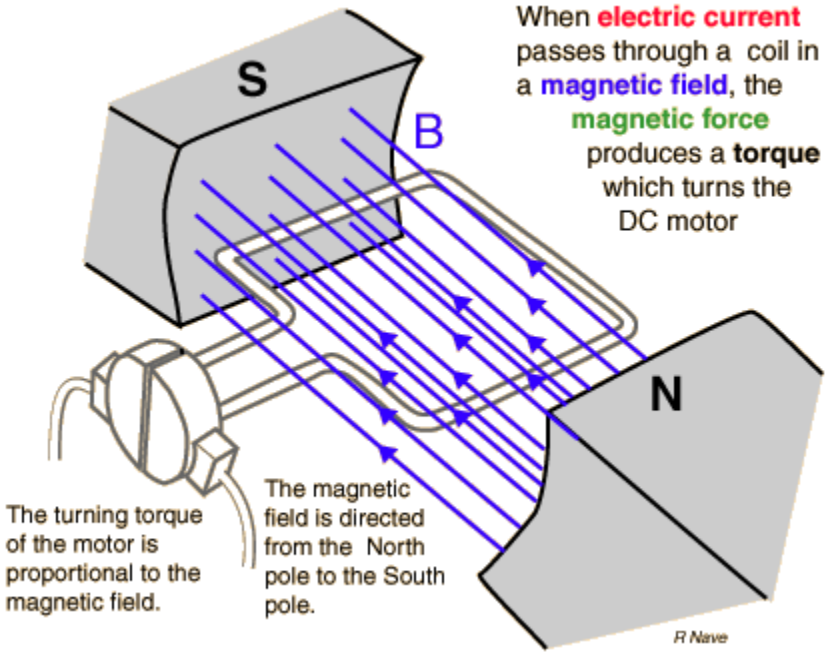
Brush DC Motor Principle

- Basic Structure



Brush DC Motor Principle

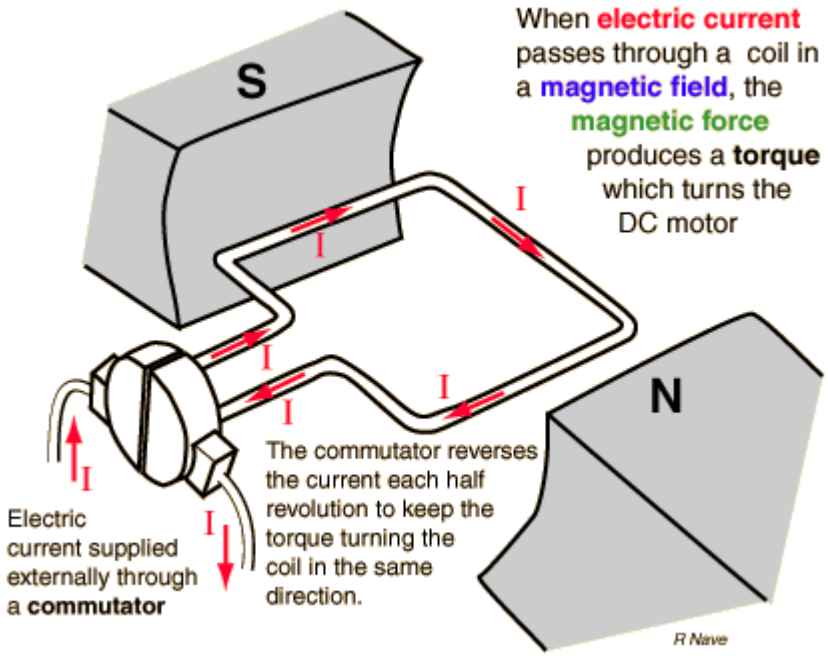
- Brush DC motor rotation



Source: http://hyperphysics.phy-astr.gsu.edu/hbase/magnetic/motdc.html#c1

Brush DC Motor Principle

- Brush DC motor rotation



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Brush DC Motor Principle

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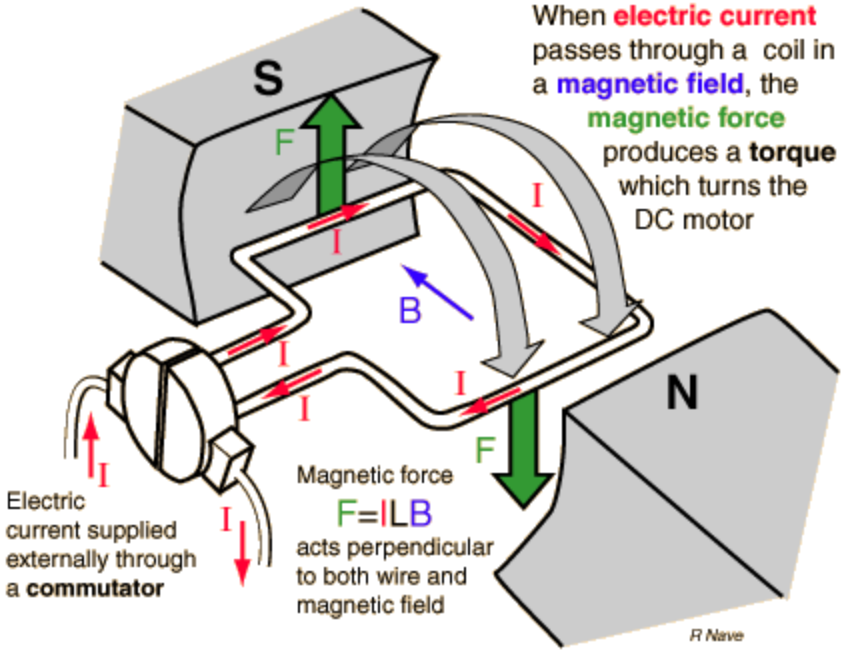

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Brush DC Motor Principle

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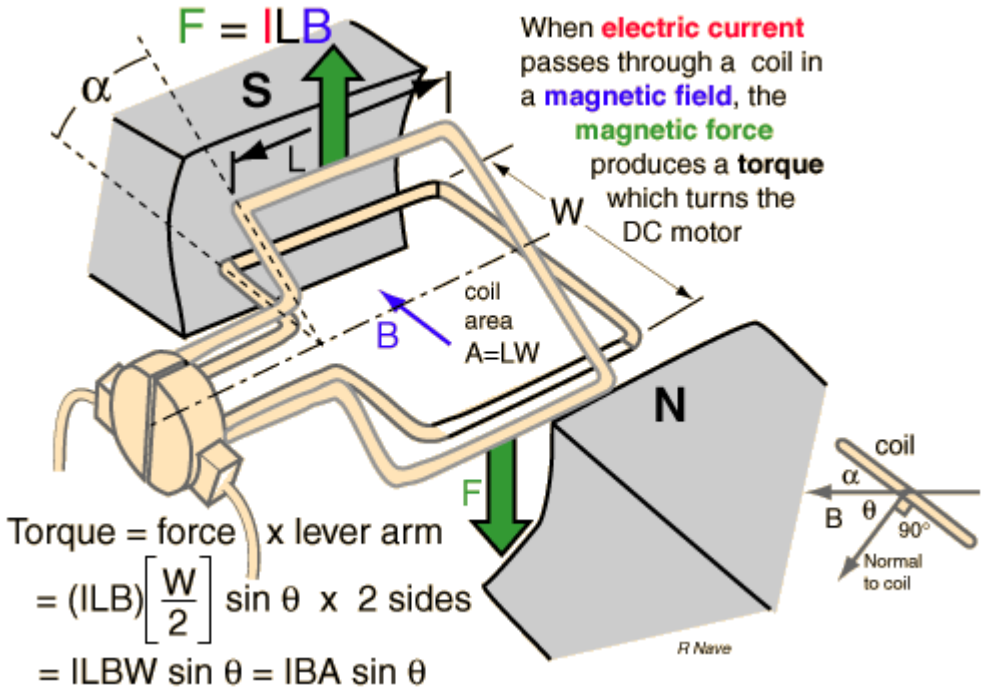

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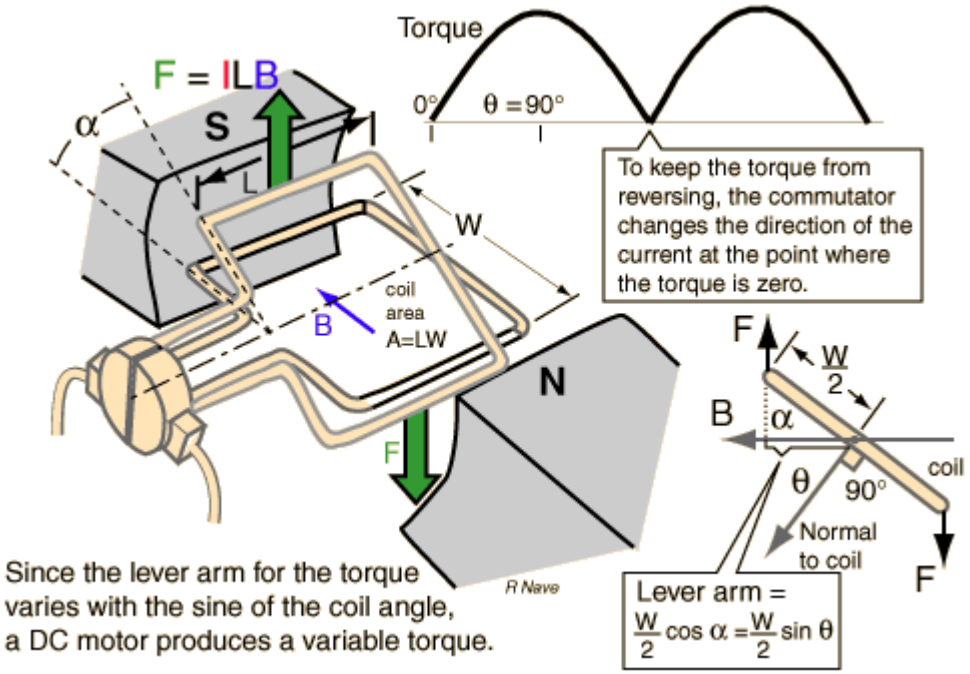
Brush DC Motor Principle

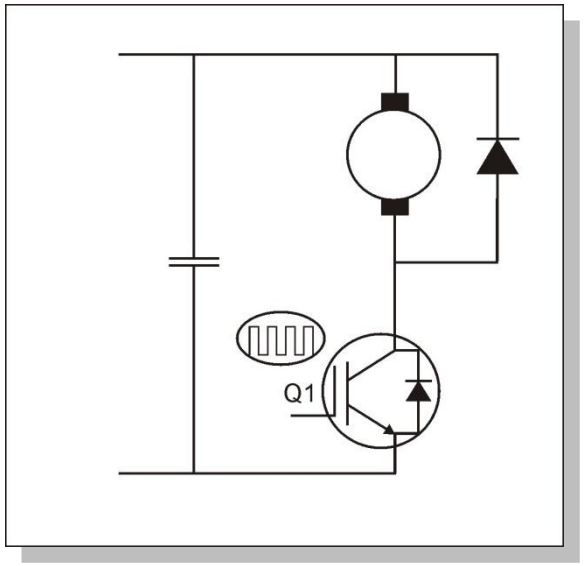
- Brush DC motor rotation



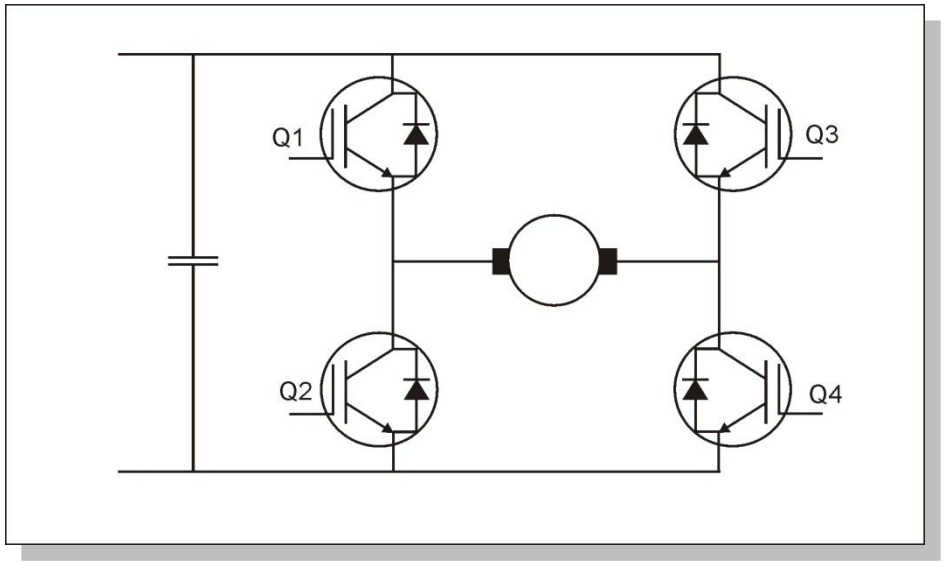
Source: http://hyperphysics.phy-astr.gsu.edu/hbase/magnetic/motdc.html#c1

Brush DC Motor Principle

- Brush DC motor control



Single quadrant operation



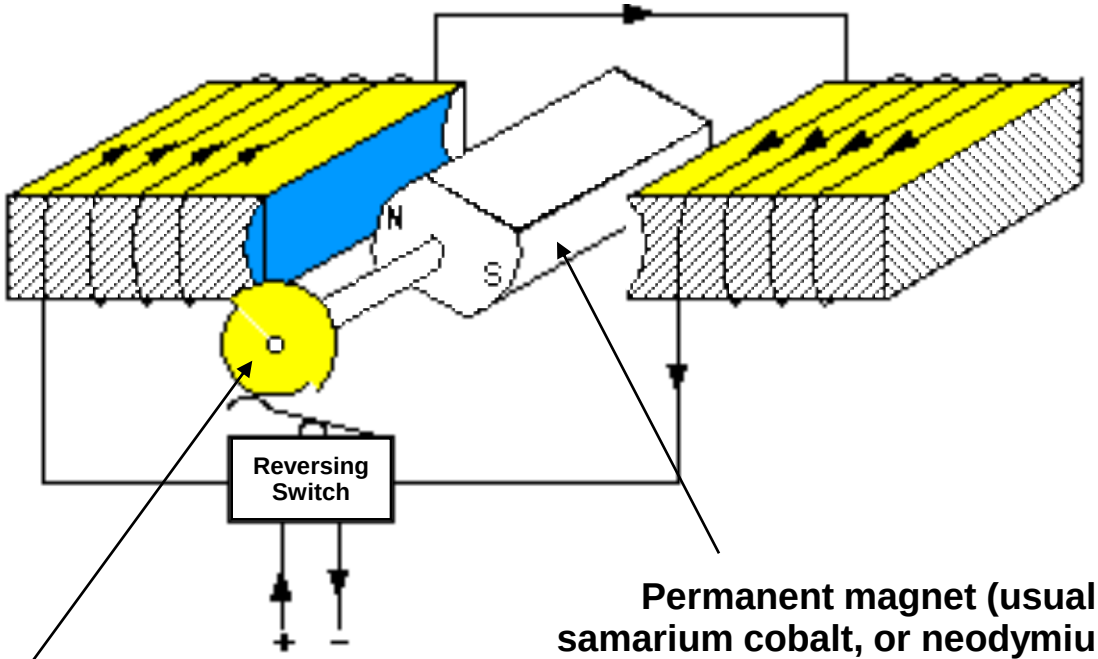
2 & 4 quadrant operation

Brush DC Motor Principle

- Advantages
  - Ease of control (self commutating).
  - Low rotor inertia (coreless rotors).
  - Lowest total system cost for basic motion.
  - Wound field motors exhibit high starting torque, (series wound) and can run with AC or DC.
- Disadvantages
  - Higher maintenance cost due to brush wear.
  - Electrical noise due to mechanical commutation.
  - Maximal speed limited by commutator
  - Heat is generated in armature, which is difficult to remove.
  - Friction losses associated with mechanical commutation.
  - Not usable in “intrinsically safe” environments.

Brushless DC Motor Principle

- Basic Structure



Permanent magnet (usually ferrite, samarium cobalt, or neodymium iron boron)

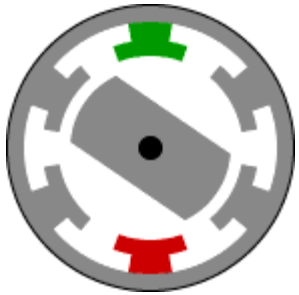
Requires mechanism to sense rotor position to commutate field properly

This is usually a hall effect sensor array or an encoder

Brushless DC Motor Principle

- Brushless DC motor rotation

- BLDC motor rotates because of the magnetic attraction between the poles of the rotor and the opposite poles of the stator.
- If the rotor poles are facing poles of the *opposite* polarity on the stator, a strong magnetic attraction is set up between them.
- The mutual attraction locks the rotor and stator poles together, and the rotor is literally yanked into step with the revolving stator magnetic field.



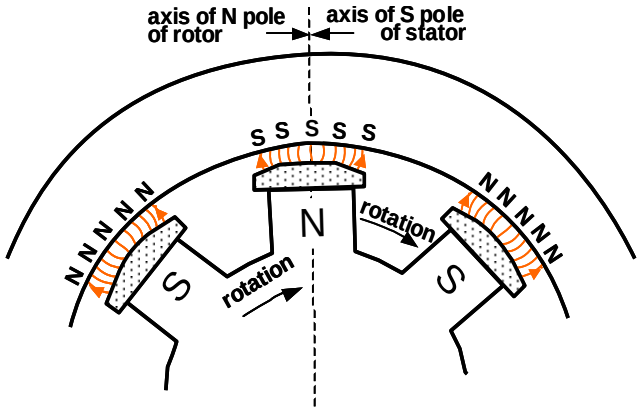


Figure 1- No-load condition

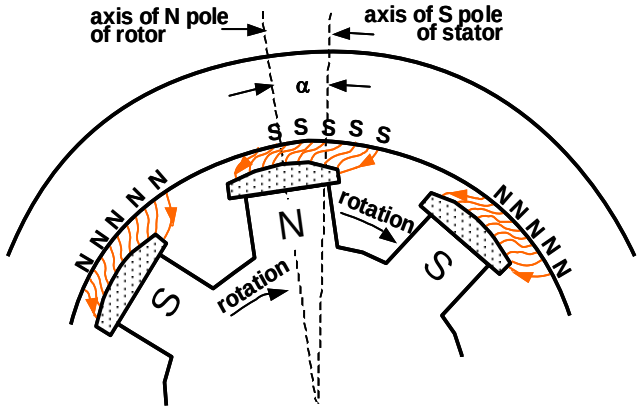
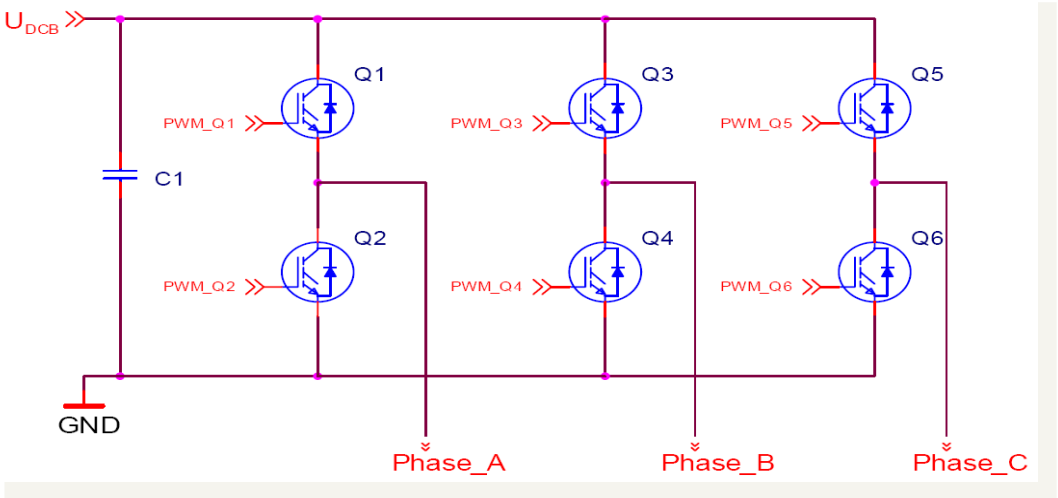


Figure 2- Load condition

Brushless DC Motor Control

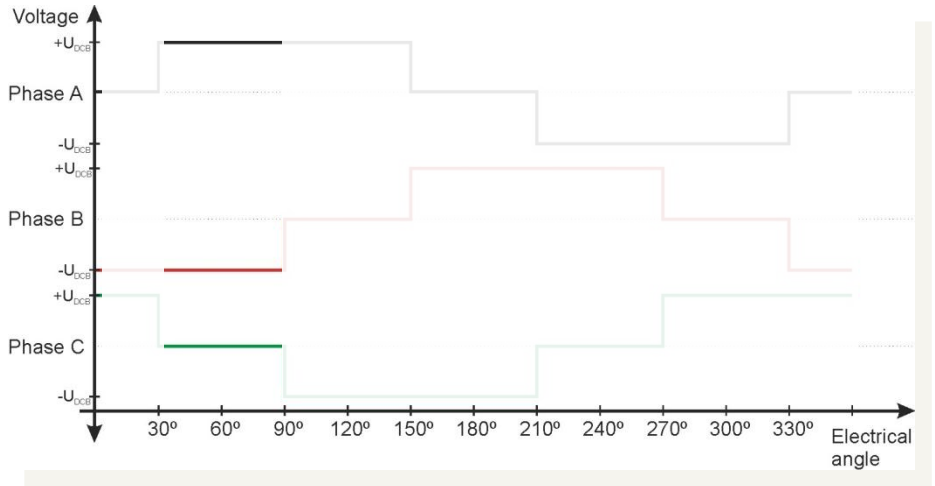
- Six Step BLDC Motor Control
  - Voltage applied on two phases only



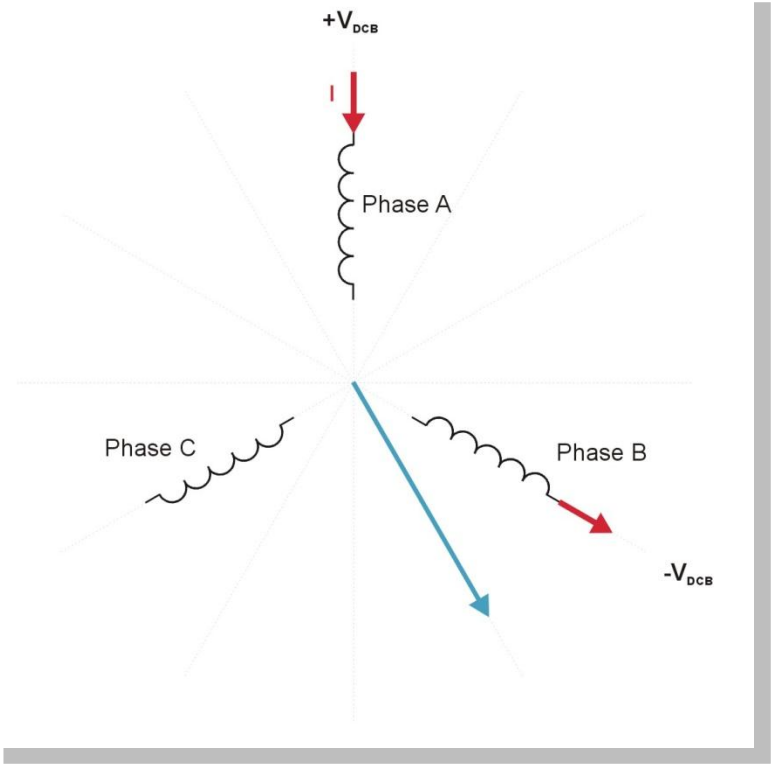
Power Stage

Brushless DC Motor Control

- Six Step BLDC Motor Control
  - Voltage applied on two phases only



Phases voltage



Brushless DC Motor Control

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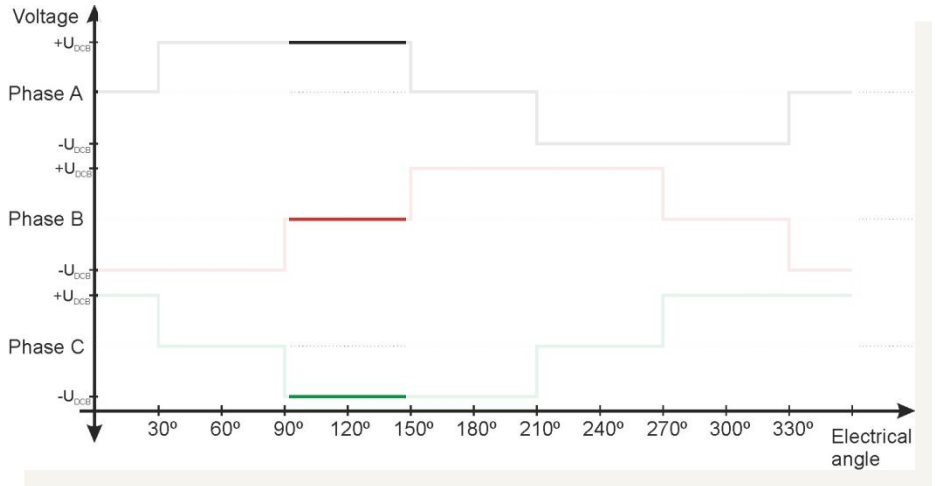
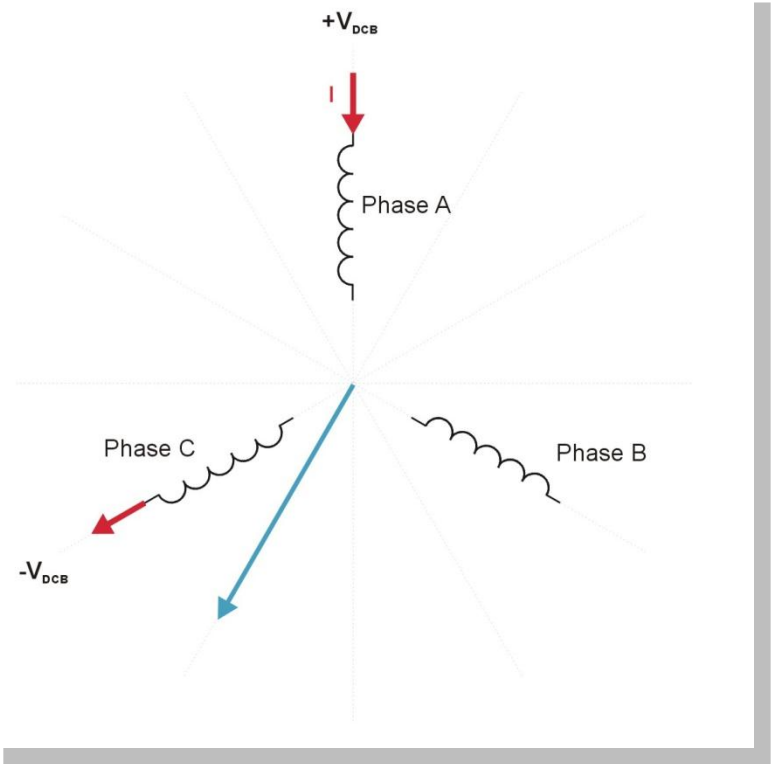


Phases voltage



Brushless DC Motor Control

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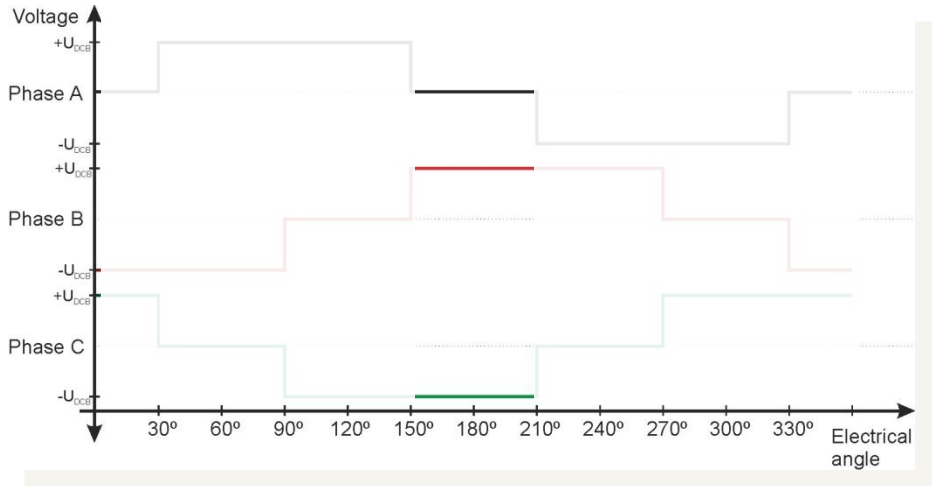
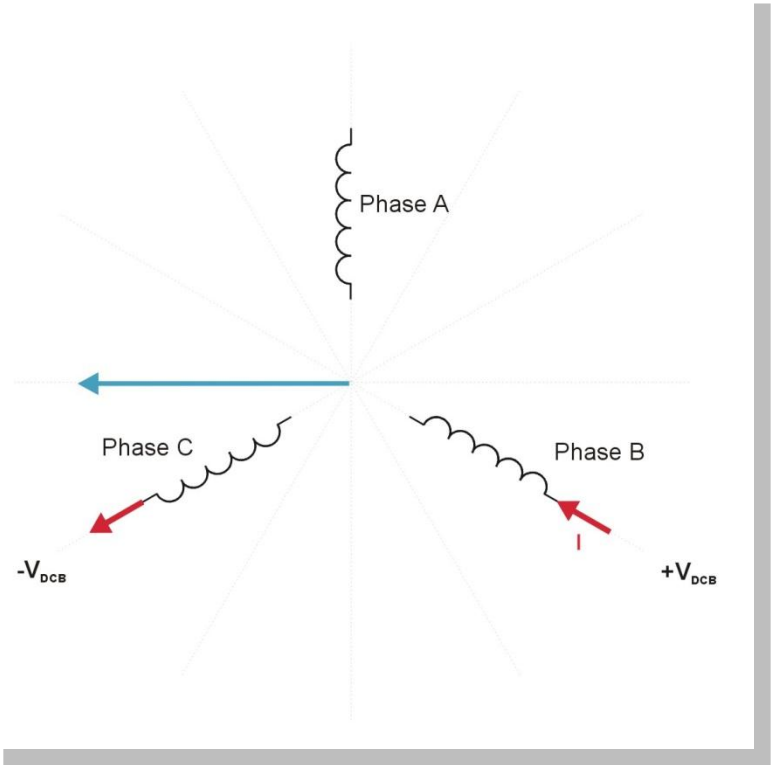


Phases voltage



Brushless DC Motor Control

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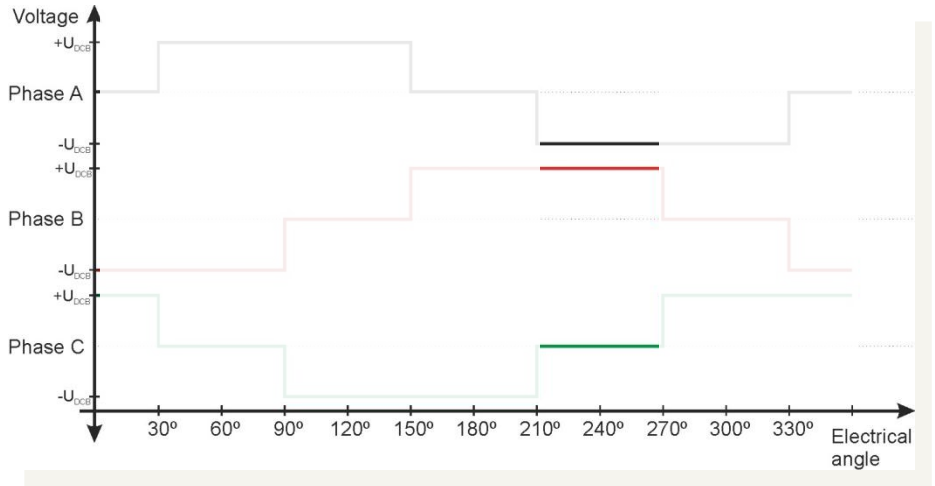
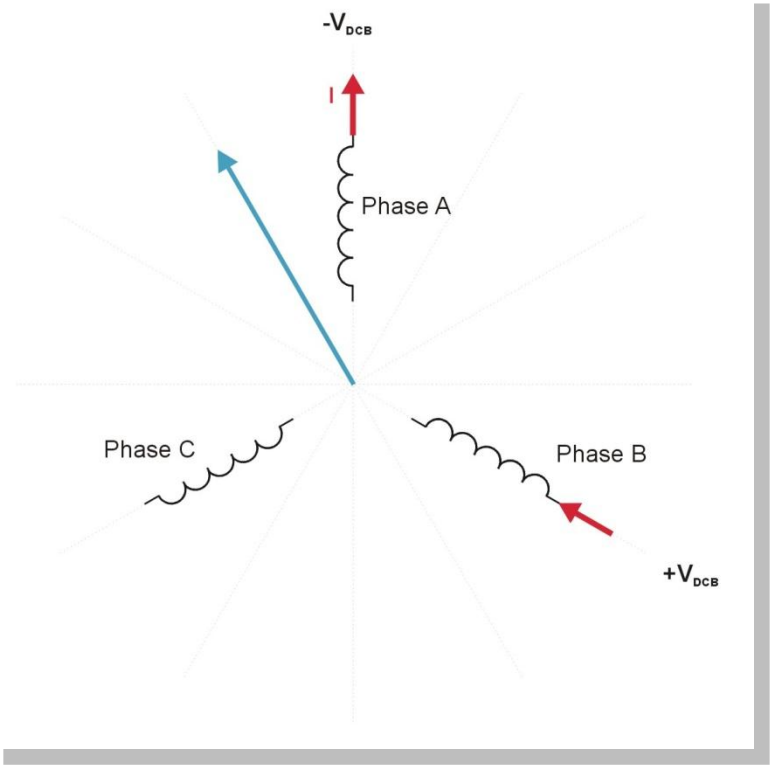


Phases voltage



Brushless DC Motor Control

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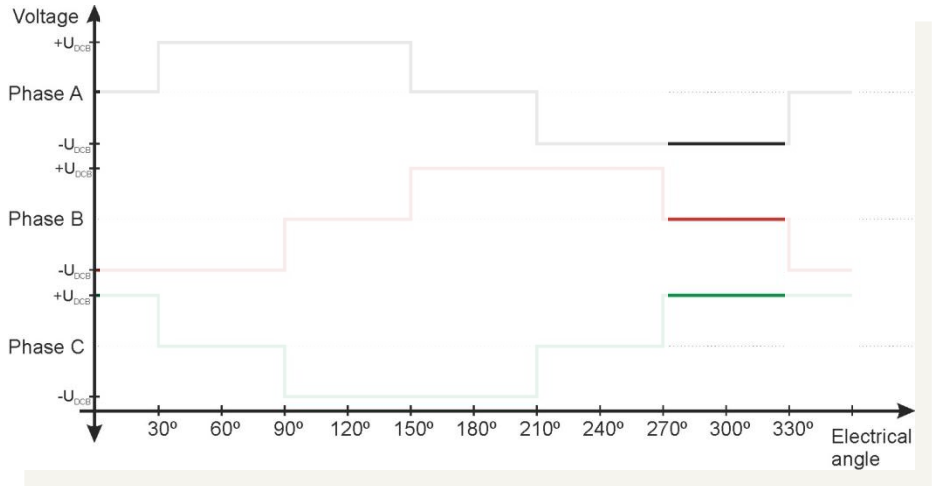
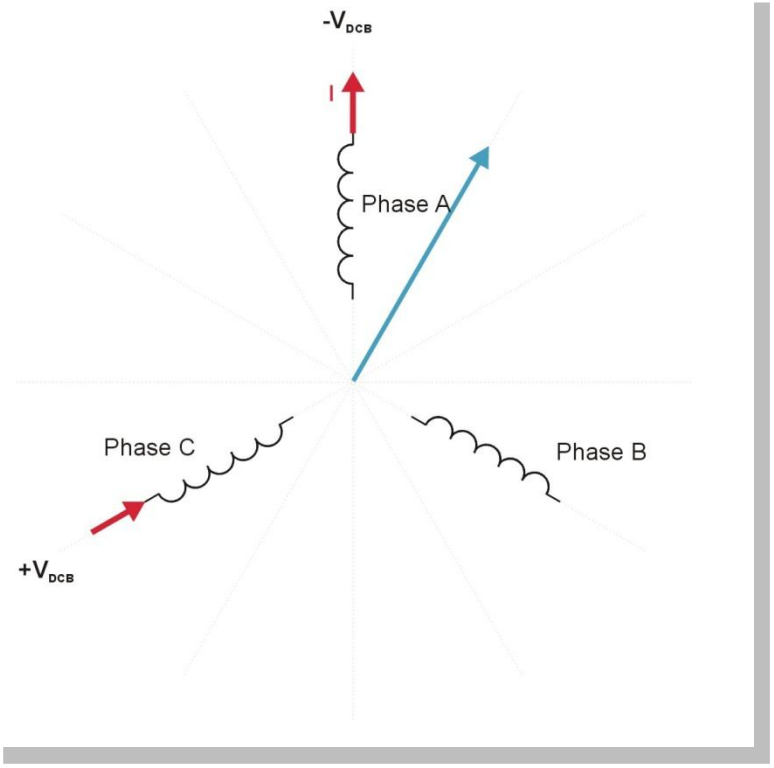
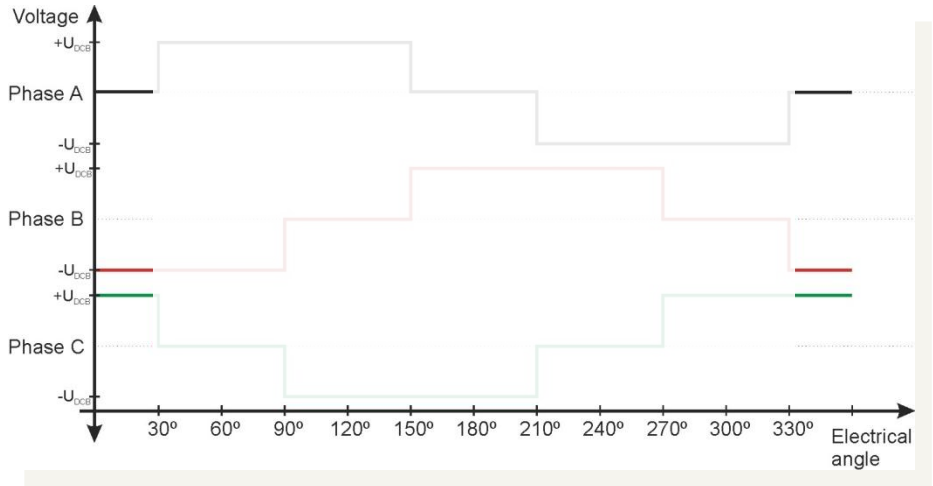


Phases voltage

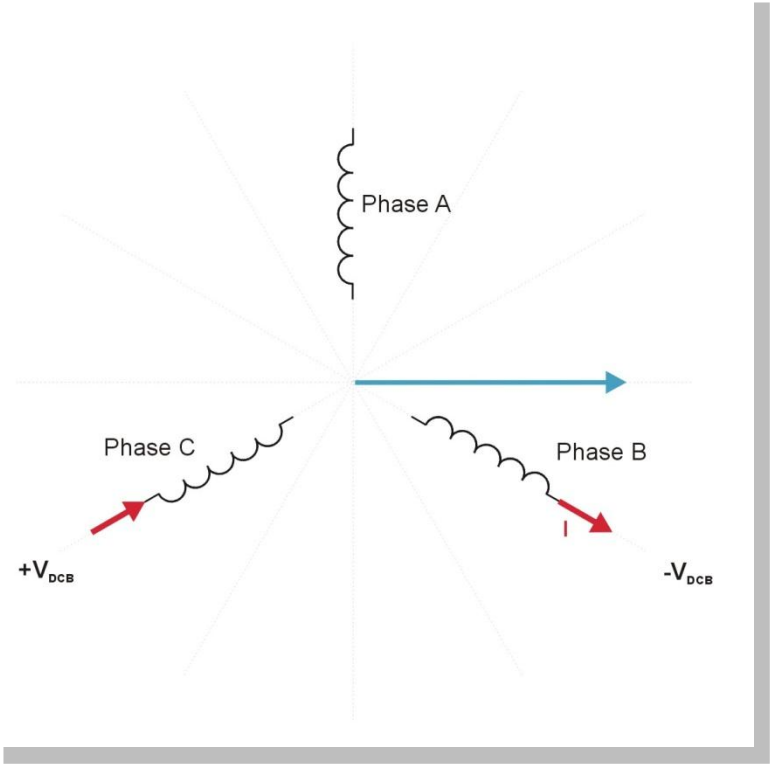


Brushless DC Motor Control

- Six Step BLDC Motor Control
  - Voltage applied on two phases only

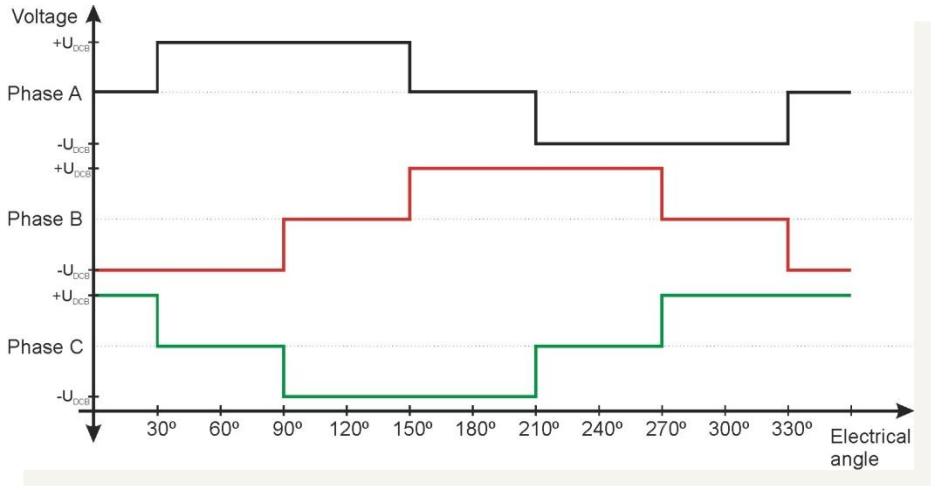


Phases voltage

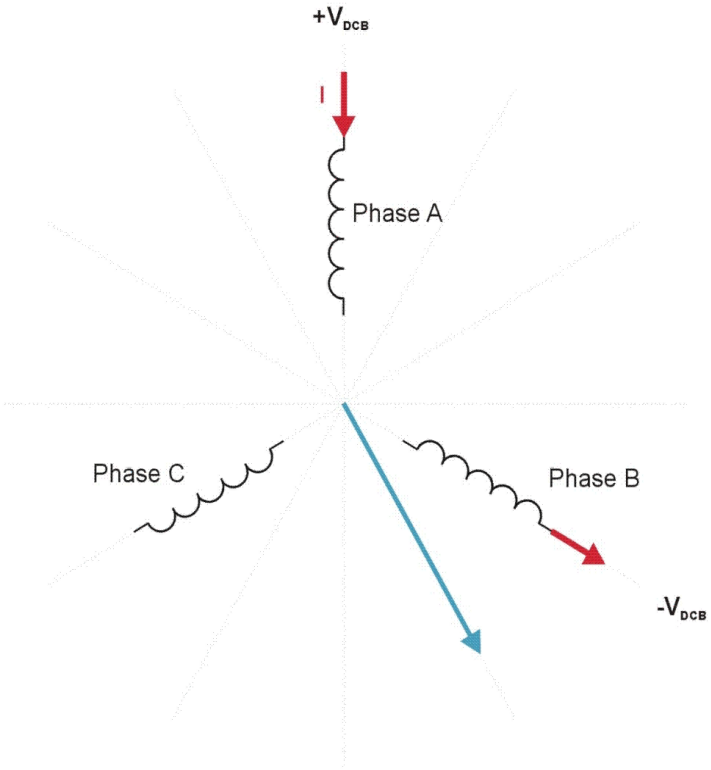


Brushless DC Motor Control

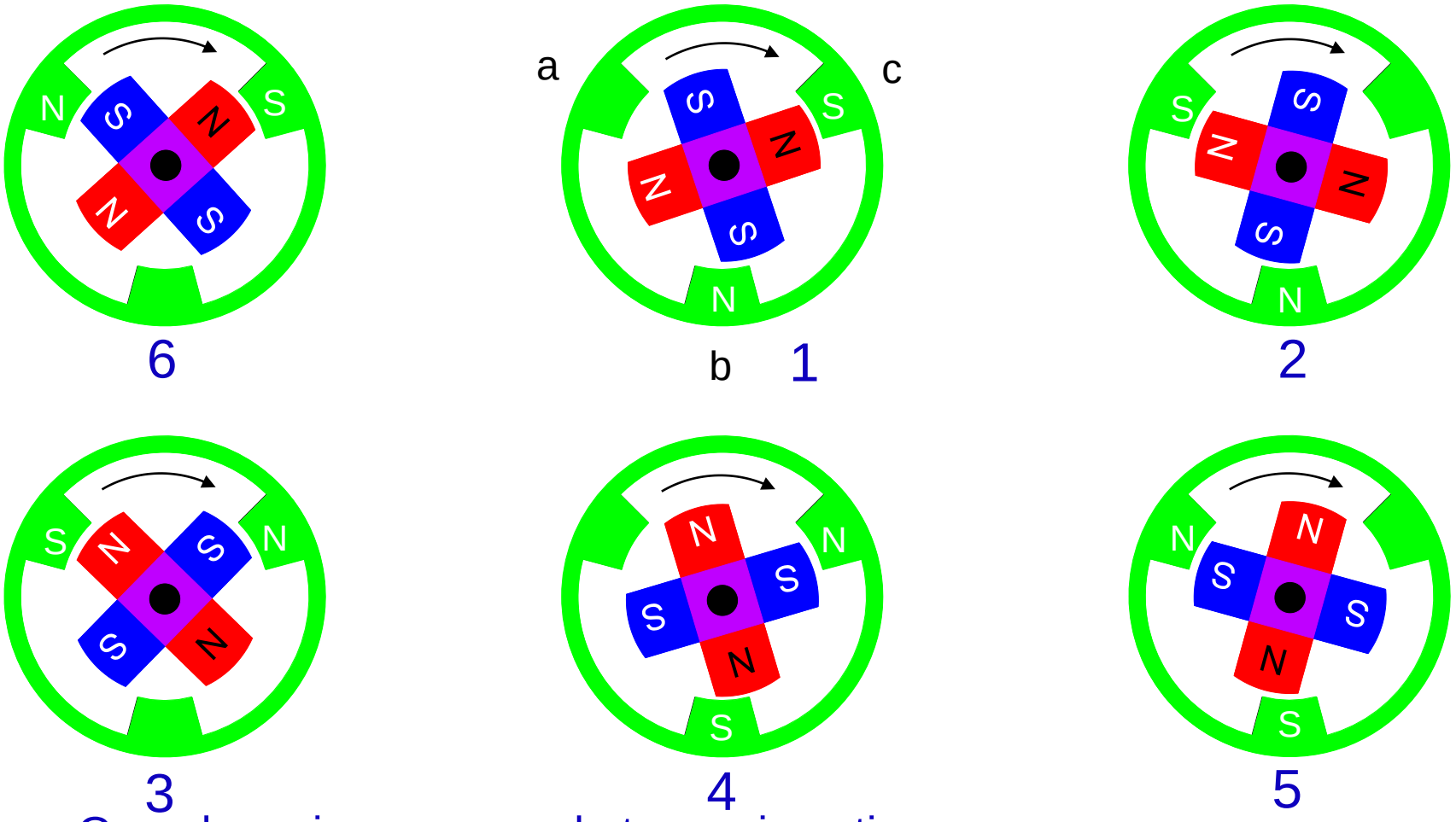
- Six Step BLDC Motor Control
  - Voltage applied on two phases only
  - It creates 6 flux vectors
  - Phases are power based on rotor position
  - The process is called Commutation



Phase voltages



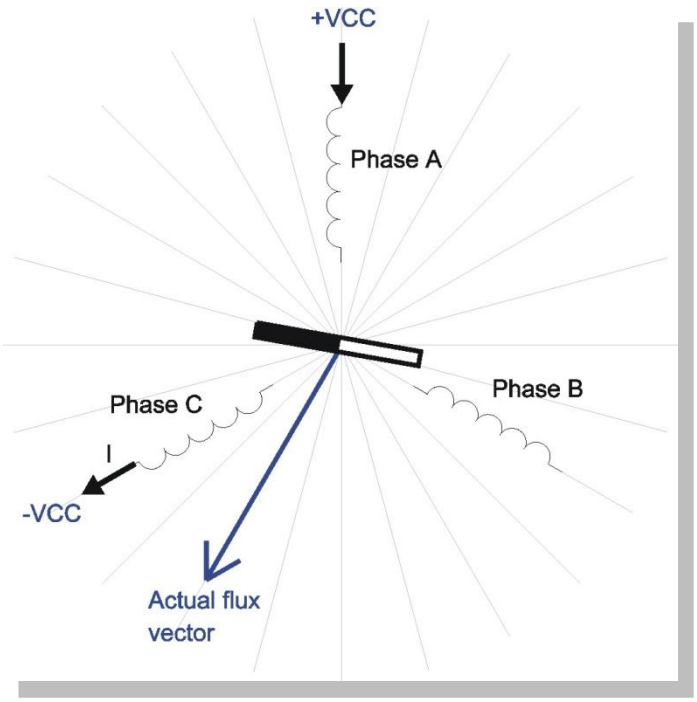
Commutation of a Brushless DC Motor



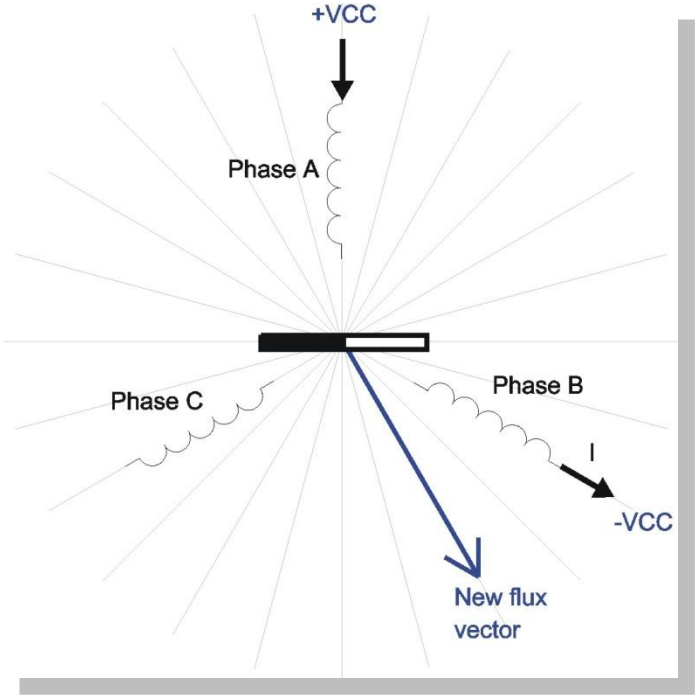
One phase is unpowered at any given time.

Brushless DC Motor Control

- Commutation example
  - Stator field is maintained 60°, 120° relative to rotor field



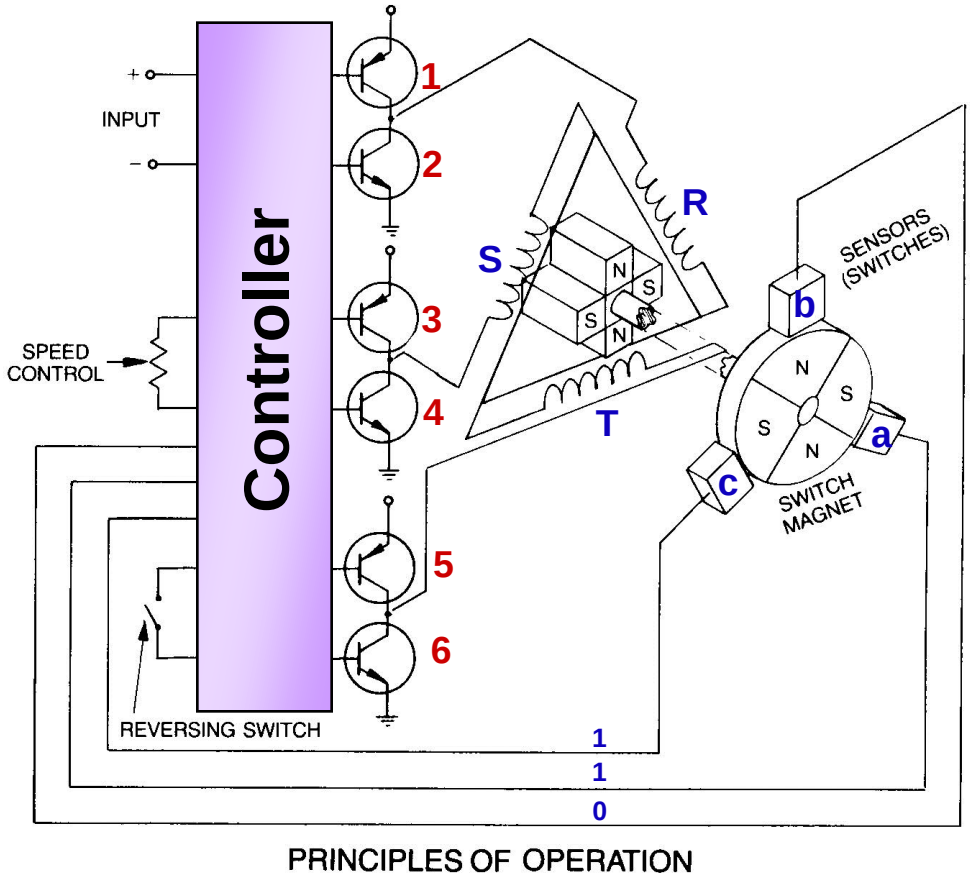
Before commutation



After commutation

Brushless DC Motor Control

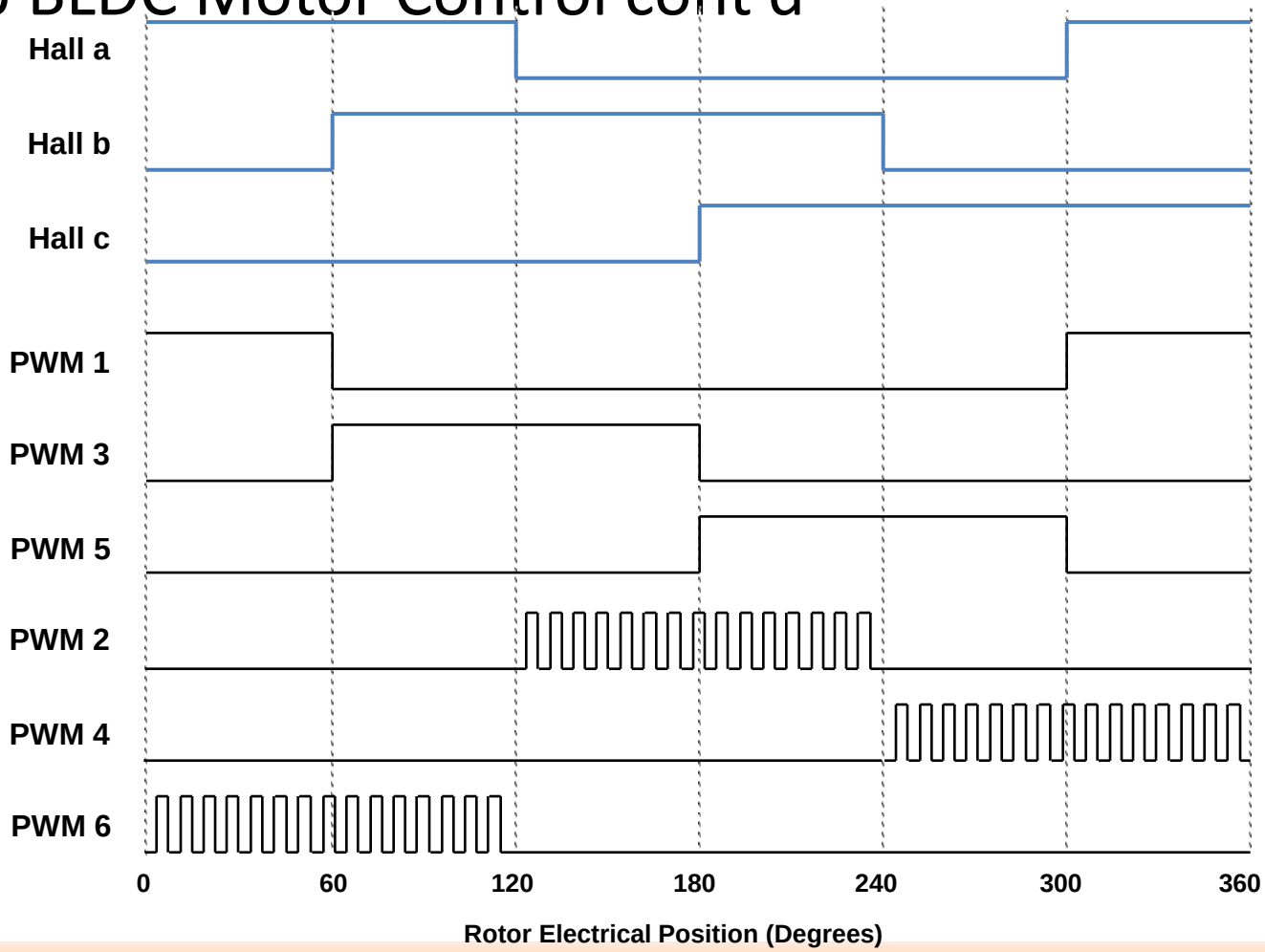
- Six Step BLDC Motor Control cont'd



Source: Eastern Air Devices, Inc. Brushless DC Motor Brochure

Brushless DC Motor Control

- Six Step BLDC Motor Control cont'd



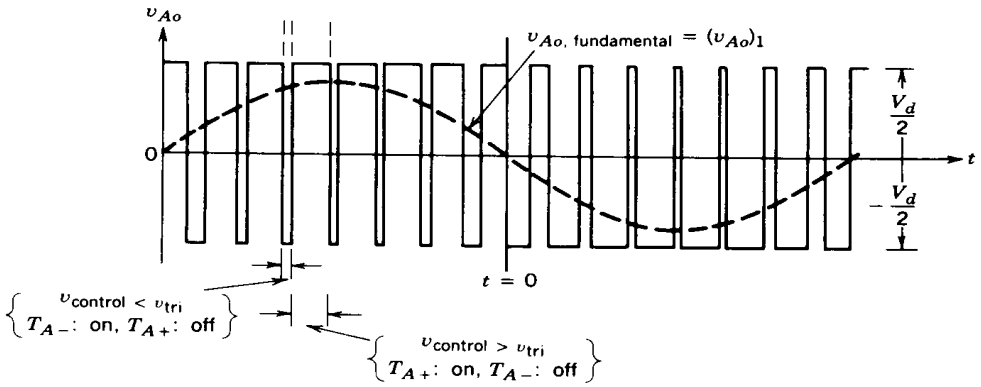
Brushless DC Motor Control

- Example of commutation table

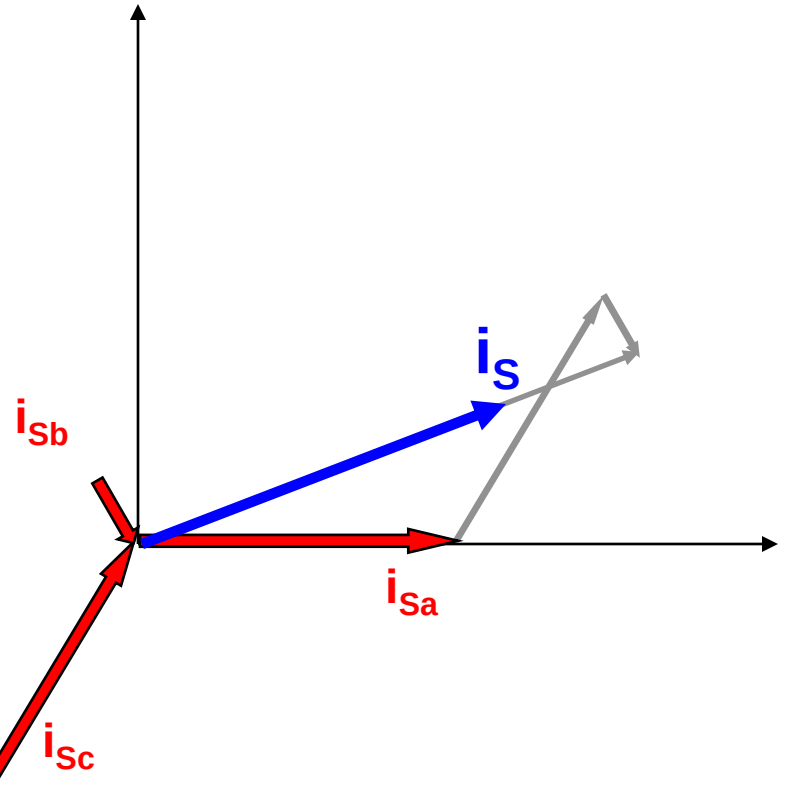
Hall Sensor A	Hall Sensor B	Hall Sensor C	Phase A	Phase B	Phase C
1	0	0	$-V_{DCB}$	$+V_{DCB}$	NC
1	0	1	NC	$+V_{DCB}$	$-V_{DCB}$
0	0	1	$+V_{DCB}$	NC	$-V_{DCB}$
0	1	1	$+V_{DCB}$	$-V_{DCB}$	NC
0	1	0	NC	$-V_{DCB}$	$+V_{DCB}$
1	1	0	$-V_{DCB}$	NC	$+V_{DCB}$

Brushless DC Motor Control

- Sinusoidal BLDC motor Control



All three phases are powered by sinewave shifted by 120°



We are able to generate stator field to any position over 360°

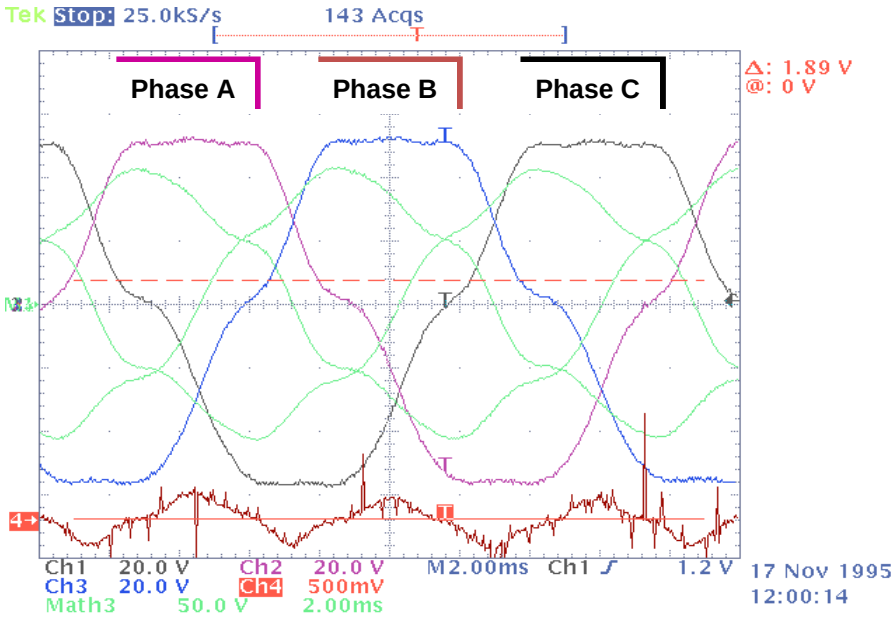
Brushless DC Motor Control Summary

- Six step control versus sinusoidal control

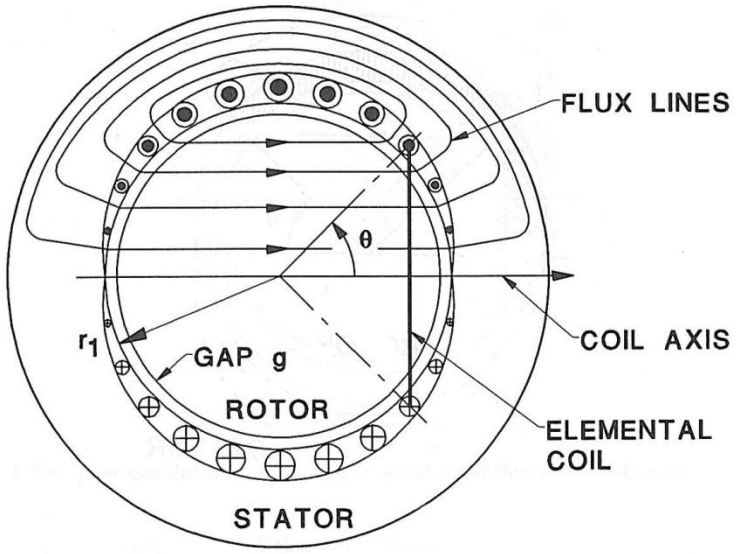
Six step control	Sinusoidal control
+ Simple PWM generation	− More complex PWM generation (sinewave has to be generated)
− Ripple in the torque (stator flux jumps by 60°)	+ Smooth torque (stator flux rotates fluently)
− A little noise operation (due to ripple in the torque)	+ Very quite
+ Simple sensor	− Requires sensor with high resolution

Brushless DC Motor Control

- BLDC Motor versus PMSM Motor
  - The both motors have identical construction. The difference is in stator winding only. The BLDC has distributed stator winding in order to have trapezoidal Back-EMF. The PMSM motor has distributed stator winding in order to have sinusoidal Back-EMF.



Trapezoidal Back-EMF voltage



Sinusoidal winding distribution

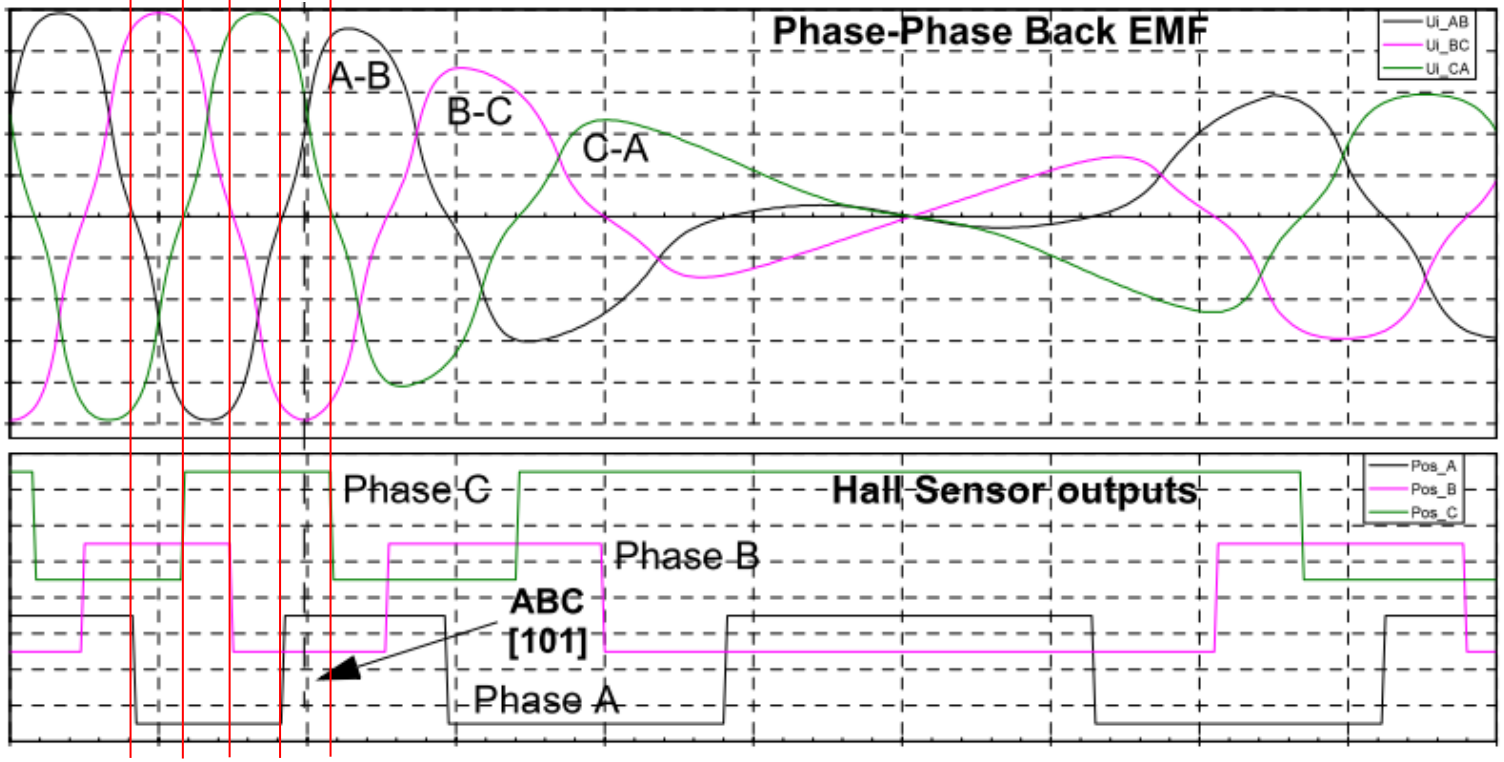
Source: Hendershot J. R. Jr, Miller TJE: Design of brushless permanent-magnet motors

Commutation Table

- The commutation table is fundamental for six step commutation BLDC control algorithm
- Motor commutates and thus rotates according to the commutation table
- The commutation table must be created depending on the actual motor configuration

Commutation Table

- Hall Sensors sense rotor flux and are aligned to phase to phase Back EMF voltage

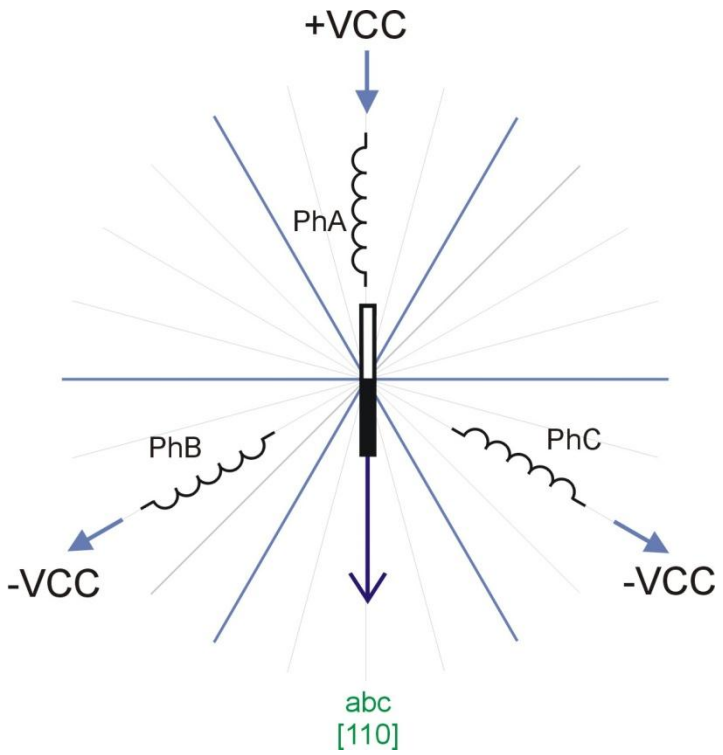


How to Get Commutation Table?

- There is a simple method using power supply with current limit
- Step 1 – Preparation for Hall Sensors measurement
  1. Mark all phases and all sensors as you want
  2. Set current limit of power supply to 20-30% of nominal motor current
  3. Choose direction of motor rotation (clockwise, counterclockwise)
  4. Connect any phase to “+” terminal
  5. Connect remain two phases to “-” terminal (All phases are always connected to power supply)

How to Get Commutation Table?

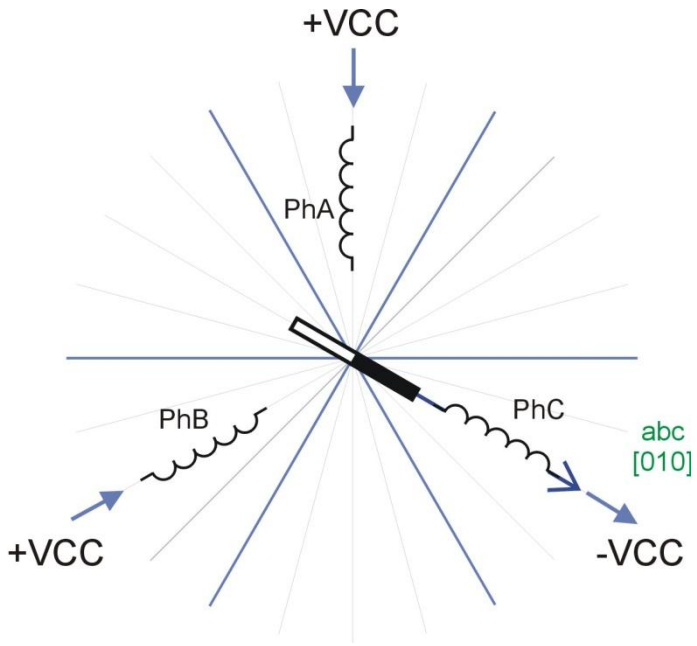
- Step 2 – Hall Sensors Measurement



Phase			Hall Sensor		
A	B	C	a	b	c
+	-	-	1	1	0

How to Get Commutation Table?

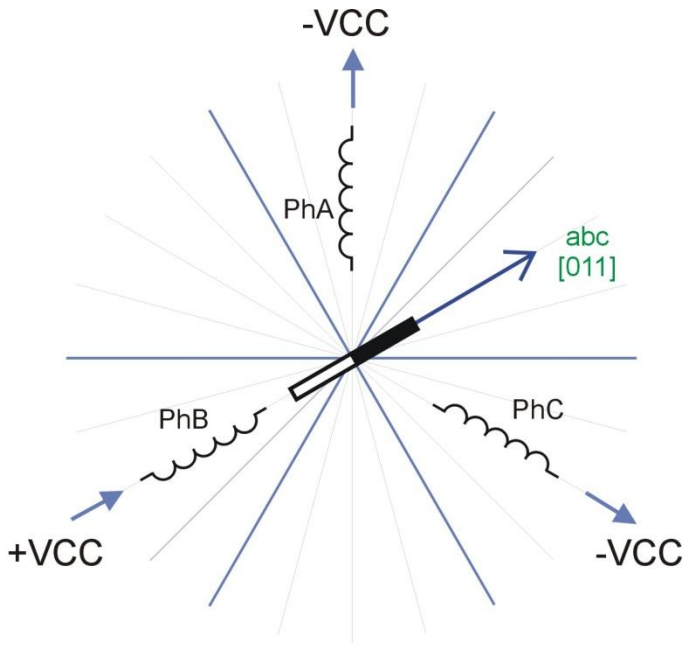
- Step 2 - Hall Sensors Measurement



Phase			Hall Sensor		
A	B	C	a	b	c
+	-	-	1	1	0
+	+	-	0	1	0

How to Get Commutation Table?

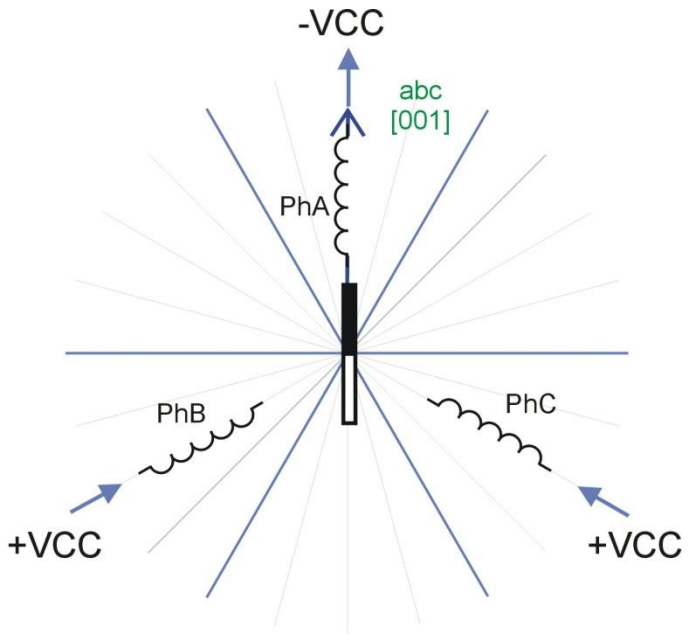
- Step 2 - Hall Sensors Measurement



Phase			Hall Sensor		
A	B	C	a	b	c
+	-	-	1	1	0
+	+	-	0	1	0
-	+	-	0	1	1

How to Get Commutation Table?

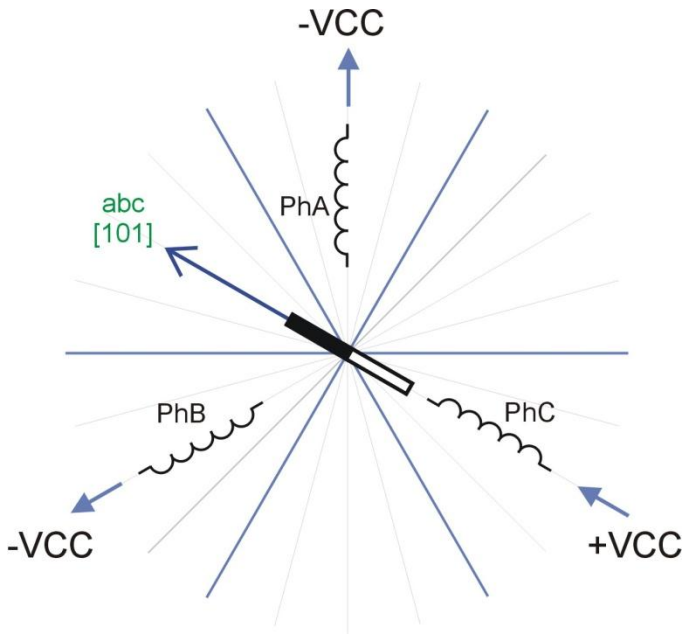
- Step 2 - Hall Sensors Measurement



Phase			Hall Sensor		
A	B	C	a	b	c
+	-	-	1	1	0
+	+	-	0	1	0
-	+	-	0	1	1
-	+	+	0	0	1

How to Get Commutation Table?

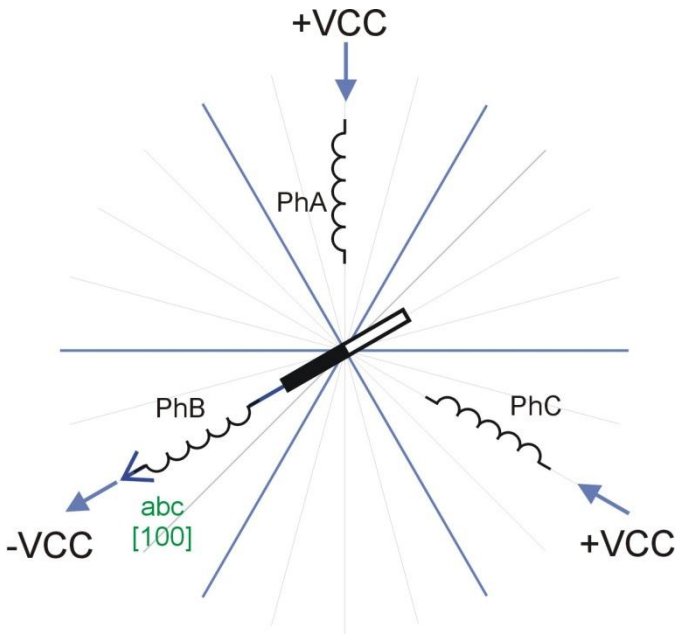
- Step 2 - Hall Sensors Measurement



Phase			Hall Sensor		
A	B	C	a	b	c
+	-	-	1	1	0
+	+	-	0	1	0
-	+	-	0	1	1
-	+	+	0	0	1
-	-	+	1	0	1

How to Get Commutation Table?

- Step 2 - Hall Sensors Measurement

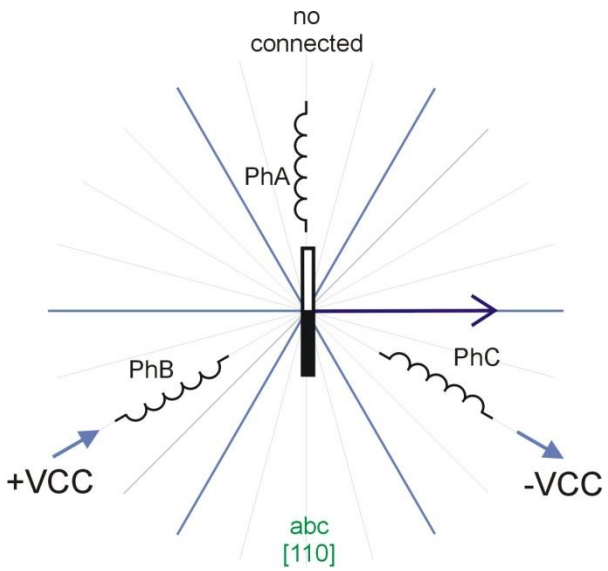


Phase			Hall Sensor		
A	B	C	a	b	c
+	-	-	1	1	0
+	+	-	0	1	0
-	+	-	0	1	1
-	+	+	0	0	1
-	-	+	1	0	1
+	-	+	1	0	0

This is not commutation table!!!

How to Get Commutation Table?

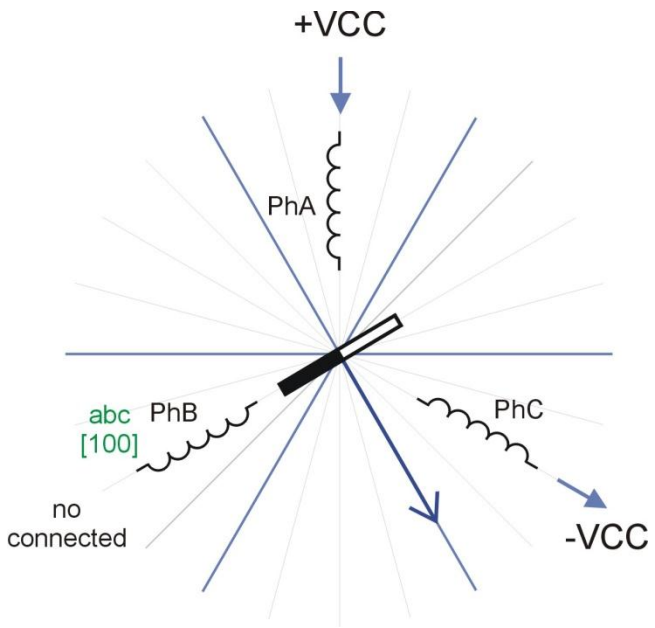
- Step 3 - Making Commutation Table



Hall Sensors			Phase		
a	b	c	A	B	C
1	1	0	NC	+	-
0	1	0			
0	1	1			
0	0	1			
1	0	1			
1	0	0			

How to Get Commutation Table?

- Step 3 - Making Commutation Table



Hall Sensors			Phase		
a	b	c	A	B	C
1	1	0	NC	+	-
0	1	0	-	+	NC
0	1	1	-	NC	+
0	0	1	NC	-	+
1	0	1	+	-	NC
1	0	0	+	NC	-

This is our commutation table

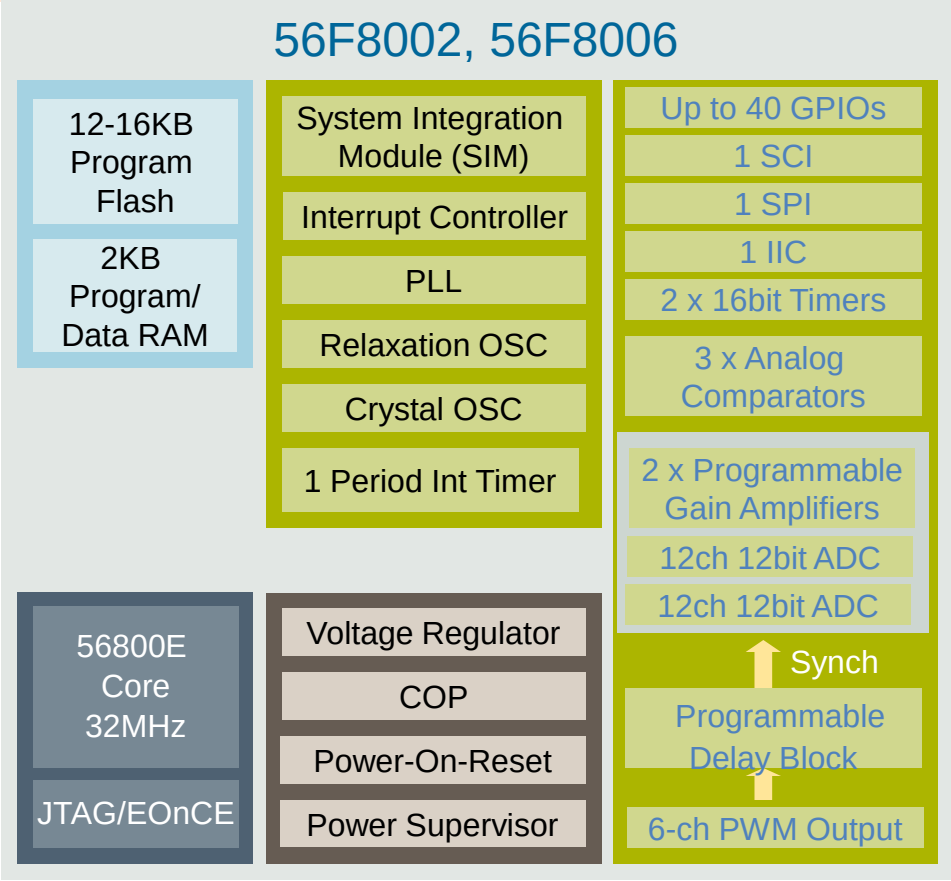
Agenda

- Separately exited DC motor
- Basic Terms
- PWM Modulation techniques for DC and BLDC drives
- BLDC Motor Theory
- Microcontroller MC56F8006
  - Microcontroller roadmap
  - Microcontroller overview
  - Peripherals

DSCS - 56F8006/2

Ultra Low Cost: 56F800x

- 32 MHz/32 MIPS 56800E core
- 1.8-3.6V operation
- 12K - 16K Bytes program FLASH with Flash security
- 2K Bytes program/data RAM
- Tunable internal relaxation oscillator and 32 KHz clock
- Phase locked loop (PLL)
- Up to 96 MHz peripherals – timers, PWM & Hi-SCI
- 6 output PWM module with 4 programmable fault inputs with selectable PWM frequency for each PWM signal complementary pair
- Two programmable gain amplifiers with x2, x4, x8, x16 gains (clocked in order to cancel input offset)
- Two 12-bit ADCs with up to 24 inputs , 2.5us per conversion
- Programmable delay block provides precise control of ADC/PGA sample times relative to PWM reload cycles
- Three high speed analog comparators
- 2 multiple function programmable timers
- Computer operating properly timer
- One periodic interval timer (PIT)
- 1 high speed serial communication interface (Hi-SCI)
- 1 serial peripheral interface (SPI)
- I^2C communications interface
- Up to 40 GPIOs – versatile pin usage
- JTAG/EOnCE™ debug port
- Industrial temperature range: -40C – 105C



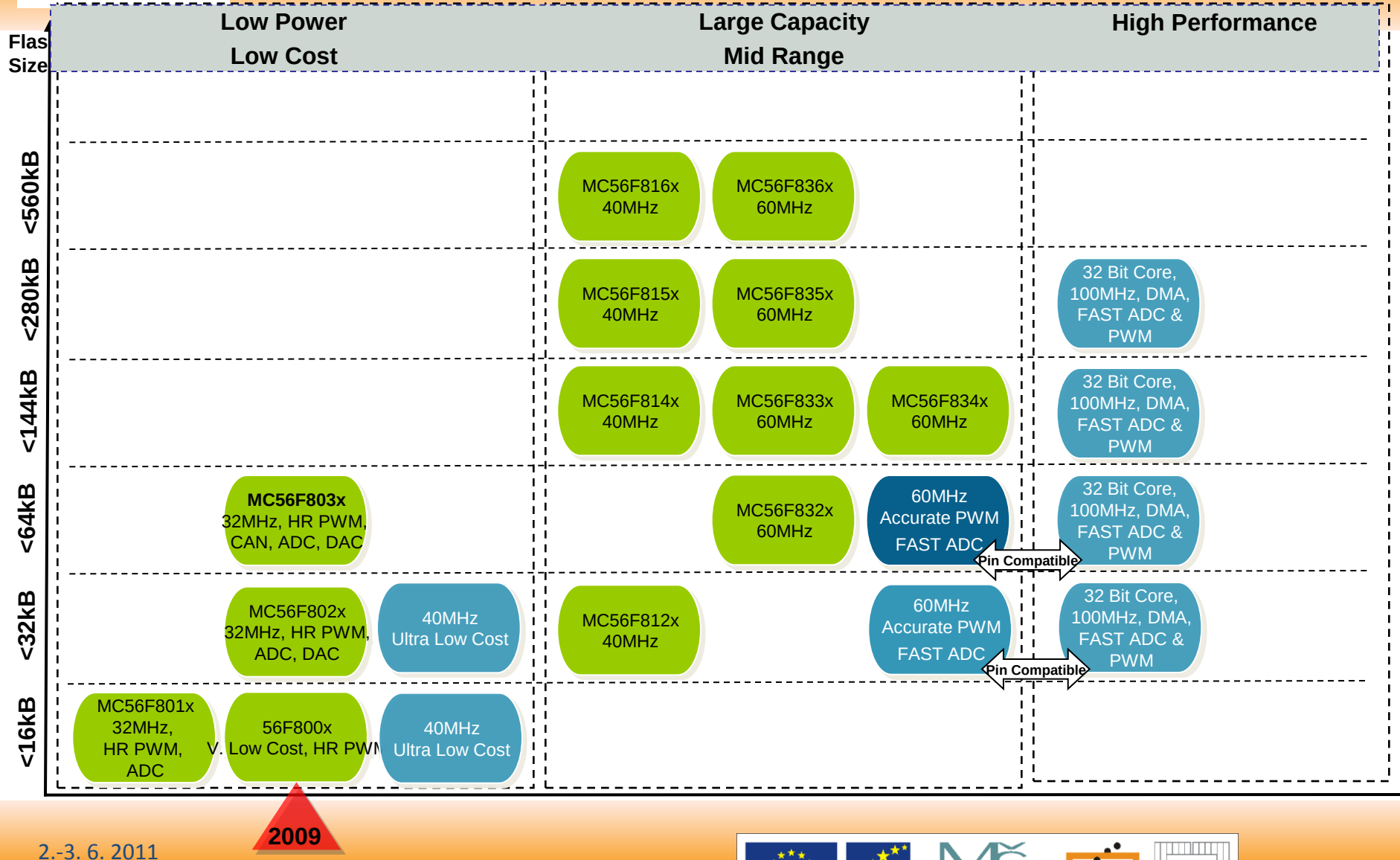
Package: 28SOIC, 32SDIP , 32LQFP, 48 LQFP

In Production

56F8000 Series Feature Summary

	56F8002	56F8006	56F8011	56F8013	56F8014	56F8023	56F8025	56F8036	56F8027/37
Performance	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs	32MHz/MIPs
Temperature Range (V)	-40C~105C	-40C~105C	-40C~125C	-40C~125C	-40C~125C	-40C~105C	-40C~105C	-40C~105C	-40C~105C
Voltage Range	1.8V - 3.6V	1.8V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V	3.0V - 3.6V
Voltage Regulator	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip
Program/Data Flash	12KB	16KB	12KB	16KB	16KB	32KB	32KB	64KB	32KB / 64KB
Program/Data RAM	2KB	2KB	2KB	4KB	4KB	4KB	4KB	8KB	4KB /8KB
Program Security	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
On Chip Relaxation Osc.	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PLL	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
COP (Watchdog)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PWM (96 Mhz Clock)	1 x 6ch	1 x 6ch	1 x 6ch	1 x 6ch	1 x 5ch	1 x 6ch	1 x 6ch	1 x 6ch	1 x 6ch
PWM Fault Inputs	4	4	4	4	3	4	4	4	4
12-bit ADCs	2 x 8ch	2 x 12ch	2 x 3ch	2 x 3ch	2 x 4ch	2 x 3ch	2 x 4ch	2 x 5ch	2 x 8ch
12-bit DACs	0	0	No	No	No	2	2	2	2 (Pinned out)
Analog Comparator	3	3	No	No	No	2	2	2	2
Prog Gain Amp	2	2	No	No	No	No	No	No	No
16-bit Timers	3	3	4	4	4	4	4	4	8
Prog. Interval Timers	1 (RTC)	1 (RTC)	No	No	No	1	3	3	3
GPIO (max) (+/-8mA)	23	40	26*	26*	26*	26*	35*	39*	53*
IIC	1	1	1	1	1	1 - QIIC	1 - QIIC	1 - QIIC	1 - QIIC
SCI (UART) / LIN Slave	1 - SCI	1 - SCI	1 - SCI	1 - SCI	1 - SCI	1 - QSCI	1 - QSCI	1 - QSCI	1 - QSCI
SPI (Synchronous)	1 - SPI	1 - SPI	1 - SPI	1 - SPI	1 - SPI	1 - QSPI	1 - QSPI	1 - QSPI	1 - QSPI
CAN	No	No	No	No	No	No	No	MSCAN	MSCAN
JTAG/EOnCE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Power Consumption	IDD = 45.6mA;IDDA = 4.5mA		IDD = 42mA; IDDA = 13.5mA			IDD = 48mA; IDDA = 18.8mA		IDD = 48mA; IDDA = 18.8mA	
Package	32LQFP (.8p)	28SOIC 32LQFP 32SDIP 48LQFP	32LQFP	32LQFP	32LQFP	32LQFP	44LQFP	48LQFP	64LQFP

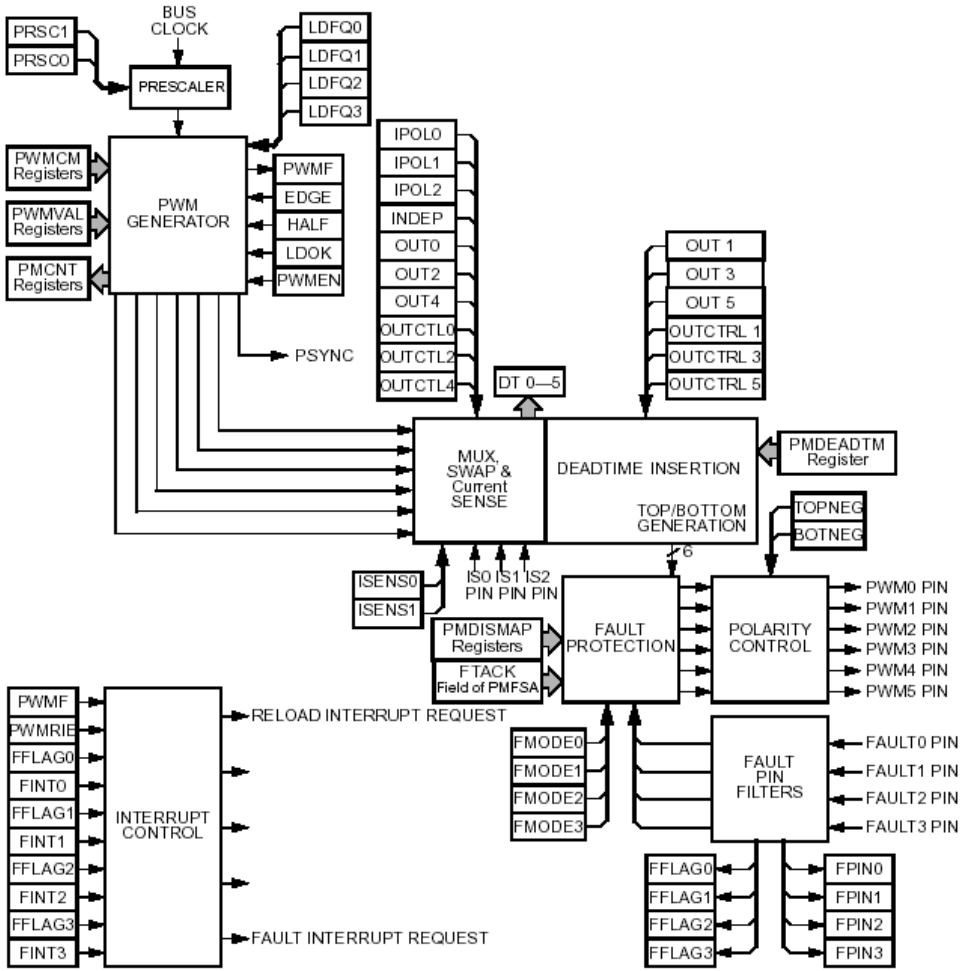
DSC Roadmap


Low Power
Low Cost
Large Capacity
Mid Range
High Performance
Flas
Size
<560kB
<280kB
<144kB
<64kB
<32kB
<16kB
MC56F816x
40MHz
MC56F836x
60MHz
MC56F815x
40MHz
MC56F835x
60MHz
32 Bit Core,
100MHz, DMA,
FAST ADC &
PWM
MC56F814x
40MHz
MC56F833x
60MHz
MC56F834x
60MHz
MC56F803x
32MHz, HR PWM,
CAN, ADC, DAC
MC56F832x
60MHz
60MHz
Accurate PWM
FAST ADC
Pin Compatible
MC56F802x
32MHz, HR PWM,
ADC, DAC
40MHz
Ultra Low Cost
MC56F812x
40MHz
Pin Compatible
MC56F801x
32MHz,
HR PWM,
ADC
56F800x
V. Low Cost, HR PWM
40MHz
Ultra Low Cost
2009

Pulse Width Modulator

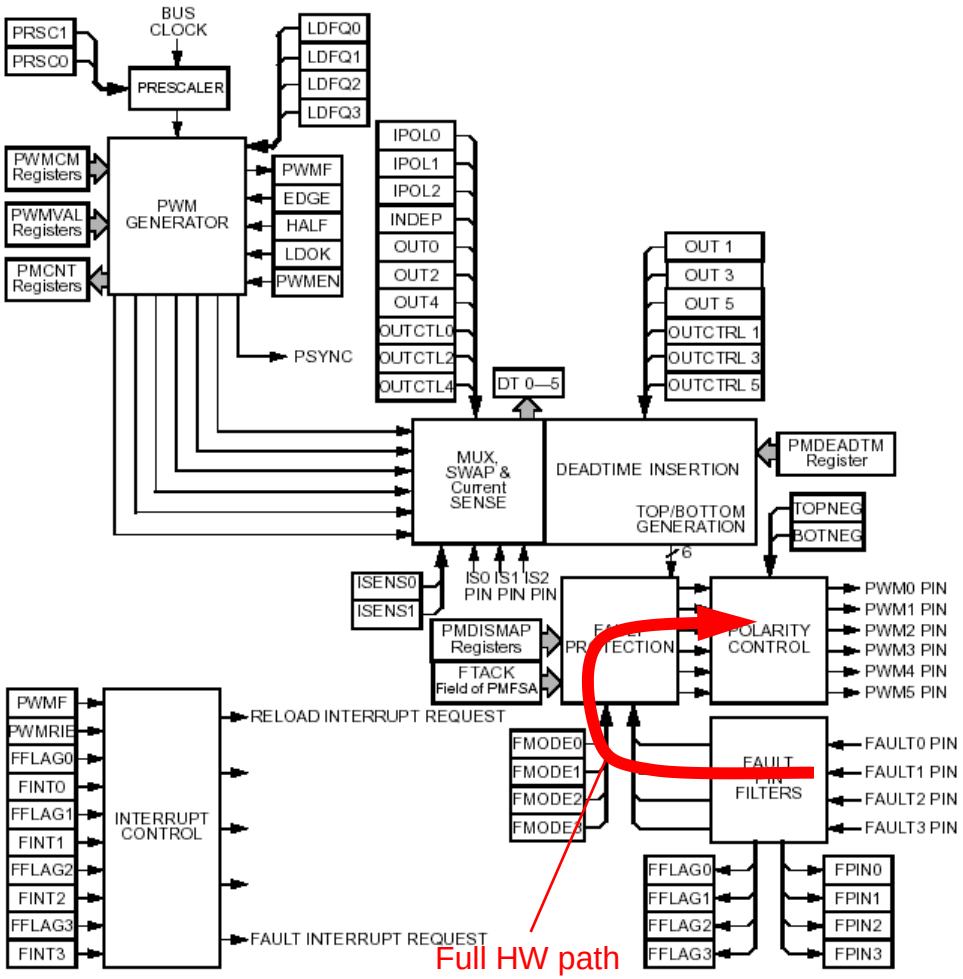
- **Up to 96 MHz operation**
- **Six PWM signals**
  - All independent
  - Complementary pairs
  - Mix independent and complementary
- **Features of complementary channel operation**
  - Independent top and bottom deadtime insertion
  - Separate top and bottom pulse width correction via current status inputs or software
  - Separate top and bottom polarity control
  - Can be controlled from internal PWM generator, software, external digital pins, timers or results of ADC
- **Edge- or Center-Aligned PWM signals**
- **Asymmetric PWM outputs**
- **15-bits of resolution**
- **Half-cycle reload capability**
- **Integral reload rates from 1/2 to 16**
- **Individual software controlled PWM output**
- **Programmable fault protection**
- **Write protected registers**
  - Protection for key parameters

DSC56F80xx Pulse Width Modulator



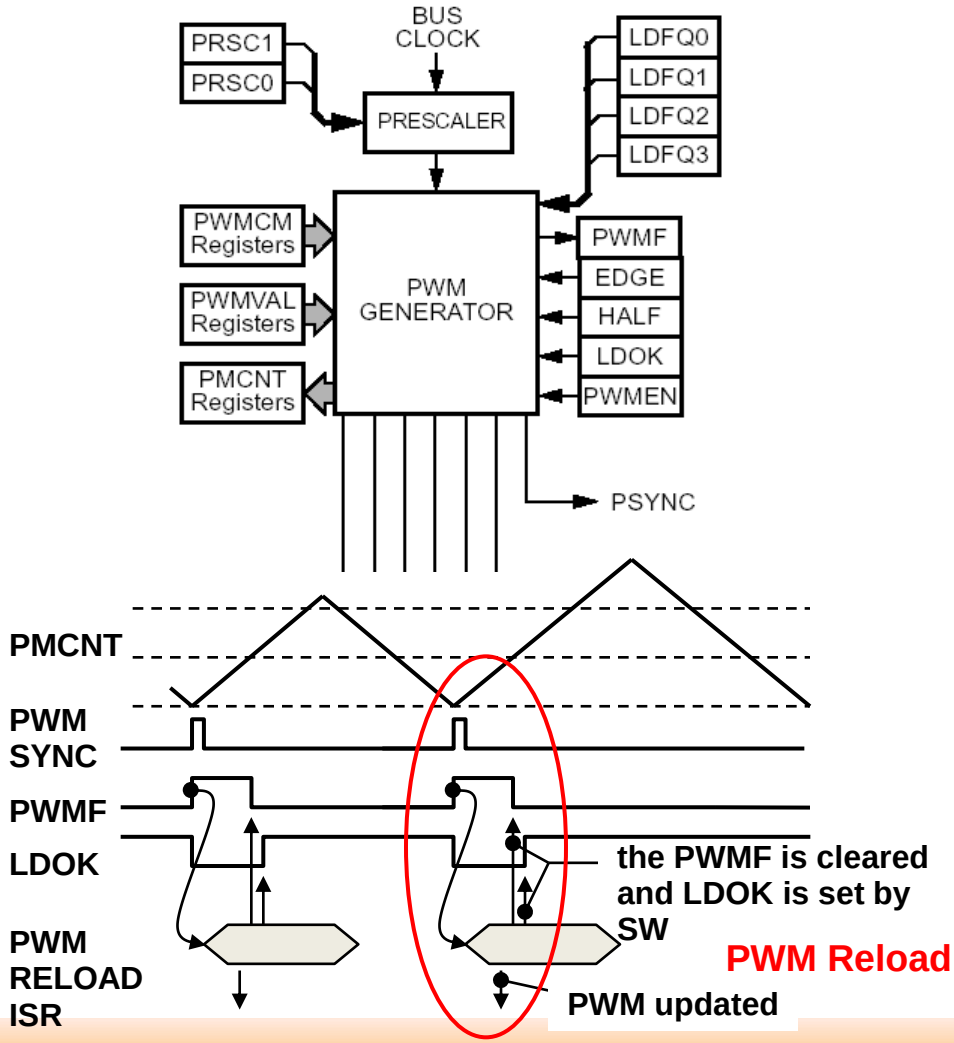
- **Safety** - Write protected registers
- Prescaler
- PWM Generator
- MUX Swap & Current sense
- Deadtime Insertion Top/Bottom Generation
- Software Output Control
- Fault Protection
- Fault Pin Filters
- Polarity Control
- Interrupt Control

PWM - Safety



- **Safety critical setting can be protected** by the write-protect bit (WP).
  Once set **it prevents** any further **writes to write-protected registers or bits**.
  Protection can be cleared only by RESET !
- The list of write-protected registers (their bits) and functions:
  - **PWM polarity**
  - **Complementary PWM pair operation**
  - **Centre aligned PWM channels**
  - **Deadtime value**
  - **PWM fault disable mapping matrix**
  - **HW acceleration features**
  - **PWM generator channels swapping**
  - **Enable PWM in Debug or Wait mode bits**
  - **56F80x Compatibility bit**
- The functions which are still available:
  - PWM Value setting, PWM Frequency setting
  - PWM Clock Prescaller setting
  - PWM Re-load Frequency + Half Cycle reload
  - Deadtime Correction Method setting, odd/even PWMVALx selection for Deadtime Correction
  - Fault Interrupts Enable/Disable, Fault Clearing Mode selection, Fault acknowledging
  - PWM Pins SW Output Control
  - PWM channels masking.
- **At fault the PWM's are forced to INACTIVE state ! It is faster than tri-stating PWM's.**

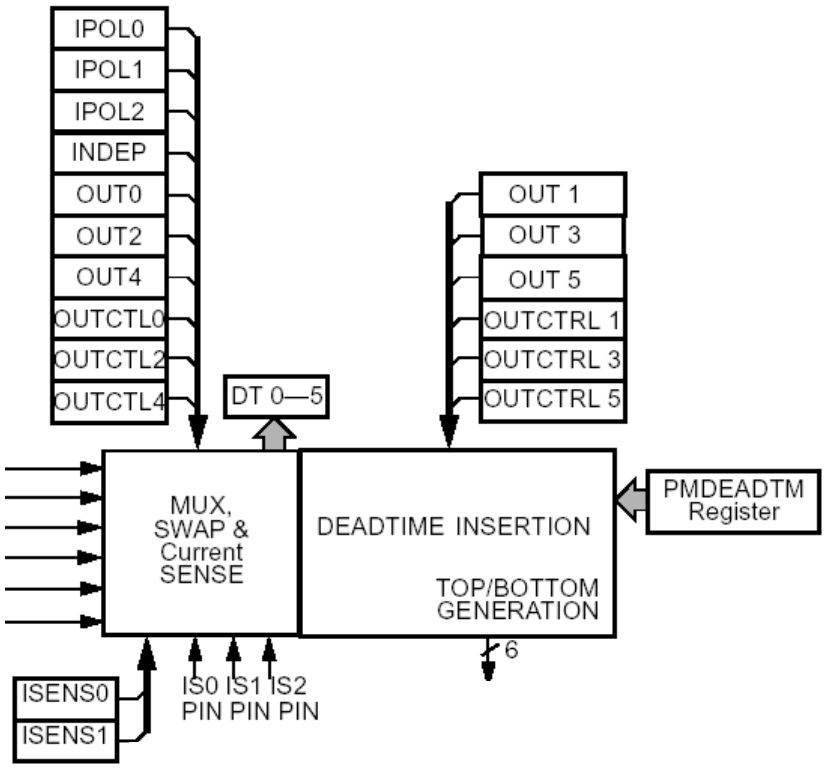
PWM - 6xPWM Generator



- **Prescaler** - 1, 2, 4, 8
- **PWM Generator**
  - **Contains up/down counter counts**
    - 15 bit resolution
    - up to 96 MHz max → 10.417 nsec resolution
  - **Alignment** - edge/centre-aligned
  - **Period** - set by PWM Counter Modulus
  - **Pulse Widths** - defined by PWM Value Registers
    Resolution:
    - 12.2bit @ 20 kHz PWM(edge-aligned)
    - 11.2bit @ 20 kHz PWM(centre-aligned)
  - **Reload Frequency** - half to 16 cycles
  - **Load Enable** interlock bit - prevents reloading of the PWM parameters before software is finished calculating them - **coherent update**
  - **Synchronization output** - high-true pulse occurs for each PWM reload
  - **HW Acceleration** - enables multi-write access of the PWM Value Registers

PWM Reload Interlock Mechanism for Coherent PWM Update

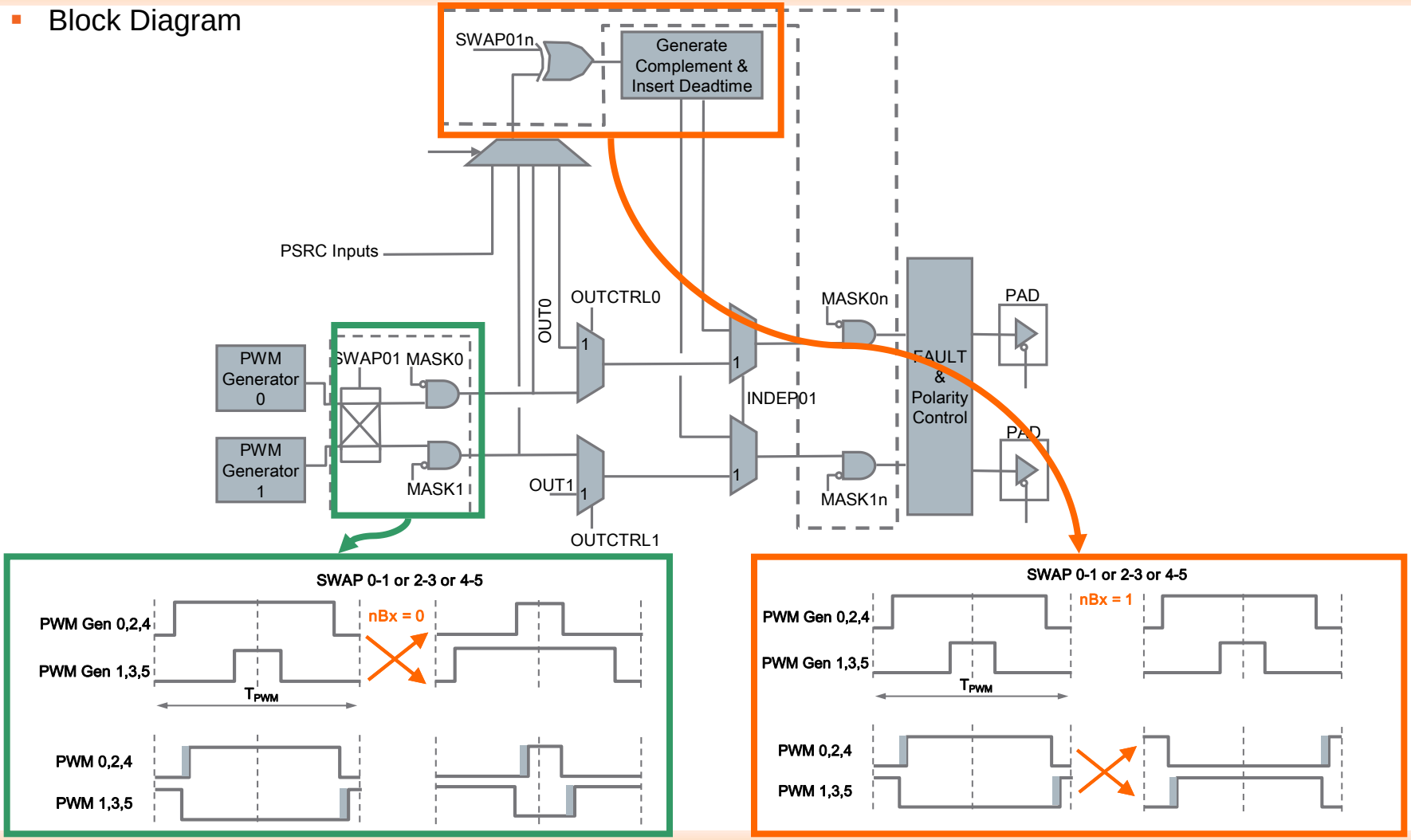
PWM - MUX, SWAP, MASK, Deadtime, SW OUT CTRL



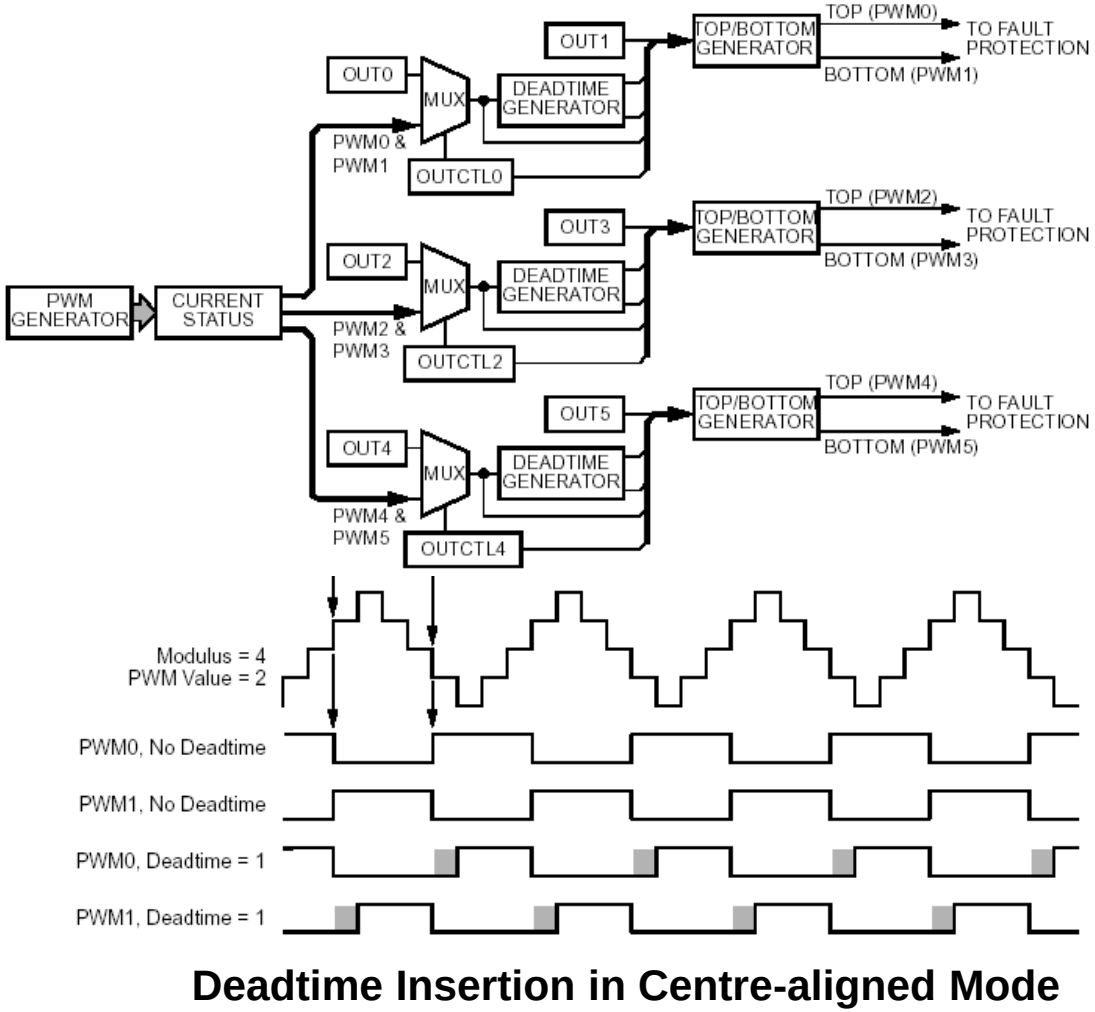
- **MUX Swap & Current sense**
  - **Channel Mask & Swap** - individually swaps and masks PWM generator channels
  - **MUX & Current Sense** - enables SW Output Control and Dead time correction
  - **SW Output Control** - individually controls the PWM outputs with respect to deadtime and complementary operation settings
- **Deadtime Insertion & Top/Bottom Generation**
  - Deadtime generators automatically insert software-selectable “deadtimes” into each pair of PWM outputs
  - The Pulse Module Deadtime register specifies the number of PWM clock cycles to use for deadtime delay
  - Every time the deadtime generator inputs changes state, deadtime is inserted
- **Software Output Control**
  - In an independent mode the output bit OUTx controls the PWMx channel.
  - In a complementary channel operation the OUT0/2/4 bits control the top/bottom pair.

PWM – Mux and Swap Options

- Block Diagram



PWM - Deadtime Generators

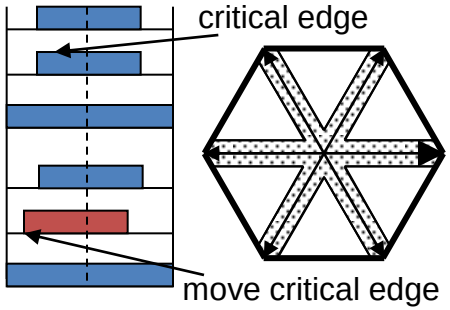


Deadtime Insertion in Centre-aligned Mode

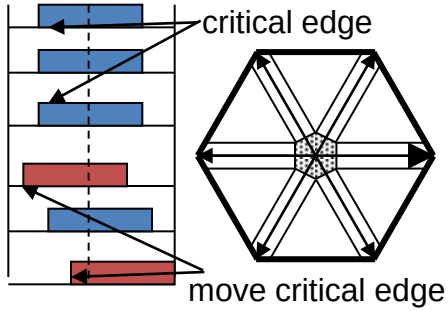
- **Deadtime Generators**
  - Deadtime generators automatically insert software-selectable “deadtimes” into each pair of PWM outputs
  - Every time the deadtime generator inputs changes state, deadtime is inserted
  - In Software Output Control
    - Deadtime generators continue to insert deadtime whenever an OUT0/2/4 bit toggles.
    - Deadtime is not inserted when the OUT1/3/5 bit toggles.
  - The Pulse Module Deadtime register specifies the number of PWM clock cycles to use for deadtime delay

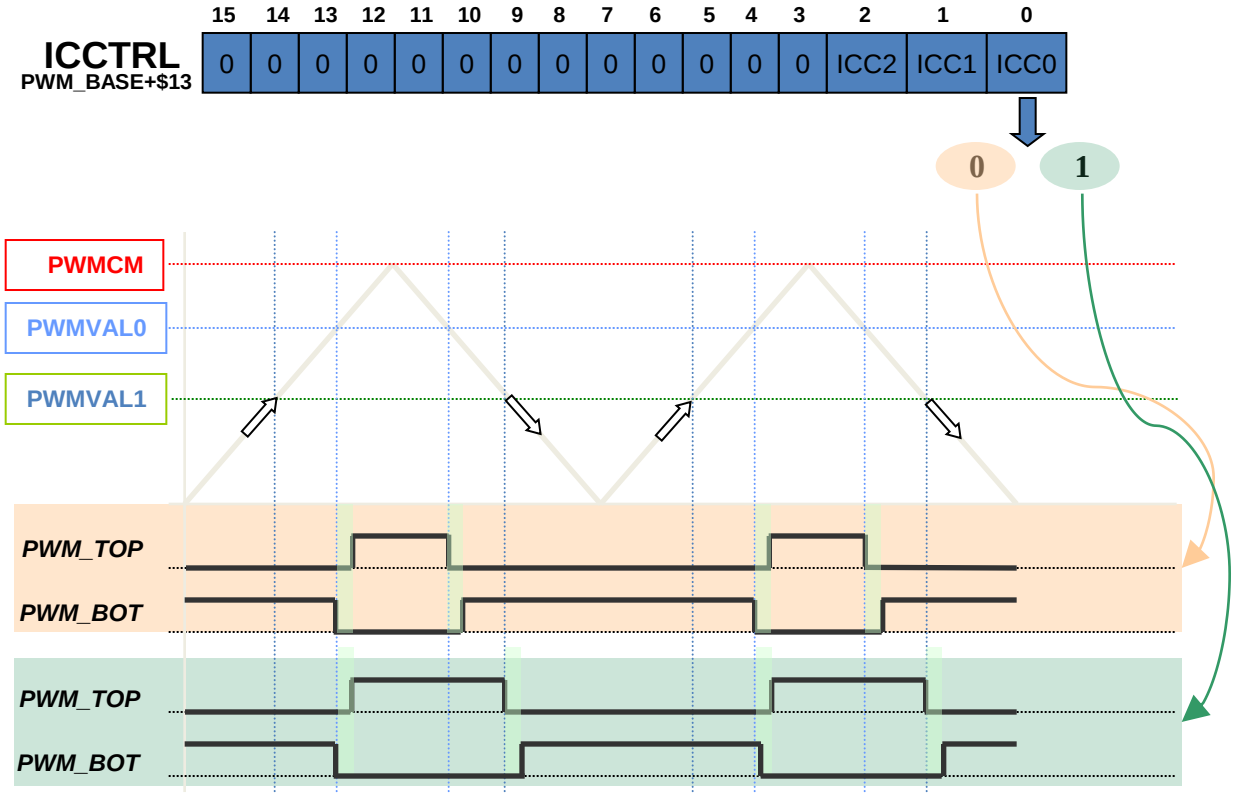
PWM – Asymmetrical Generation

- Passing active vector



- Low modulation index



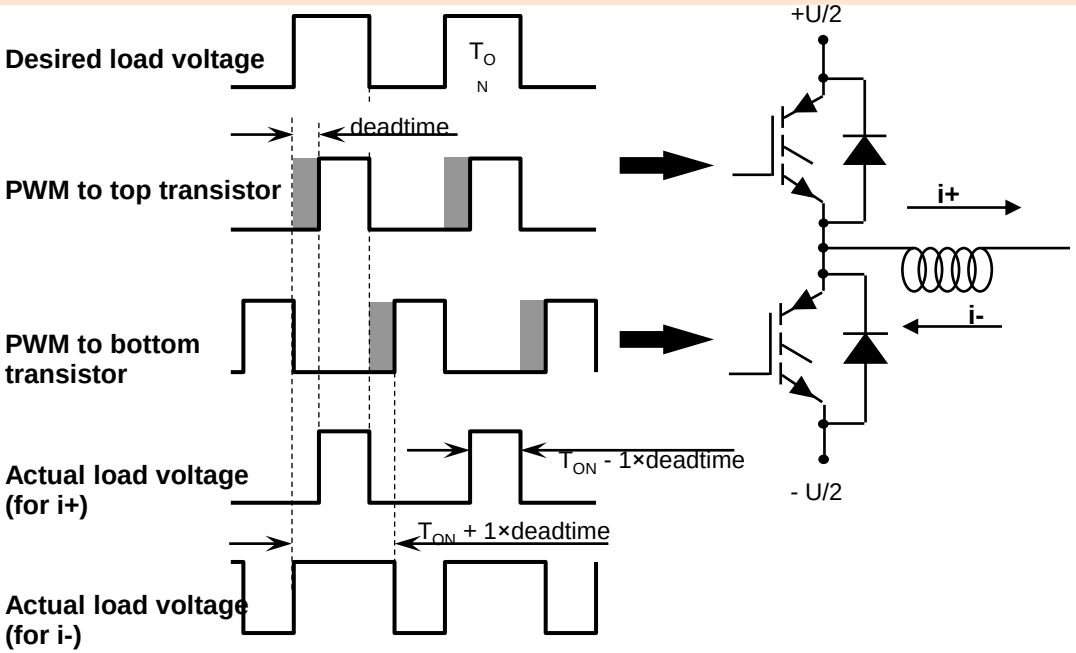


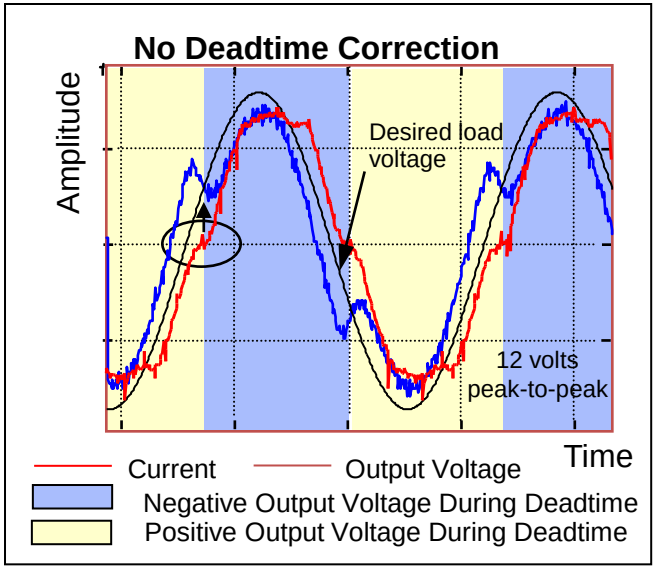
PWM - SW Output Control - Details

OUTx bit	Complementary channel operation	Independent channel operation
OUT0	1—PWM0 is active + deadtime insertion 0—PWM0 is inactive	1—PWM0 is active 0—PWM0 is inactive
OUT1	1—PWM1 is complement of PWM 0 0—PWM1 is inactive	1—PWM1 is active 0—PWM1 is inactive
OUT2	1—PWM2 is active + deadtime insertion 0—PWM2 is inactive	1—PWM2 is active 0—PWM2 is inactive
OUT3	1—PWM3 is complement of PWM 2 0—PWM3 is inactive	1—PWM3 is active 0—PWM3 is inactive
OUT4	1—PWM4 is active + deadtime insertion 0—PWM4 is inactive	1—PWM4 is active 0—PWM4 is inactive
OUT5	1—PWM5is complement of PWM 4 0—PWM5 is inactive	1—PWM5 is active 0—PWM5 is inactive

- ✓ **Complementary channel pairs still cannot be active simultaneously !**
  The OUT0/2/4 replace the PWM generator outputs as inputs to the deadtime generators.
  Deadtime generators continue to insert deadtime whenever an OUT0/2/4 bit toggles.
  Deadtime is not inserted when the OUT1/3/5 bit toggles.
- ✓ **Setting the OUTCTLx bits does not disable the PWM generators and current status sensing circuitry!**
  They continue to run, but no longer control the output pins.
  When the OUTCTLx bits are cleared, the outputs of the PWM generator become the inputs to the deadtime generators at the **beginning of the next PWM cycle**.
- ✓ **Software can drive the PWM outputs even when PWM enable bit (PWMEN) is set to zero.**
- ✓ **During software output control, TOPNEG and BOTNEG still control output polarity !**

PWM - Distortion Caused by Inductive Loads



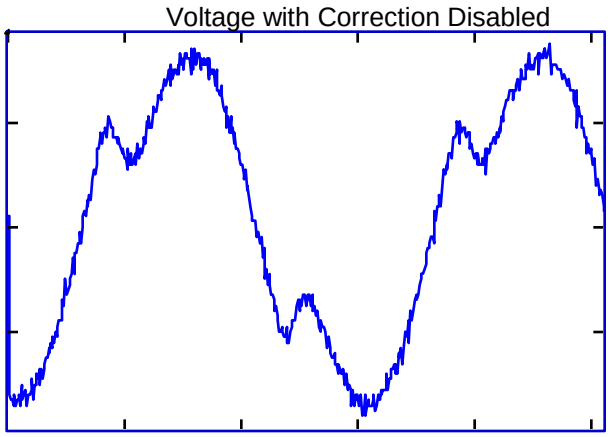


- ✓ Both transistors are "off" during deadtime. **Load inductance** keeps current flowing through the diodes and thus **defines an output voltage**.
- ✓ **Positive current flow** causes negative output voltage during deadtime – **top transistor controls output voltage.**
- ✓ **Negative current flow** causes positive output voltage during deadtime – **bottom transistor controls output voltage.**

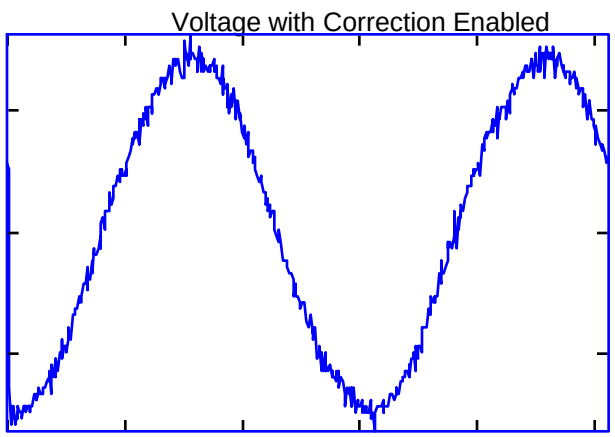
- ✓ **Causes poor low-speed motor performance**
- ✓ **Torque ripple**
- ✓ **Distorts current**
- ✓ **Produces noise in audible region**

PWM - Patented PWM Distortion Correction

Actual waveforms taken on a 1/2 horsepower motor



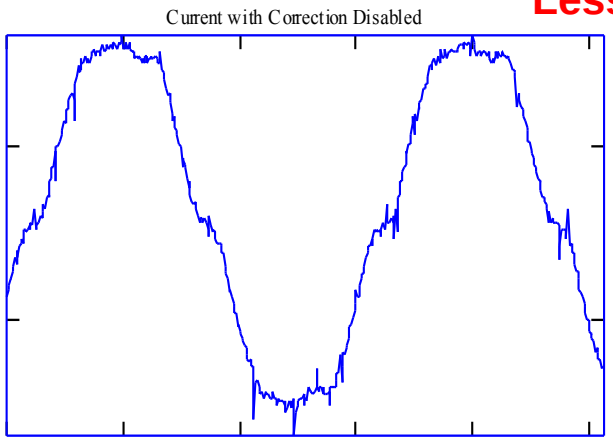
Motor Voltage



Before

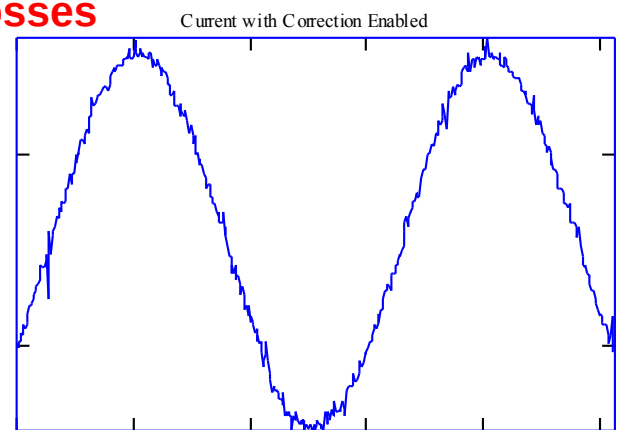
Quieter operation
Smoother operation
Less motor harmonic losses

After



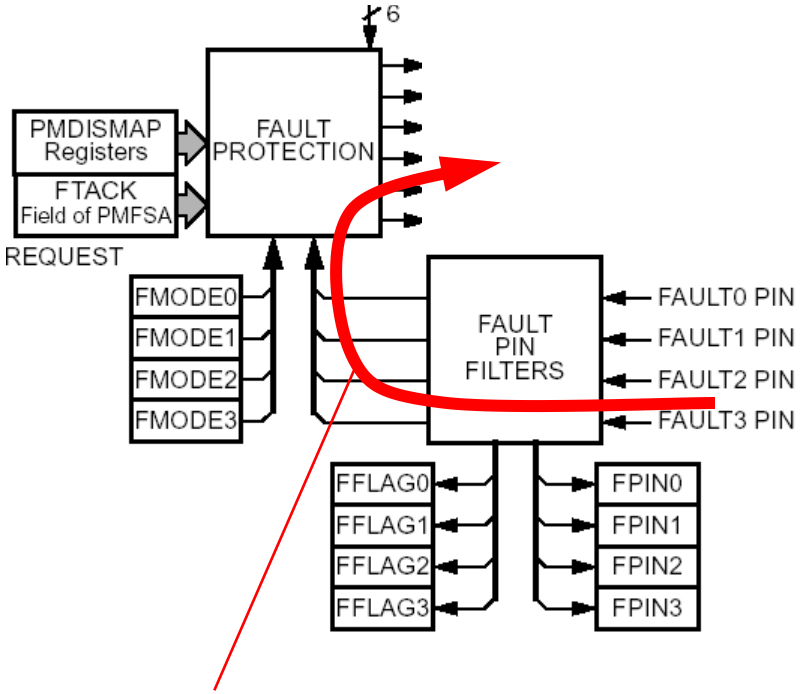
Motor Current

1/2 horse 3 phase motor
PWM Frequency = 7.3 KHz
Dead Time = 3 uS
Output ω = 1.7 Hz.



More details in dedicated presentation

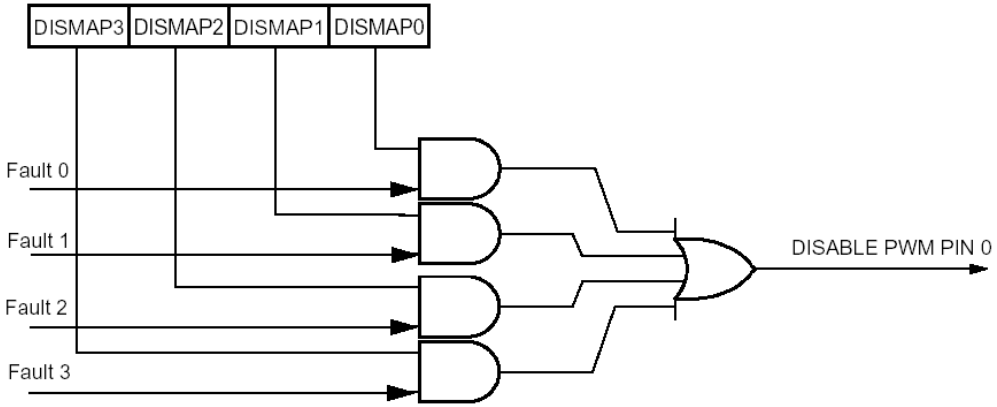
PWM - Fault Protection



Full HW path

- **Fault Protection**
  - **Fault protection can automatically disable any combination of PWM pins !**
  - Faults are generated by a logic 1 on any of the FAULT pins.
  - **When fault occurs, only the output pins are deactivated - the PWM generator continues to run !**
  - **The fault protection is enabled even when the PWM is not enabled**. Service faults before PWM enable.
  - **Automatic Fault Clearing -** the disabled PWM pins are enabled when the FAULTx pin returns to logic 0 and a new PWM half cycle begins.
  - **Manual Fault Clearing**
    - FAULT0/2 - the disabled PWM pins are enabled when software clears the FFLAGx flag + next PWM half cycle begins regardless of the logic level detected by the filter at the fault pin.
    - FAULT1/3 - the disabled PWM pins are enabled when software clears the FFLAGx flag + the filter detects a logic zero on the fault pin at the start of the next PWM half cycle.
- **Fault Pin Filters**
  - After every IPBus cycle setting the FAULTx pin at logic 0, the filter synchronously samples the pin once in each of the next two cycles. If both samples are logic 1s, the corresponding fault bits (FAULTx, FPINx, FAULTx, FFLAGx) are set.
  - The FPINx bit remains set until the pin returns to logic 0 and the filter samples a logic 0 synchronously once in the following IPbus cycle.

PWM - Fault Pins Mapping



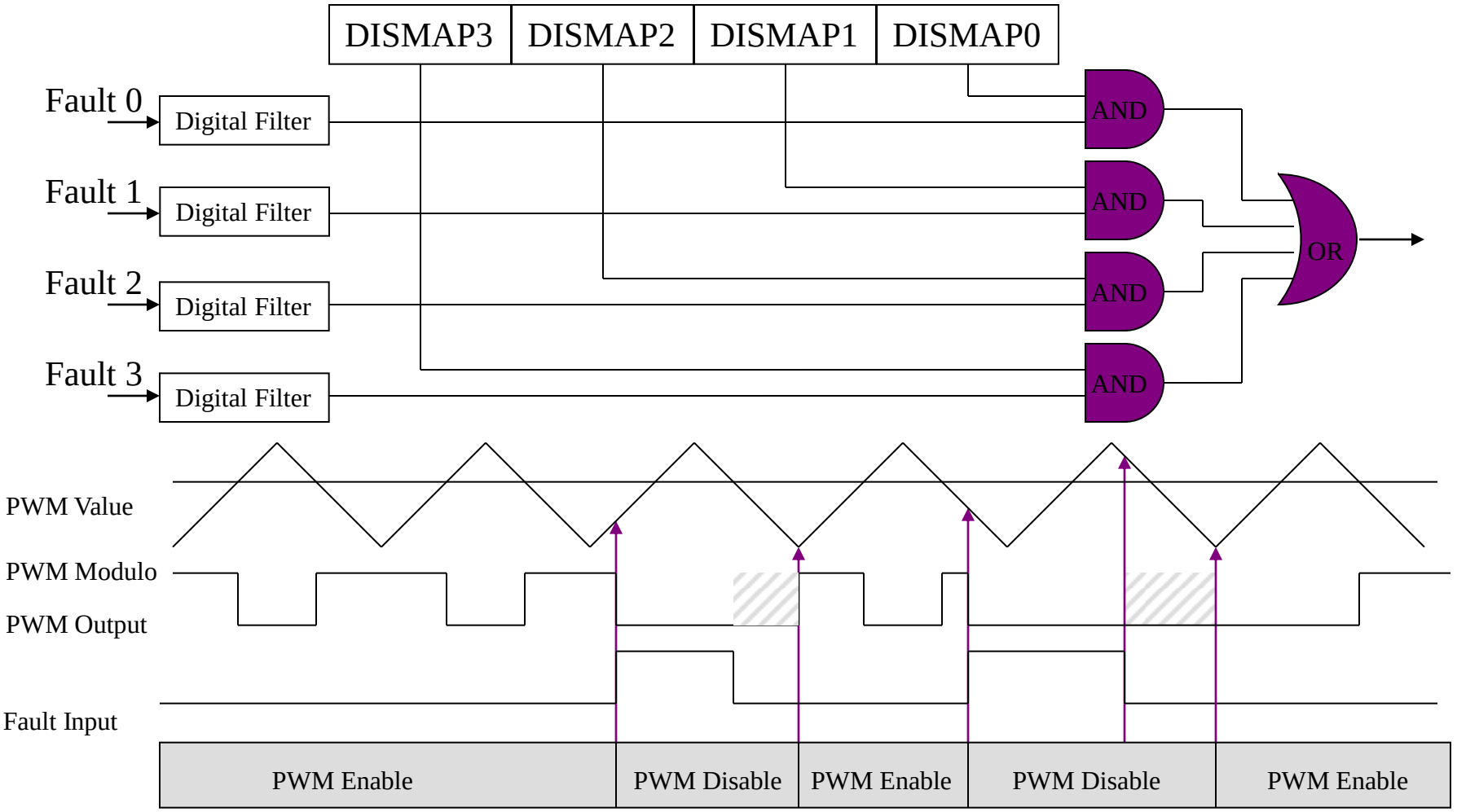
- ✓ **FAULT Pins Mapping**
  - ✓ The fault decoder disables PWM pins pre-selected by the disable mapping register.
    Each FAULT pin can be mapped arbitrarily to any of the PWM pins.
  - ✓ Each bank of four bits in the disable mapping register control the mapping for a single PWM pin.

PWM Pin to be disabled	Fault0	Fault1	Fault2	Fault3	PWM Disable Mapping Register
	to assign Fault and PWM pin set **DISMAP bit #**				
PWM0	0	1	2	3	PMDISMAP1 [0:3]
PWM1	4	5	6	7	PMDISMAP1 [4:7]
PWM2	8	9	10	11	PMDISMAP1 [8:11]
PWM3	12	13	14	15	PMDISMAP1 [12:15]
PWM4	16	17	18	19	PMDISMAP2 [0:3]
PWM5	20	21	22	23	PMDISMAP2 [4:7]

Example

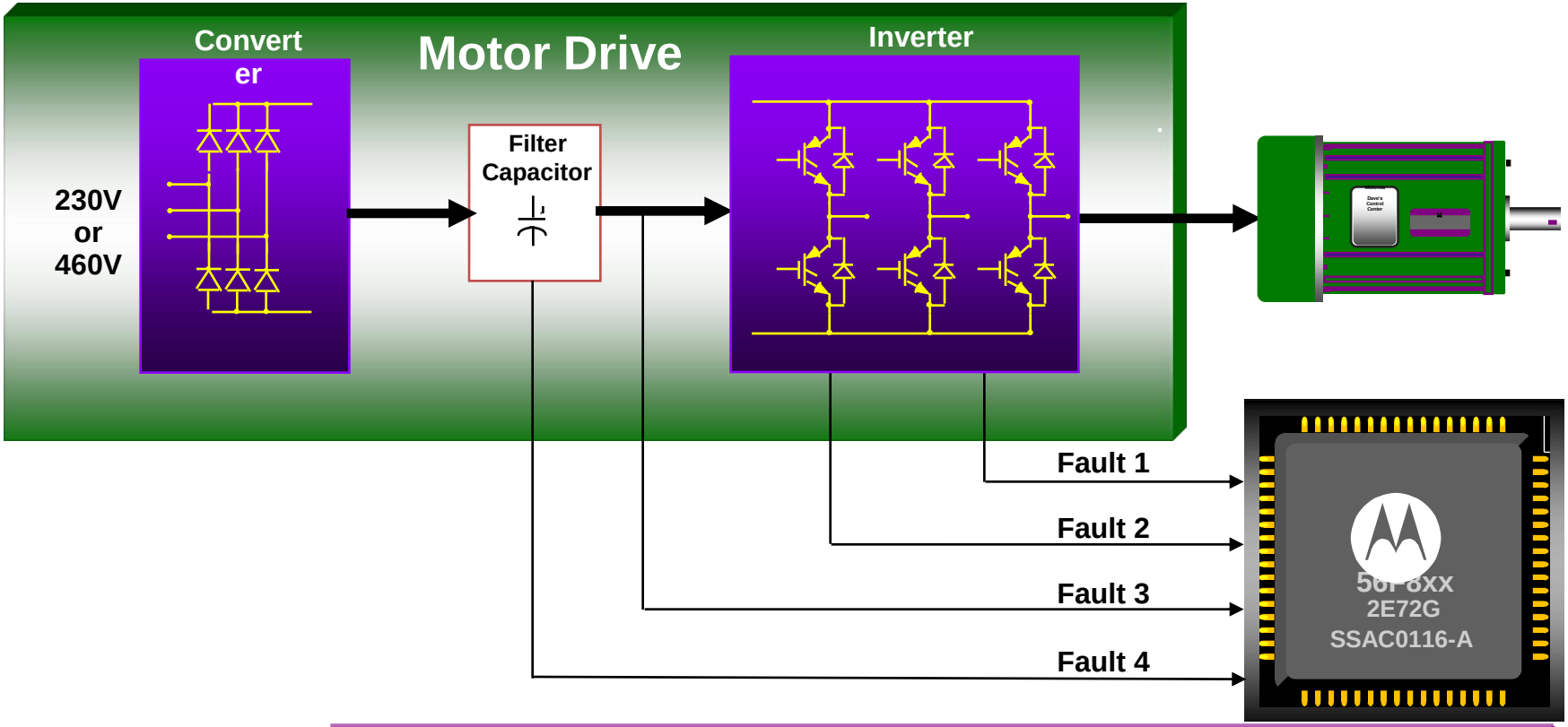
Fault Pins vs. PWM Pins Mapping

PWM Fault Decode And Automatic Clearing



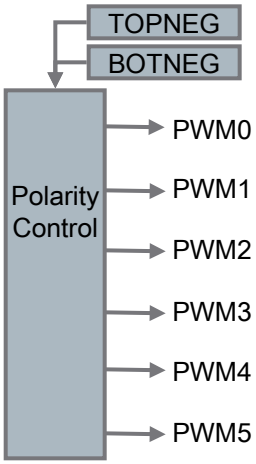
*When Fault logic returns to logic 0, the PWM restart at beginning of the next half cycle.

Multiple Fault Inputs

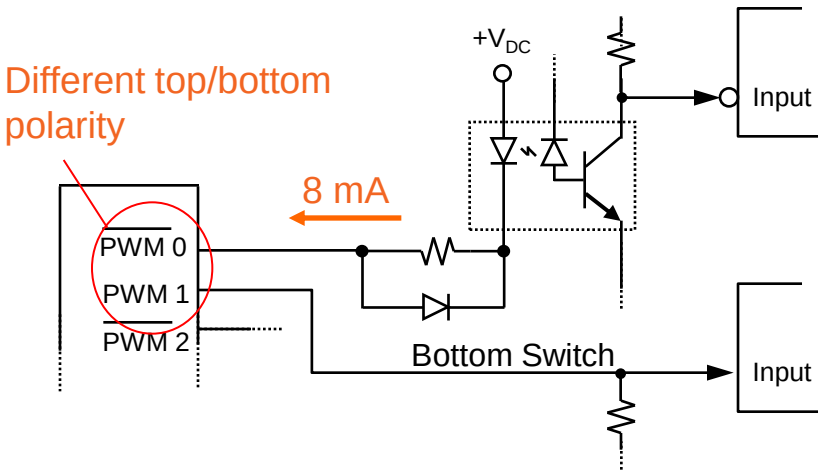


- ✓ Fault inputs can independently monitor critical system parameters, and generate an interrupt when asserted.
- ✓ Each input is mapable to immediately disable any or all PWMs
- ✓ Each input is programmable to allow Automatic or Manual PWM restart.

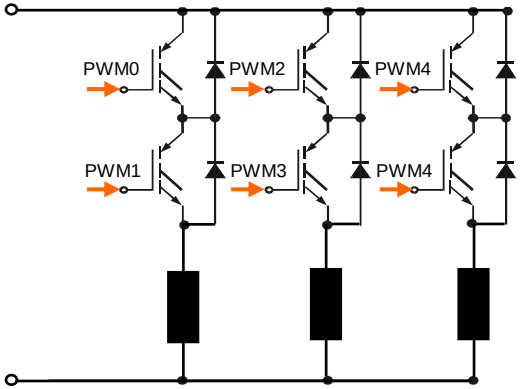
Pulse Width Modulator - Polarity Control



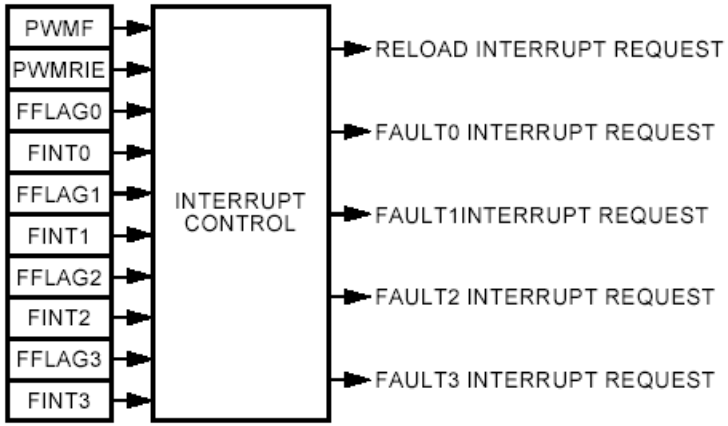
- **Polarity Control**
  - ***Positive polarity** means when the PWM is active - its output is high.*
  - ***Negative polarity** means when the PWM is active - its output is low.*
  - ***Separate control of top and bottom PWM outputs.***
    ***TOPNEG** - controls PWM0/2/4 polarity.*
    ***BOTNEG** - controls PWM1/3/5 polarity.*
- **High Current Capability**
- **8 mA current sink / current source capability**



Direct PWM pin-optocoupler connection



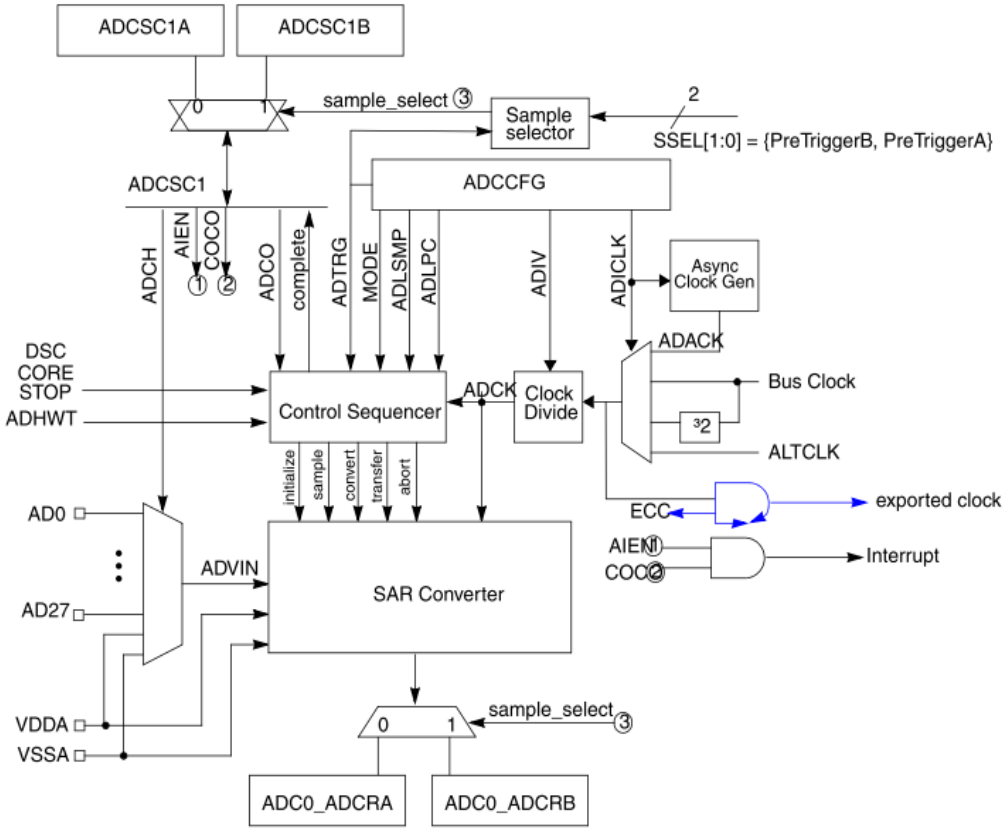
PWM - Interrupt Control



- **The PWM module can generate up to 5 interrupt requests.**
- **Reload flag (PWMF)** - PWMF is set at the beginning of every reload cycle.
  The reload interrupt enable bit (PWMRIE) enables PWMF to generate CPU interrupt requests.
- **Fault flags (FFLAG0–FFLAG3)** - The FFLAGx bit is set when fault pin filters recognises a logic 1 on the FAULTx pin.
  The fault pin interrupt enable bits (FIE0–FIE3) enable the FFLAGx flags to generate CPU interrupt requests.

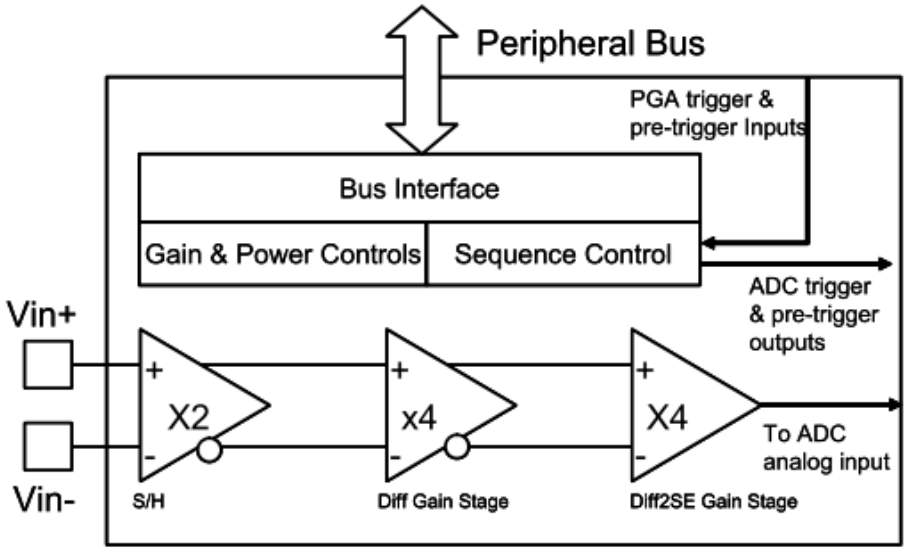
A/D Converter

- Two ADC modules allowing parallel conversion
- Input voltage range from VSSA to VDDA
- Up to 28 analog inputs
- Output in 12-, 10- or 8-bit right-justified format
- Single or continuous conversion (automatic return to idle after single conversion)
- 2.5 μs conversion time
- Configurable sample time and conversion speed/power
- Conversion complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in wait or stop modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Hardware and software triggering
- Temperature sensors that are routed to ANA26 and ANB26
- Support up to four samples per conversion



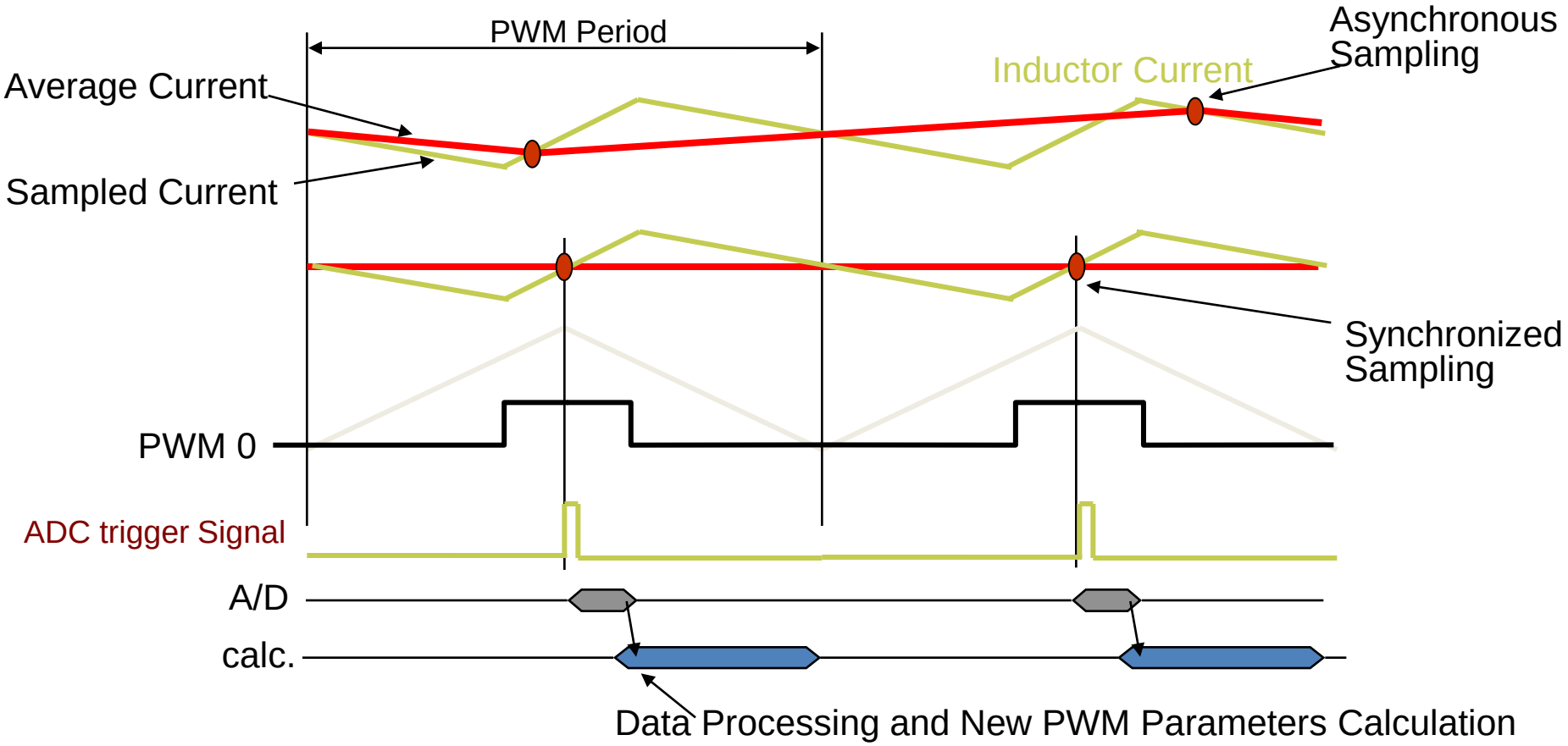
Programmable Gain Amplifier (PGA)

- Sampled PGA architecture
- Common mode noise and offset cancelation
- Synchronized with PWM operation
- 0.14 MSPS maximum
- Sampling time can be precisely controlled (to less than 0.1 µs)
- Programmable gains (1×, 2×, 4×, 8×, 16×, and 32×)
- Selectable tradeoff for slower/low power versus faster/more power
- Rail-to-rail input voltage range
- Single-ended output routed directly to on-chip ADCs ANA15 and ANB15
- Software and hardware triggers are available
- Includes additional calibration features:
  - Offset calibration eliminates any errors in the internal reference used to generate the VDDA/2 output center point
  - Gain calibration can be used to verify the gain of the overall datapath
  - Both features require software correction of the ADC result



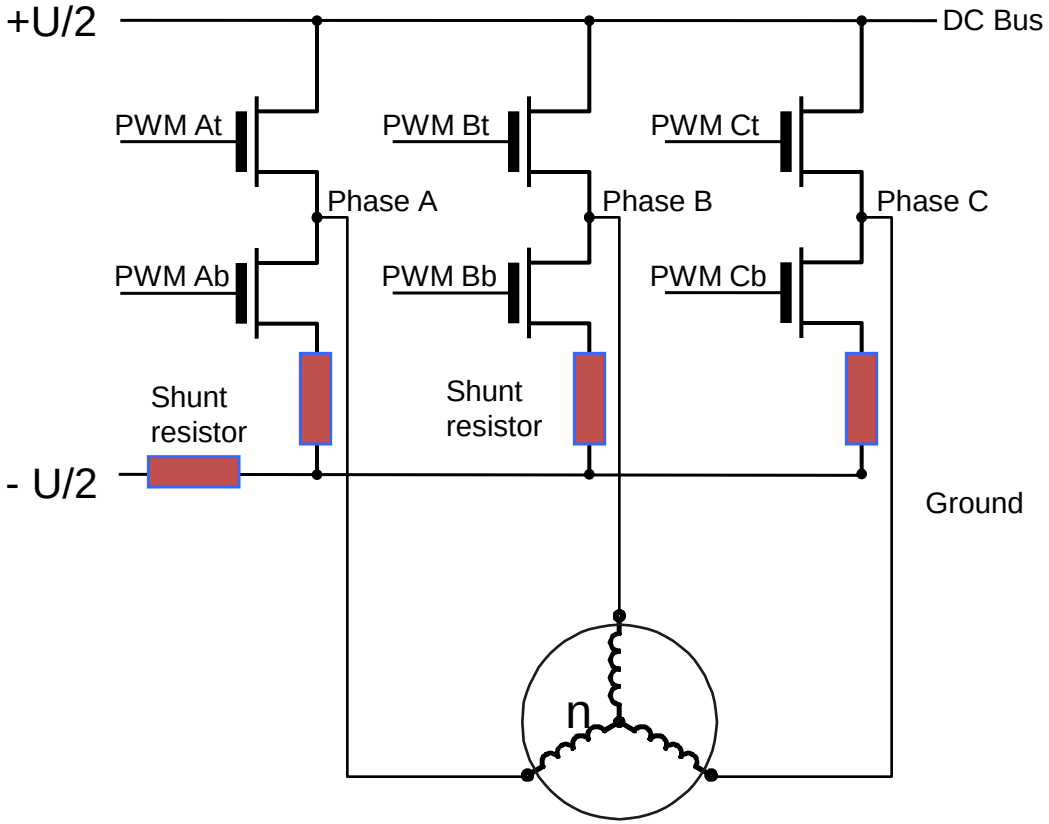
Why Is ADC to PWM Synchronization Needed?

- ADC sampling helps to filter the measured current - antialiasing

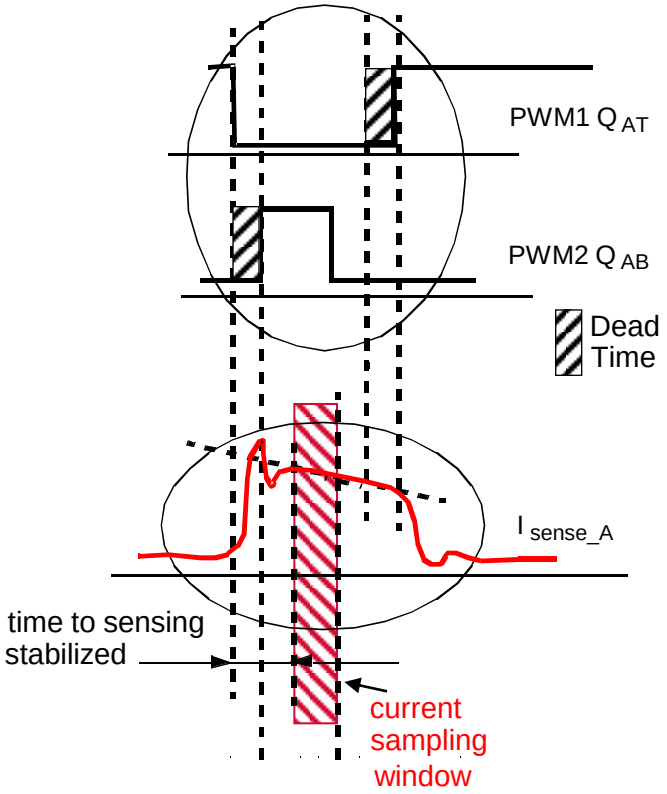


Why Is ADC to PWM Synchronization Needed?

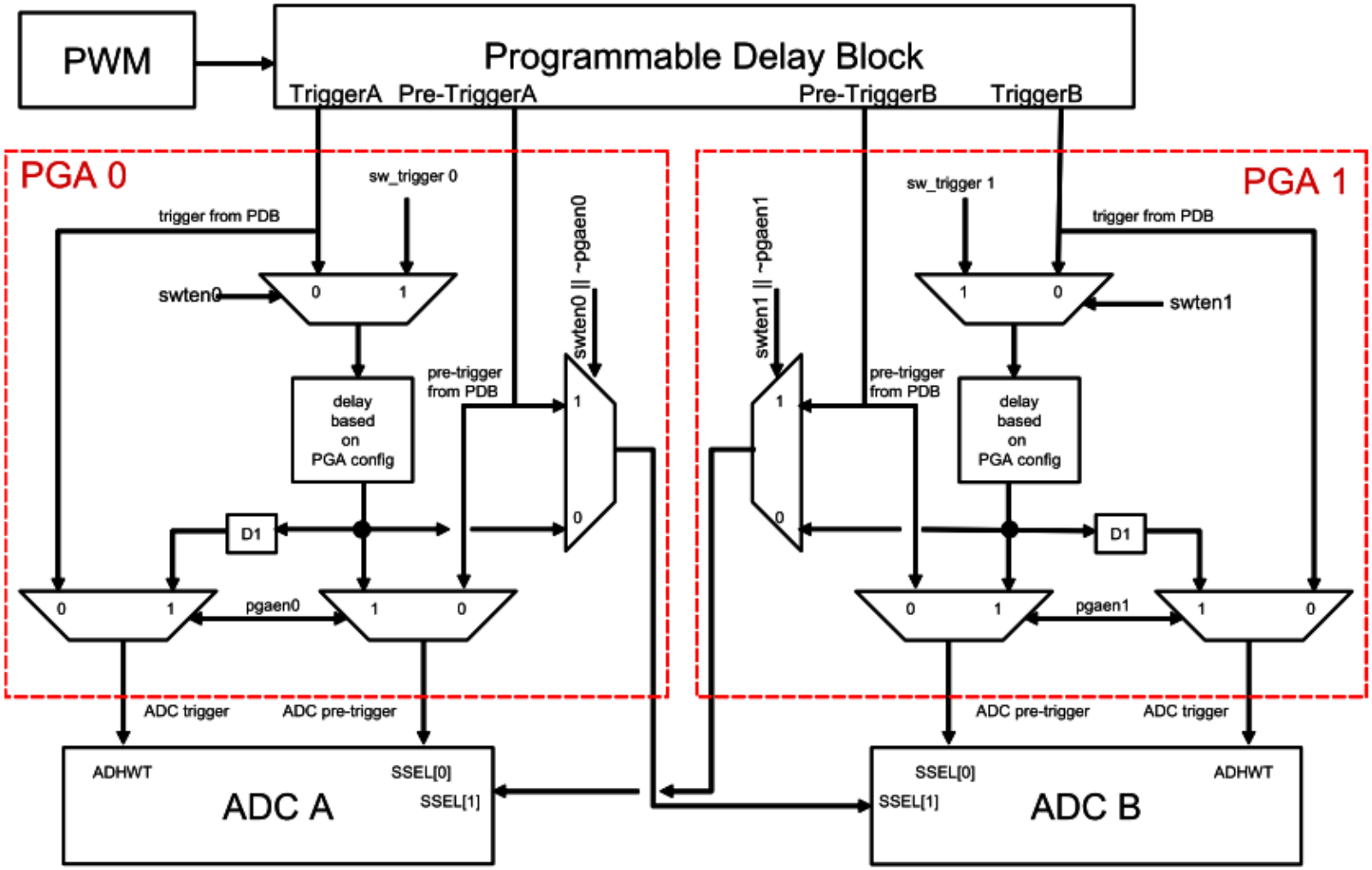
- Phase current can be sensed for certain time only



3-ph AC Induction Motor
3-ph PM Synchronous Motor

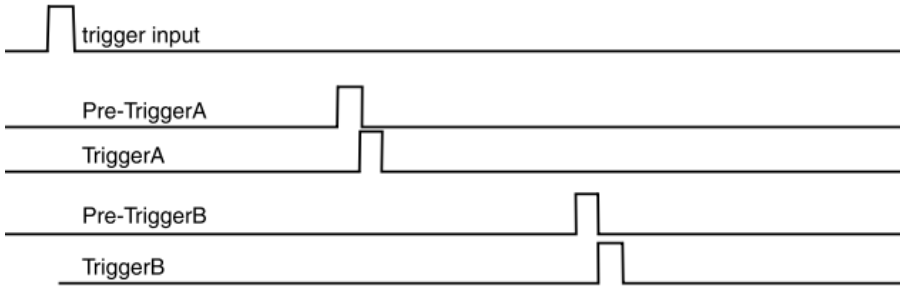


ADC to PWM Synchronization: MC56F800x

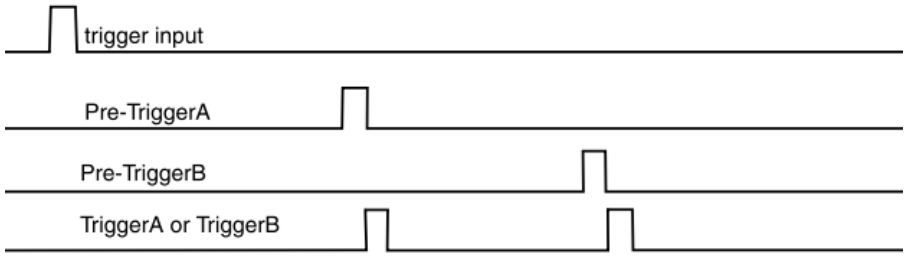


Programmable Delay Block Operation Modes

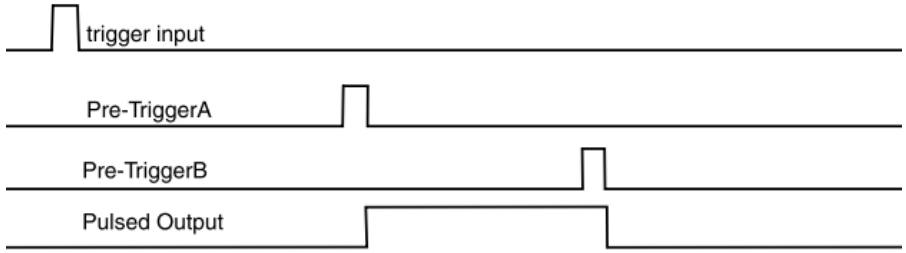
- Individual Operation
  - Each ADC is controlled individually



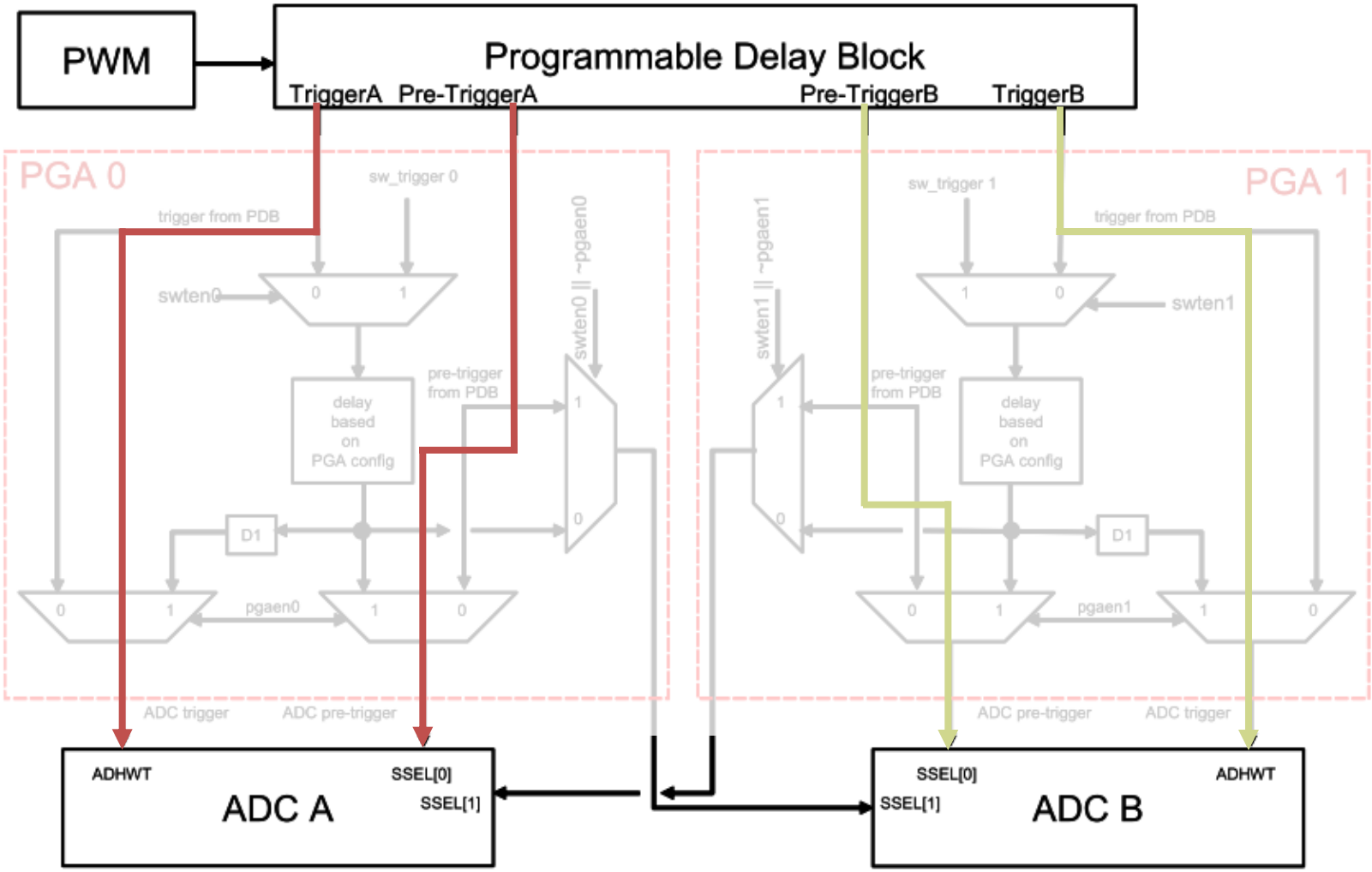
- ORed Operation
  - Both ADC converters operate in ping – pong mode. Up to four samples can be taken per conversion sequence



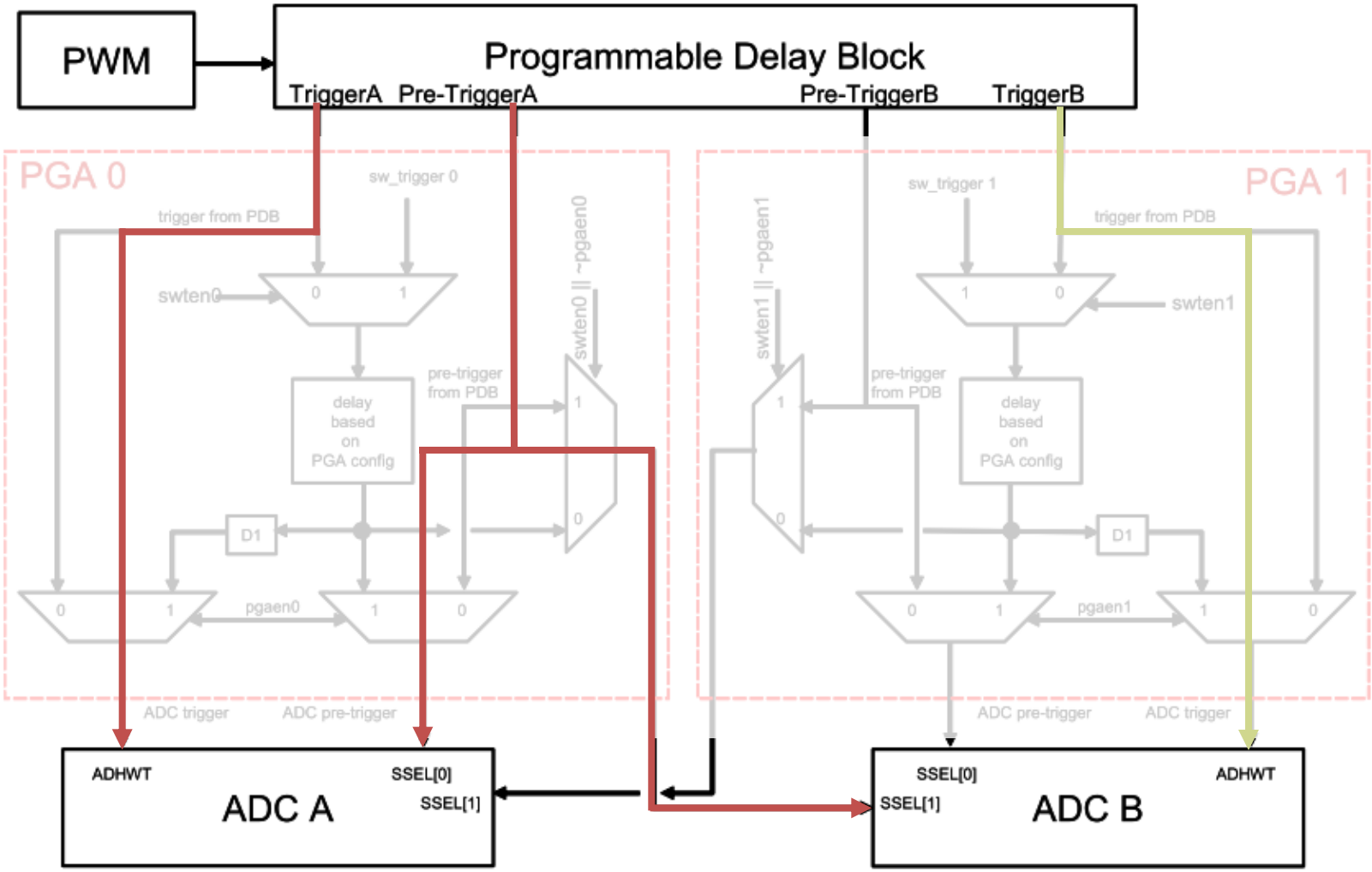
- Pulsed (PWM) Operation
  - This mode can be used for window operation of high speed comparator
  - The output can be connected to pin and generated PWM signal



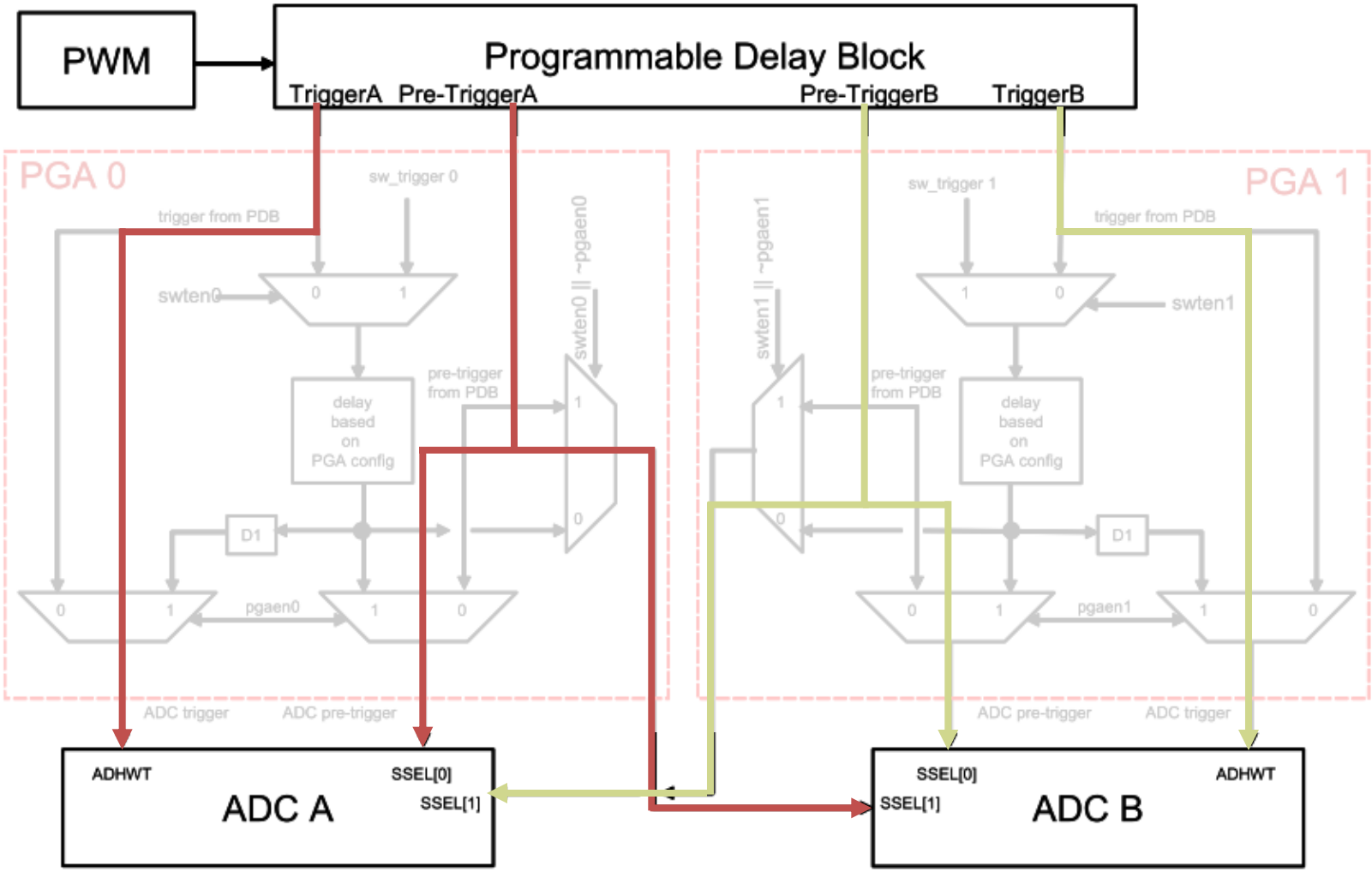
ADC to PWM Synchronization: (Individual Mode)



ADC to PWM Synchronization: (ORed Mode)



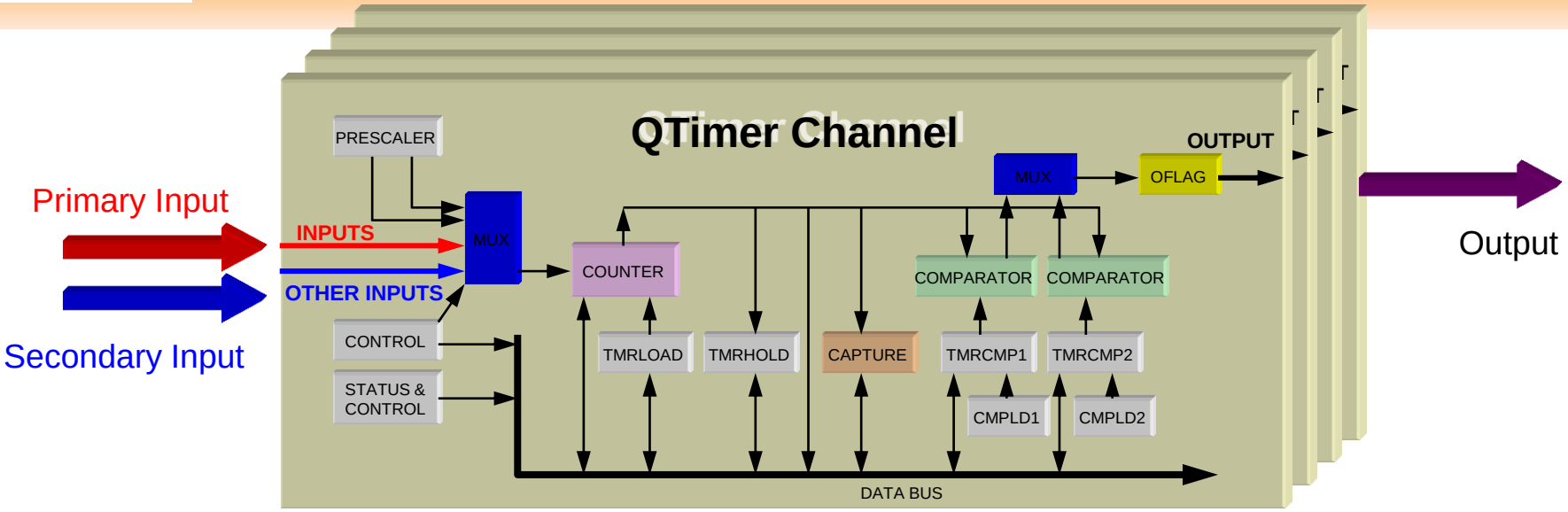
ADC to PWM Synchronization: (ORed Mode)



Quad Timer Module

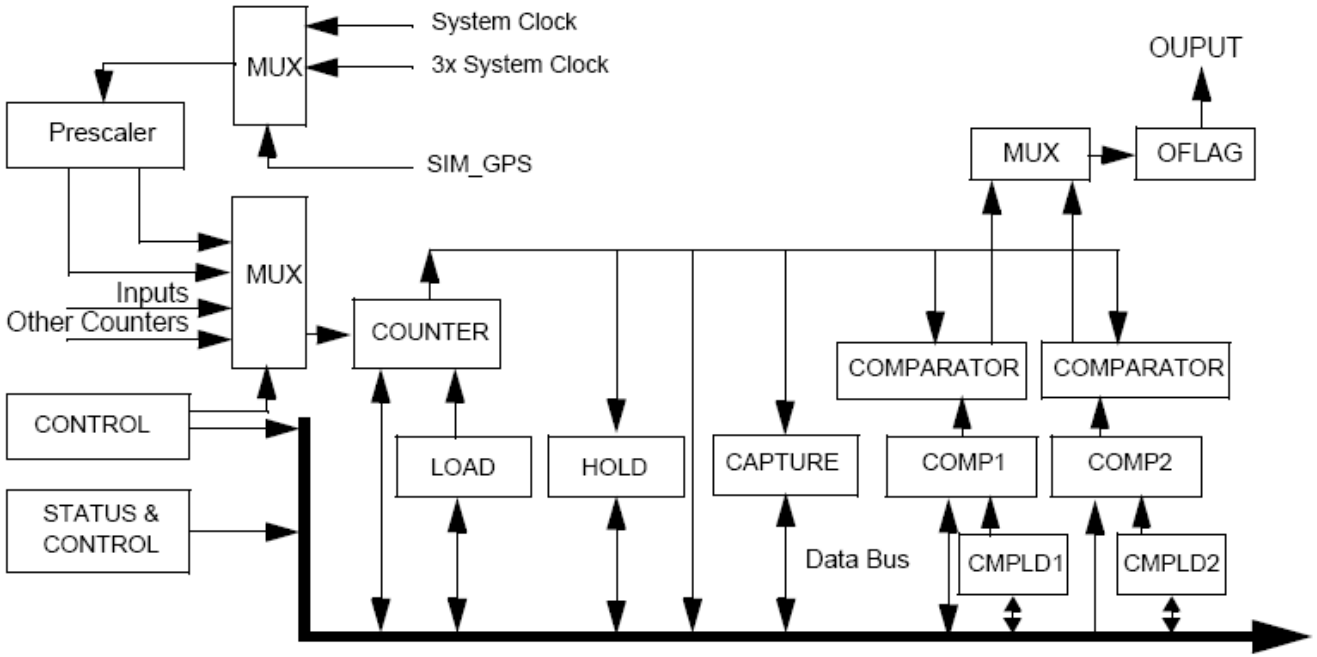
- **4x 16-bit general purpose up/down timer/counters per module**
- **Up to 96 MHz operation**
- **Individual channel capability**
  - Input capture trigger
  - Output compare
  - Clock source
  - Prescaler
- **Max. count rate**
  - external events counting - peripheral clock/2
  - internal clock counting - peripheral clock
- **Counters are pre-loadable**
- **Count once or repeatedly**
- **Programmable count modulo**
- **Input pins are fully shareable within timer module**
- **Pins available as general I/O when timer(s) not in use**
- **Counters in module can be daisy-chained to yield longer counter lengths**
- **Master operation**
  - “Broadcasts” compare function
  - channel re-initialization for coherent operation
- **Up to 12 operation Modes**

Quad Timer Module



- **Unique architecture with -** 2x Inputs (Primary + Secondary) and 1x Output
- **Powerful MUX -** Primary Input, Secondary Input and Output can be connected to ext. pins
- **Individual channel capability -** Input capture trigger, Output compare, Clock source, Prescaler
- **Counters are pre-loadable, Count once or repeatedly**
- **Master Operation** - any channel can be a master that broadcasts its compare signal to the other channels. Such way they can be configured to reinitialize their counters and/or force their OFLAG output signals to predetermined values.
- **Compare** - The TMRCMP1/2 registers provide the compare values (up/down) for the counter. If a match occurs, the OFLAG signal can be set, cleared, or toggled (polarity is selectable). If enabled, an interrupt is generated, and the new compare value is loaded into TMRCMP1 or 2 registers from TMRCMPLD1 and 2 (as enabled).
- **Capture** register stores a copy of the counter's value when an input edge (positive, negative, or both) is detected. Once a capture event occurs, no further updating of the Capture register will occur until the Input Edge Flag is cleared.

Quad Timer Module



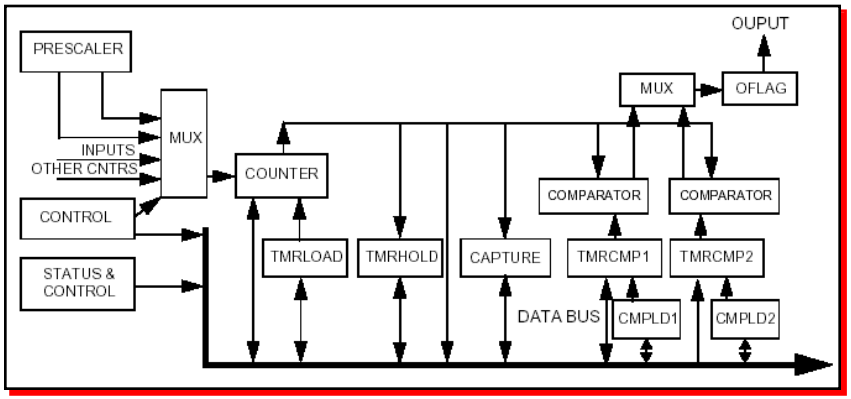
- Maximum count rate equals System Clock, or 3x System Clock for internal clocks
- Maximum count rate equals System Clock/2 for external clocks

Quad Timer Operating Modes

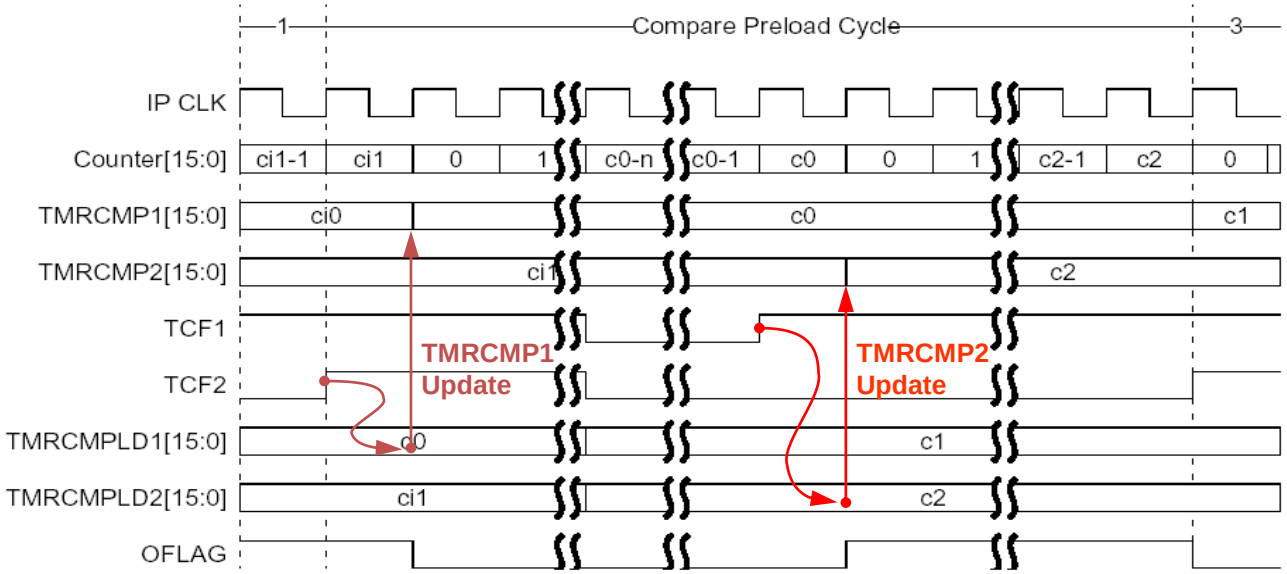
- **Stop Mode** - the counter is inert. No counting will occur, but interrupts are still possible according to input transitions on the selected input pin
- **Count Mode** - counts on rising edges (generating periodic interrupts, timing purposes)
- **Edge-Counting** - count edges (counting of simple encoder wheel)
- **Gated-Counting** - counts primary input signal if signal on secondary input is high (signal width measurement)
- **Quadrature-Counting** - counter will decode the primary and secondary external inputs as quadrature encoded signals (movement monitoring)
- **Signed-Counting** - counter increments/decrements primary clock source accordingly to level of signal asserted on secondary source
- **Triggered-Counting** - counts primary clock source if rising edge of the secondary input detected and stops counting if either rising edge or compare event occurs
- **One-Shot Mode** - provides timing delays (ADC acquisition of new samples until a specified period of time has passed since the PWM sync signal)
- **Cascade-Count Mode** - the counter's input is connected to the output of another selected counter. If any counter is read the values of other counters are captured in hold registers
- **Pulse-Output Mode** - supports stepper motor systems and provides change of signal frequency and number of pulses
- **Fixed- Freq. PWM** - fixed frequency variable duty cycle generation (driving PWM amplifiers)
- **Variable-Freq. PWM** - variable frequency and duty cycle generation (driving PWM amplifiers)

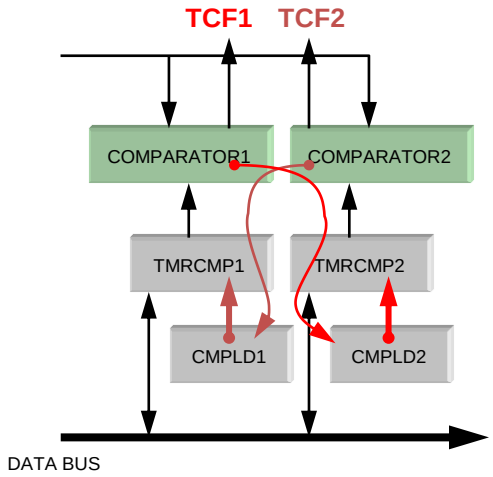
Quad Timer - Setting Modes

- **The operating modes are mainly combination of**
  - **Count Mode**
    000 = No operation
    001 = Count rising edges of primary source
    010 = Count rising and falling edges of primary source
    011 = Count rising edges of primary source while secondary input high active
    100 = Quadrature count mode, uses primary and secondary sources
    101 = Count primary source rising edges, secondary source specifies direction
    110 = Edge of secondary source triggers primary count until compare
    111 = Cascaded counter mode (up/down)
  - **Count Once setting**
    0 = Count repeatedly
    1 = Count till compare and then stop
  - **Count Length**
    0 = Roll-over
    1 = Count till compare, then re-initialized
  - **Output Mode**
    000 = Asserted while counter is active
    001 = Clear OFLAG output on successful compare
    010 = Set OFLAG output on successful compare
    011 = Toggle OFLAG output on successful compare
    100 = Toggle OFLAG output using alternating compare registers1
    101 = Set on compare, cleared on secondary source input edge
    110 = Set on compare, cleared on counter rollover
    111 = Enable Gated Clock output while counter is active



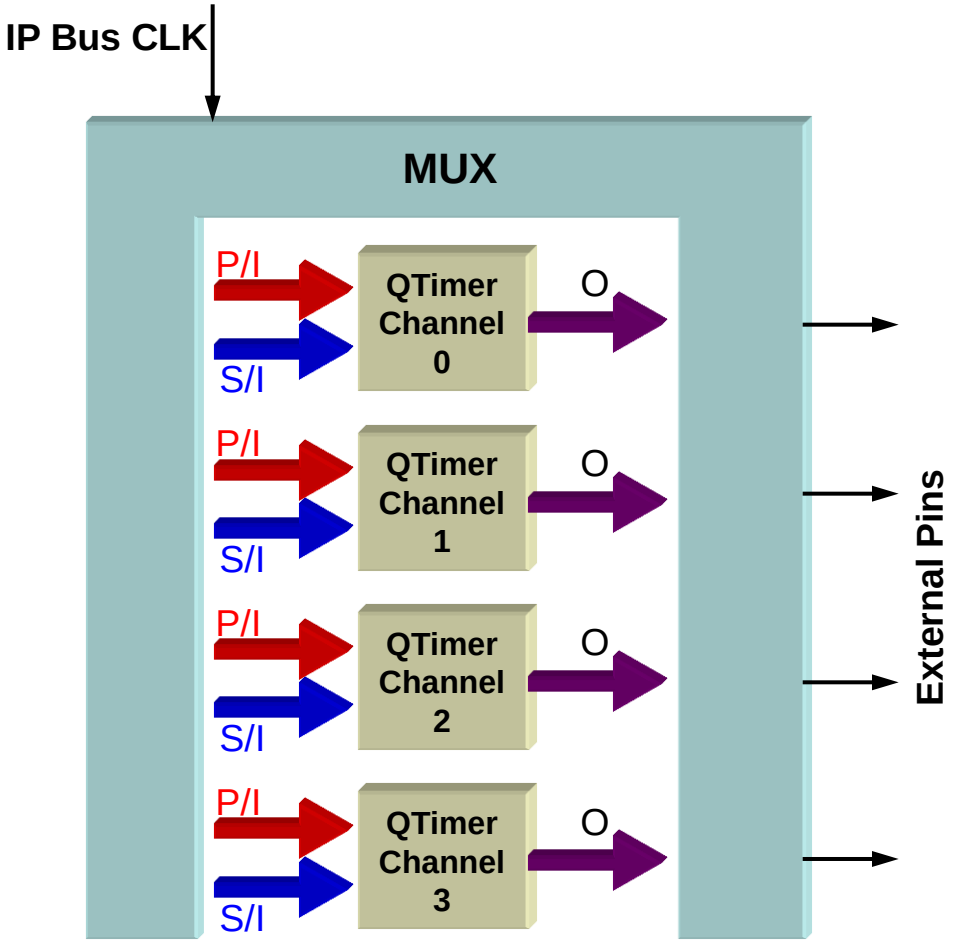
Quad Timer - Compare Pre-load - 2 Options





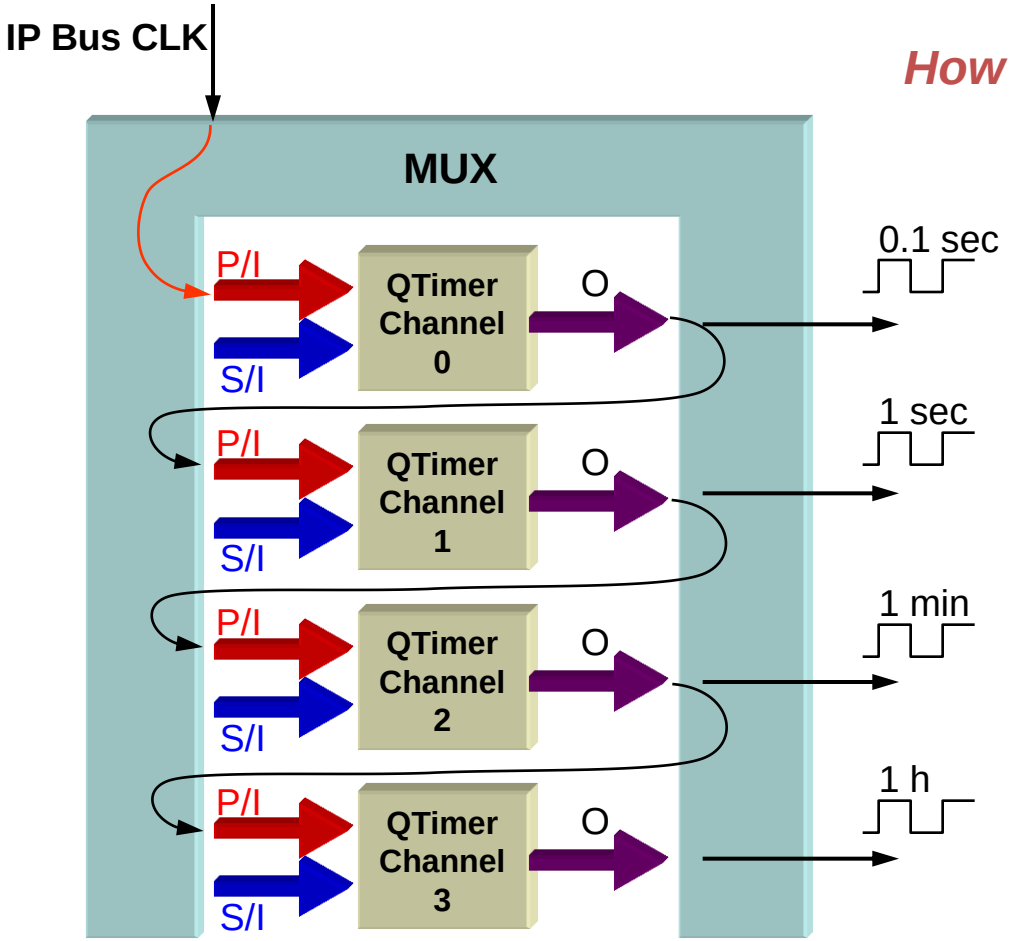
- The Compare Pre-load cycle begins with a compare event on TMRCMP2, causing TCF2 to be asserted.
- TMRCMP1 is loaded with the value in the TMRCMPLD1 one IPBus clock later.
- Additionally, an interrupt is asserted by the timer and the interrupt service routine is executed. During this time both Comparator Load registers are updated with new values.
- When TCF1 is asserted, TMRCMP2 is loaded with the value in TMRCMPLD2.
- On the subsequent TCF2 event, TMRCMP1 is loaded with the value in TMRCMPLD1.
- The cycle starts over again as an interrupt is asserted and the interrupt service routine clears TCF1 and TCF2, calculating new values for TMRCMPLD1 and TMRCMPLD2

Quad Timer Module - SW Model



- ✓ **Unique architecture with**
  - ✓ Primary input
  - ✓ Secondary input
  - ✓ Output
- ✓ **Powerful MUX**
  - ✓ Primary Input, Secondary Input and Output can be connected to ext. pins
- ✓ **Channels can be daisy-chained**
  - ✓ Output → Primary input - yields longer counter lengths
  - ✓ Output → Secondary input - time window counting of ext. event
- ✓ **Master Operation**
  - ✓ any channel can be a master that broadcasts its compare signal to the other channels.
  - ✓ Such way timer channels can be configured to reinitialize their counters and/or force their output signals to predetermined values.

Quad Timer Module - Advanced Operation #1

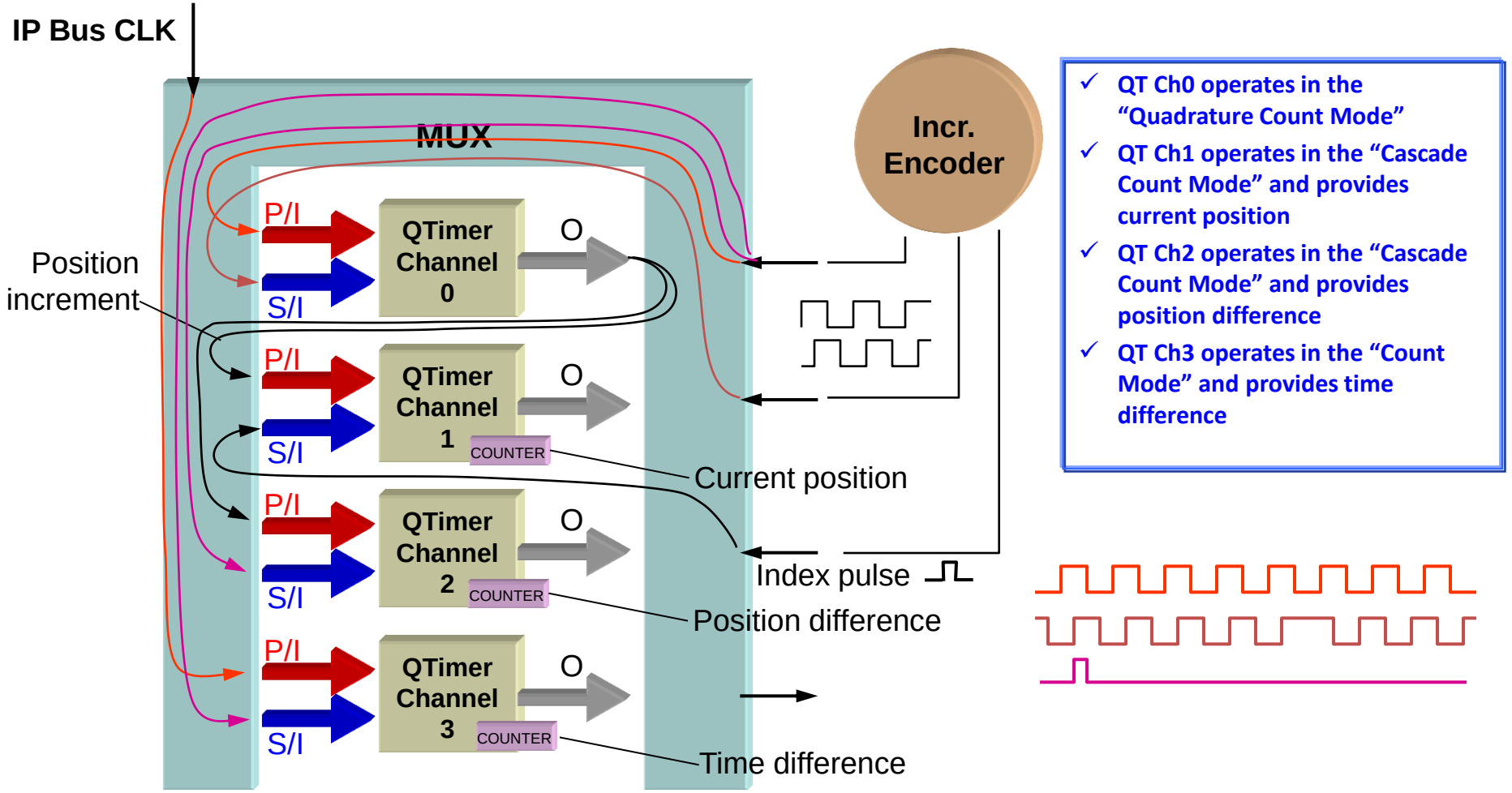


How to toggle - pin0 each 0.1 sec ?
- pin1 each 1 sec ?
- pin2 each 1 min ?
- pin3 each 1 h ?

- ✓ QT Ch0 operates in the “Count Mode”
- ✓ QT Ch1, Ch2 and Ch3 operate in the “Edge Count Mode”
- ✓ QT Ch0 compare is set to reflect 0.1 sec and to toggle the OFLAG
- ✓ QT Ch1 compare is set to reflect 1 sec and to toggle the OFLAG
- ✓ QT Ch2 compare is set to reflect 1 min and to toggle the OFLAG
- ✓ QT Ch3 compare is set to reflect 1 hour and to toggle the OFLAG
- ✓ Ch0, Ch1, Ch2 and Ch3 are “daisy-chained”

Quad Timer Module - Advanced Operation #2

How to measure the position and support the speed measurement ?

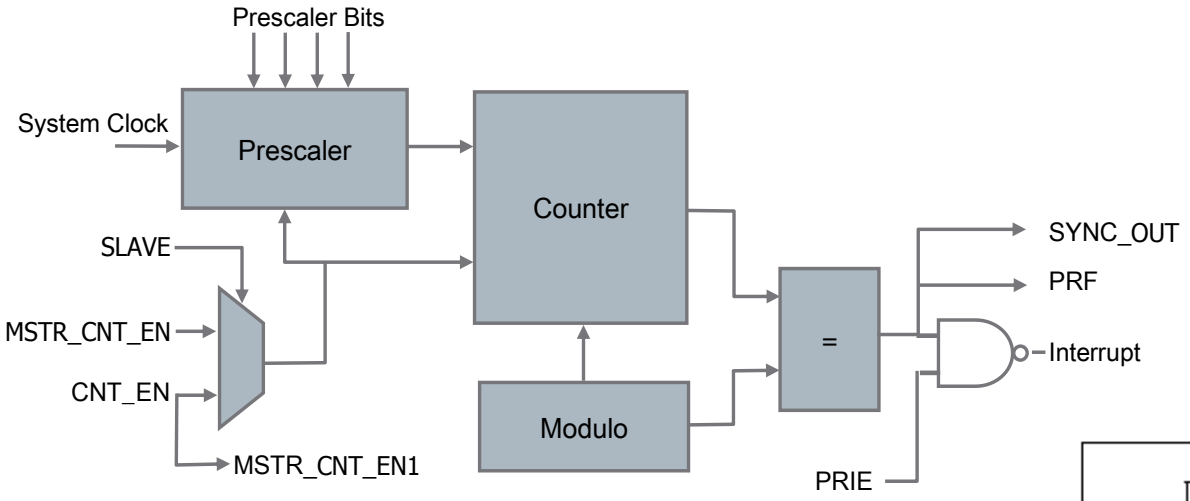


- ✓ QT Ch0 operates in the "Quadrature Count Mode"
- ✓ QT Ch1 operates in the "Cascade Count Mode" and provides current position
- ✓ QT Ch2 operates in the "Cascade Count Mode" and provides position difference
- ✓ QT Ch3 operates in the "Count Mode" and provides time difference

Programmable Interval Timer

- Three 16-bit general purpose up counter with a 4-bit prescaler
- Individually programmable time interval based on system clock source
- Counter roll-over generates interrupt request if roll-over interrupt is enabled
- Counter roll-over signal can be used as DAC conversion start signal.
- All PITs can be synchronized with PIT0
- Low Power Mode support

PIT Timer



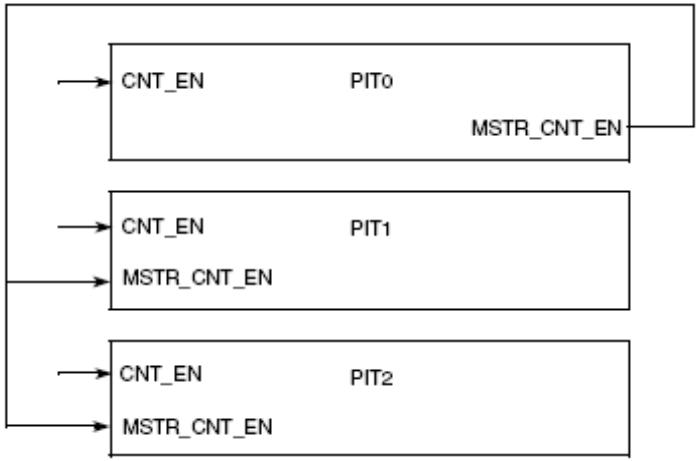


Figure 16-3. CNT_EN Connection Between Multiple PITs

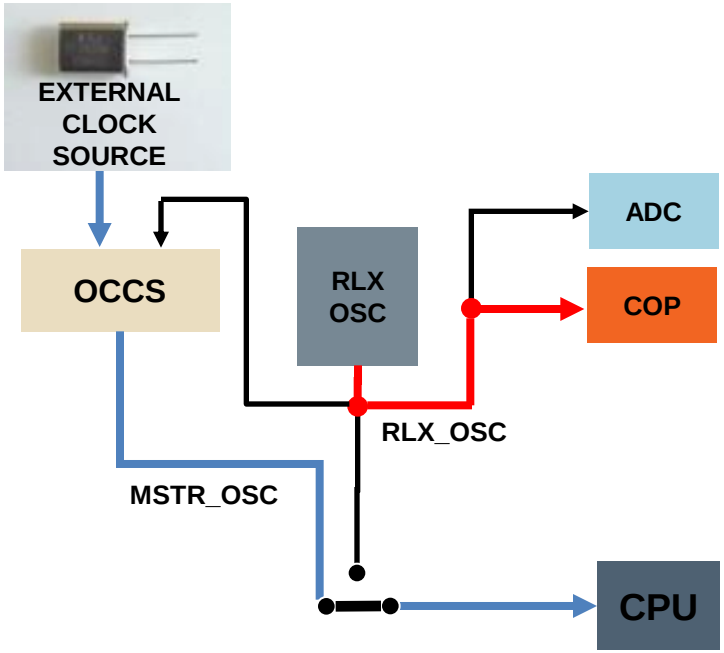
COP and Power Supervisor

- **Computer Operating Properly**
  - Free-running down counter that resets the device once the terminal count has been reached
  - Can be used as a mechanism for recovering from errant software.
  - Has an associated reset vector in the interrupt vector table
  - Allows COP Resets to be handled differently than Hardware or Software Resets.
  - Features write-protectible registers for added protection.
  - Capable of selecting different clock sources to prevent primary clock failure caused safety concerns
  - The service procedure consists of writing $5555 followed by $AAAA to the CNTR register.

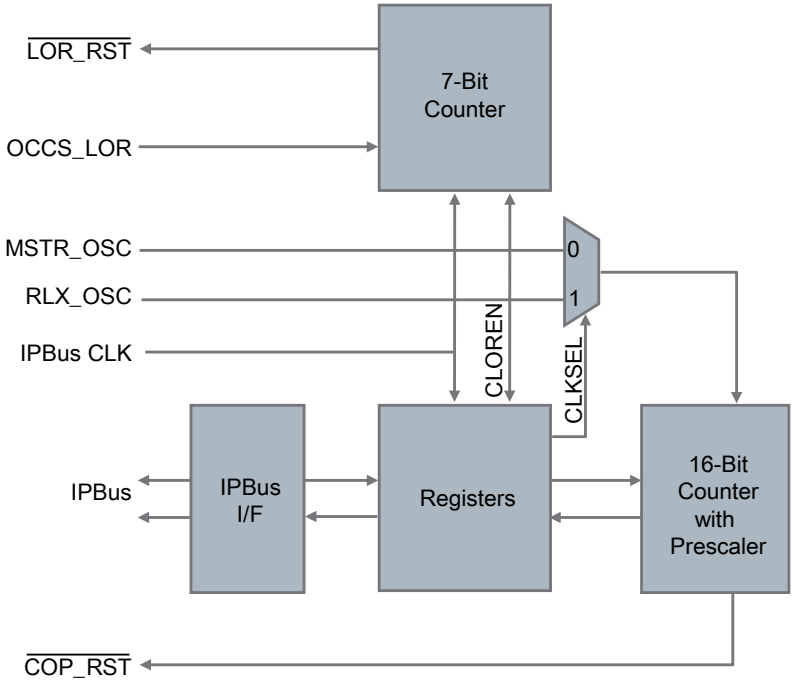
- **Power Supervisor**
  - Holds device in reset until there is enough voltage (VDD > 1.8V) for on-chip logic to operate at the oscillator frequency
    - *Precludes any problems associated with false restart*
  - Low Voltage detectors generate high-priority interrupts
    - *Two low voltage detect signals used to initiate a software controlled shutdown when the supply voltage drops below acceptable either 2.2V or 2.7V levels*
  - Eliminates need for external power monitor

COP Basics

- Independently clocked watchdog



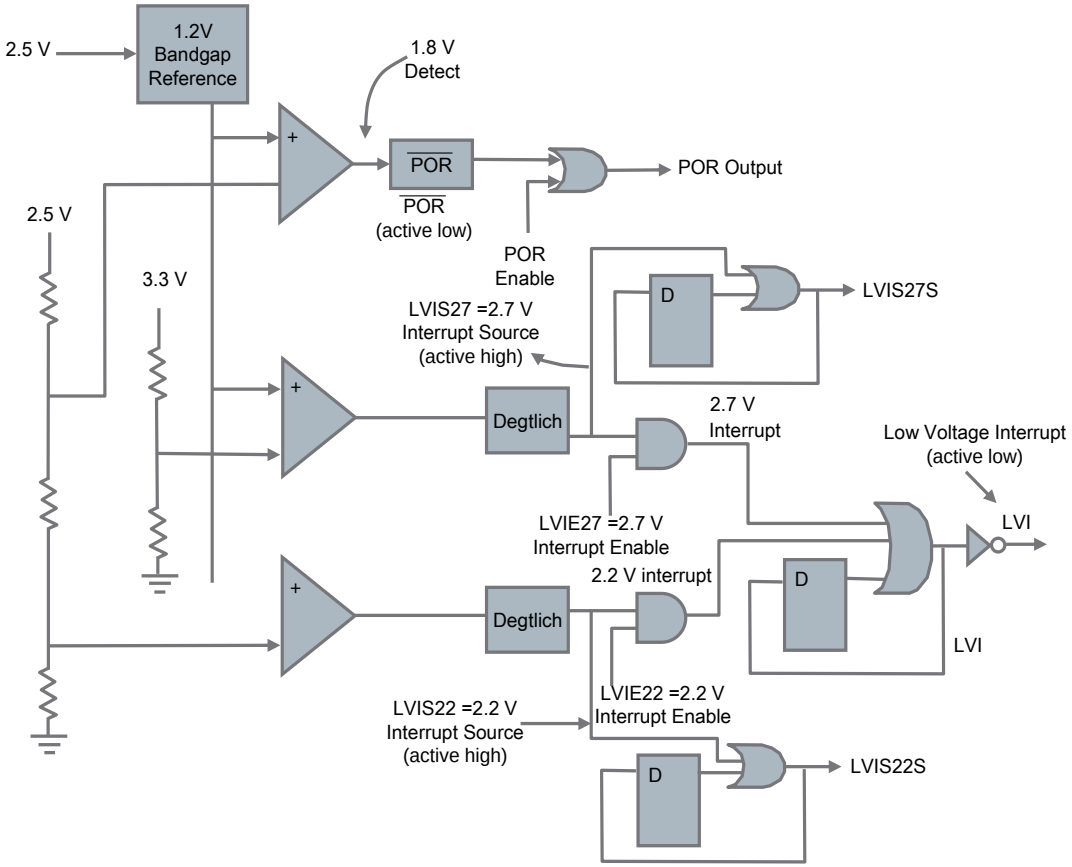
- Block diagram



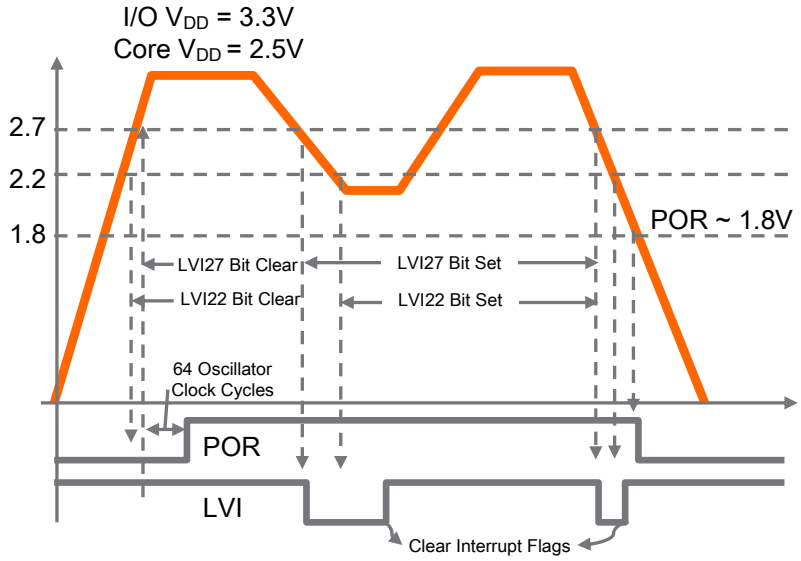
- **Option to use independent RC relaxation oscillator (RLX_OSC) for COP**
- **CPU is clocked from MSTR_CLK (External Clock Source)**
- **COP can be clocked from MSTR_CLK or RLX_OSC**
- **If OCCS selects RLX_OSC for MSTR CLK, then both COP and CPU CLKS are the same source**

Power Supervisor - Block Diagram

- Block Diagram



- Power Supervisor Operation



Thank you