



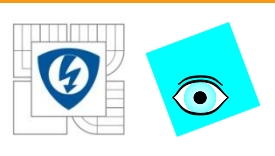
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

Spínané zdroje a jejich digitální řízení

Ing. Jaroslav Lepka
Ing. Pavel Grasblum, Ph.D.

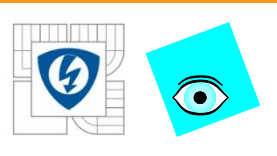
31. května – 1. června 2012

Tato prezentace je spolufinancována Evropským sociálním fondem a státním rozpočtem České republiky.



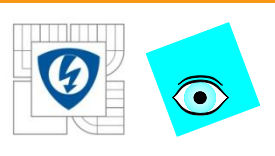
Agenda

- Linear Regulator
- Non-Isolated SMPS
- Isolated SMPS
- Resonant SMPS
- Digital Control of SMPS
- Hands on (Step down Converter)



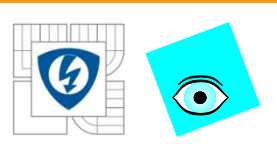
Switch Mode Power Supply Introduction

- We can distinguish SMPS according many parameters:
 - Type of source
 - Voltage Source Converters, Current source Converters
 - Type of conversion
 - DC/DC, AC/DC, AC/AC or DC/AC
 - Ratio V_{OUT}/V_{IN}
 - Step Up, Step Down or Both
 - Galvanic Isolation
 - Isolated/non-isolated
 - Type of operation
 - Linear, Pulse with modulated, Frequency Controlled (Resonant)



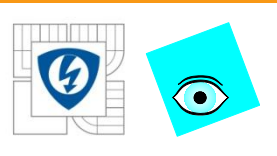
How to select right SMPS?

- When we select the power supply for our application we should consider:
 - Cost
 - Weight and space
 - Required efficiency
 - The input power source(s)
 - The number of output voltages required and their particular characteristics
 - The noise tolerance of the load circuits
 - Battery life (if the product is to be portable)



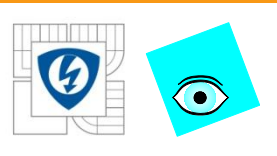
Principles of Power Supplies Operation

- Linear Regulators
- Pulse Width Modulated Switched Mode Power Supplies
- Frequency Controlled (resonant) Switched Mode Power Supplies



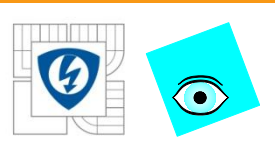
Agenda

- Linear Regulator
 - Zener shunt regulator
 - Transistor “series pass” regulator
 - How to select right linear regulator
- Non-Isolated SMPS
- Isolated SMPS
- Resonant SMPS
- Digital Control of SMPS
- Hands on



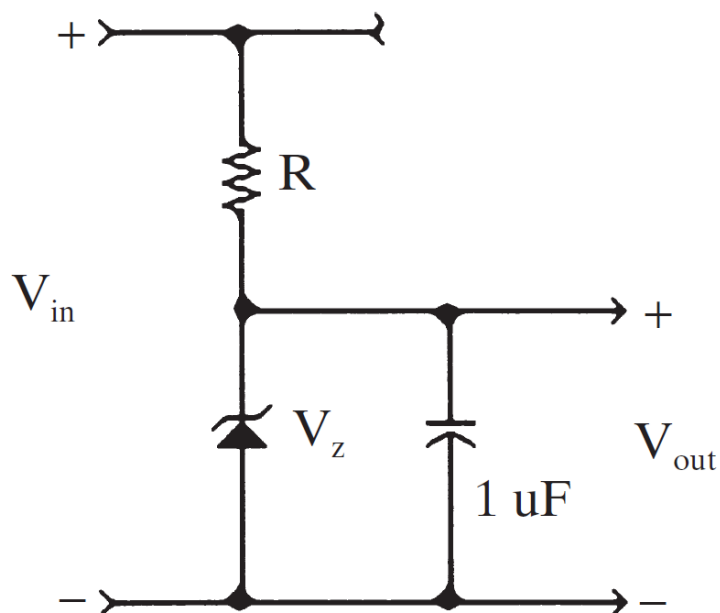
Linear Power Supply

- The control element changes the impedance to drop input voltage to desired output level
- Advantages
 - Very simple to implement
 - Low cost
 - Very low noise generation
- Disadvantages
 - Very low efficiency (35 – 50%)
 - Low output power (<10W)
 - Output voltage always lower than input
 - Cannot provide galvanic isolation



Examples of Linear Power Supply

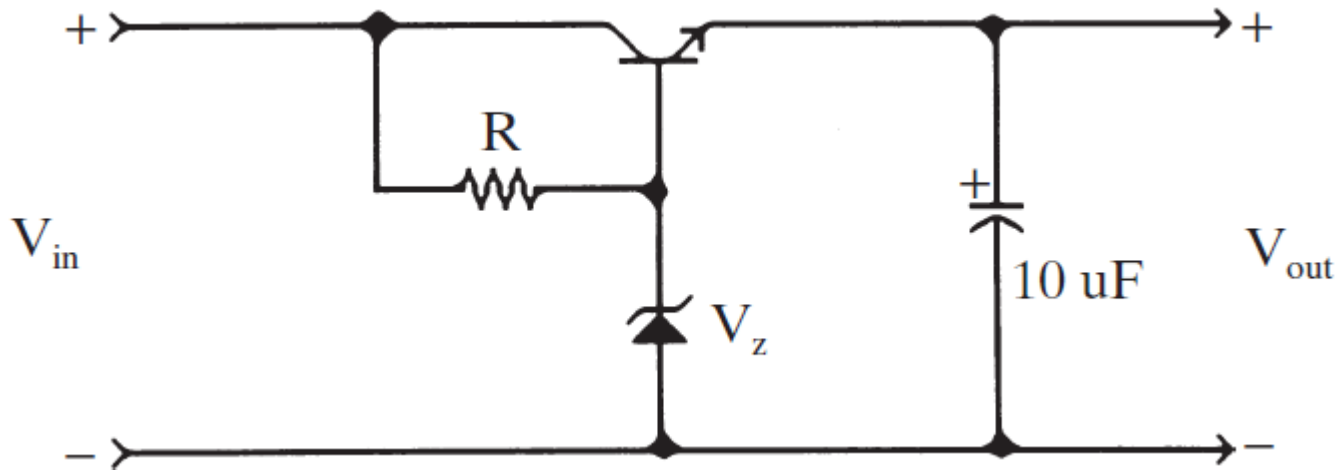
- Zener “shunt” Regulator



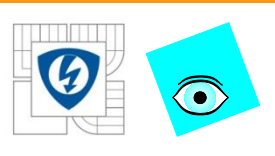
- Regulating element in parallel with load
- Very low output power
- Zener voltage changes with the temperature
- Very high losses

Examples of Linear Power Supply

- Bipolar Transistor “series-pass” Regulator

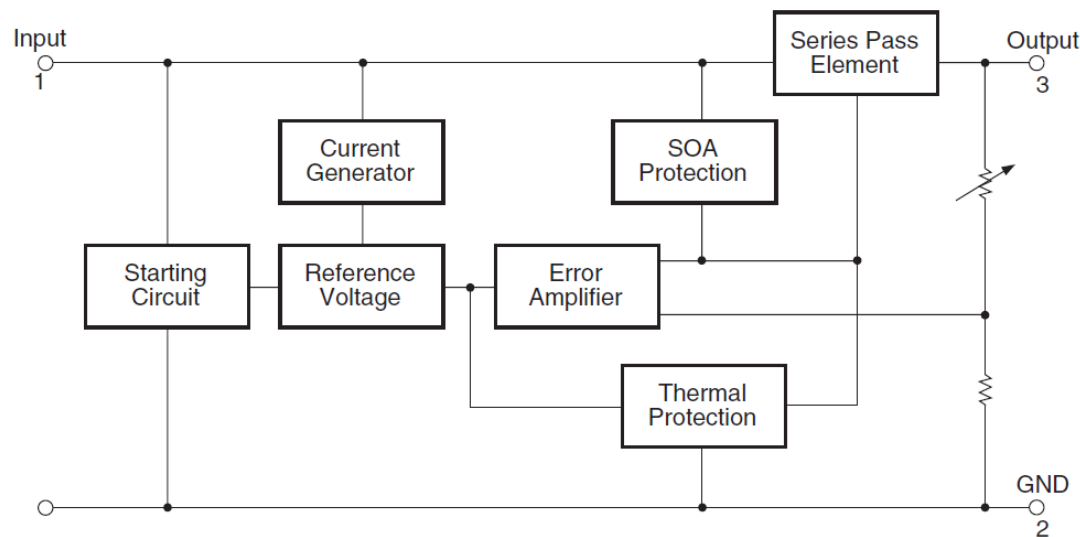


- Regulating element in series with load
- Output power depends on used transistor
- Zener voltage changes with the temperature
- Lower losses at low load

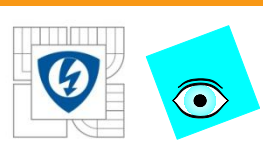


Examples of Linear Power Supply

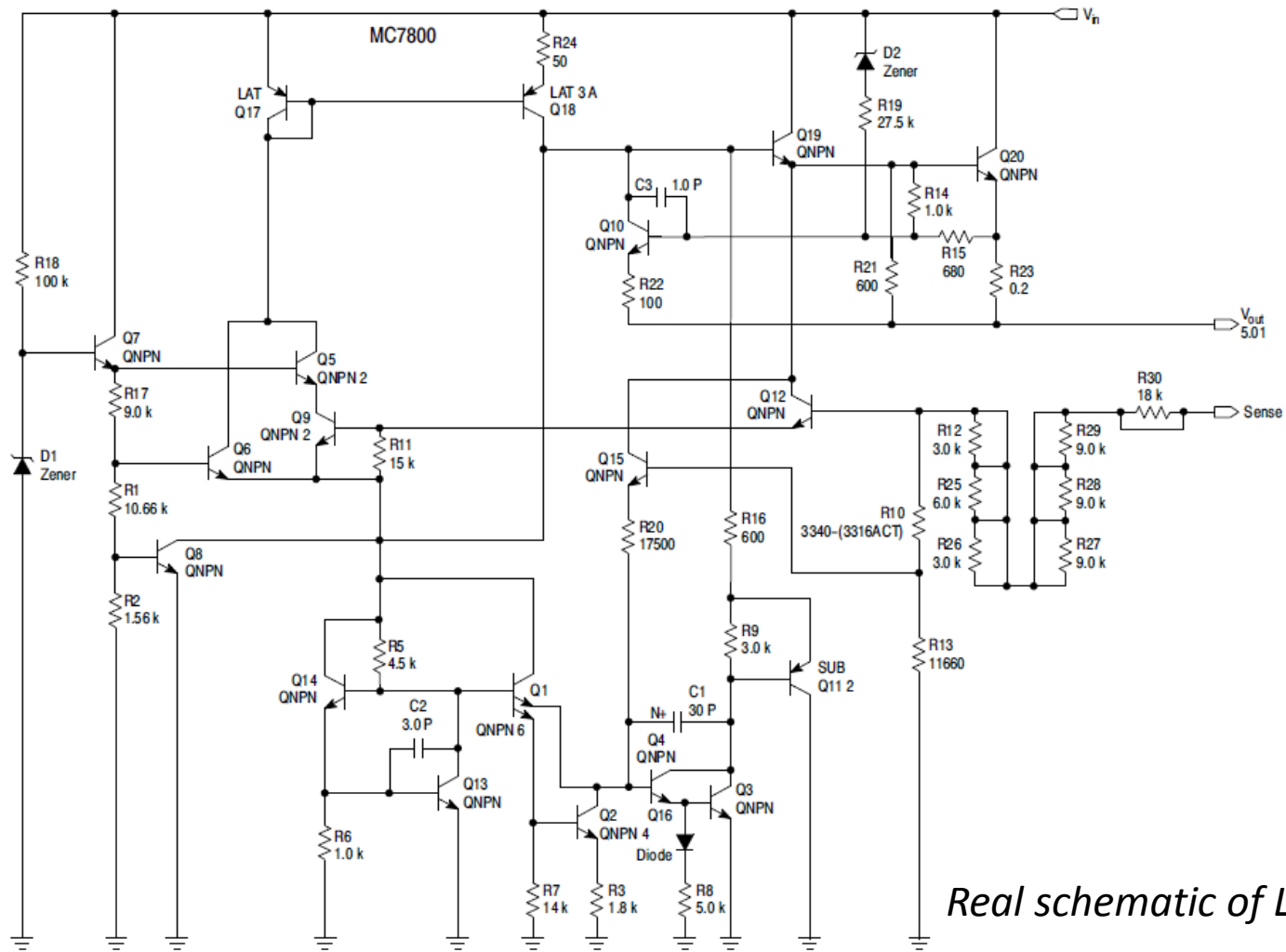
- There are plenty of integrated circuits providing linear voltage regulator
- These circuits provides more features such as current limit, thermal protection



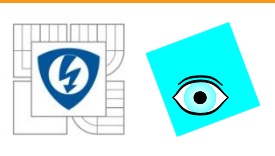
Block Diagram of LM7805



Examples of Linear Power Supply

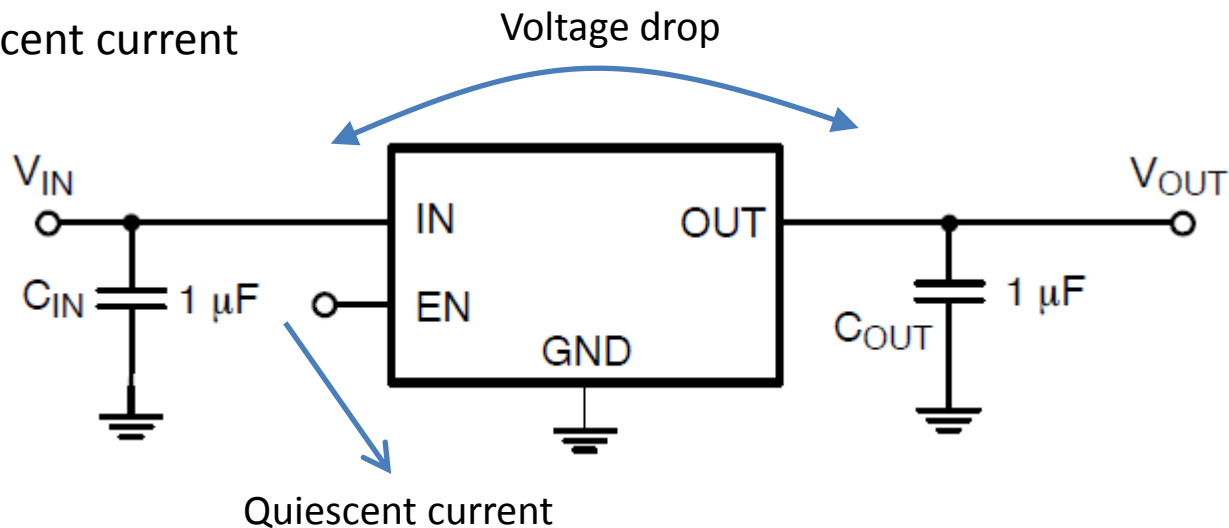


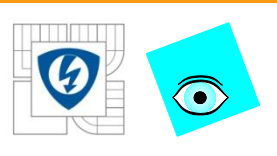
Real schematic of LM7805



Linear Power Supply

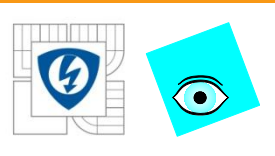
- The most important parameters for voltage regulator selection
 - Input voltage range (V_{IN})
 - Output voltage/current
 - Voltage drop
 - Quiescent current





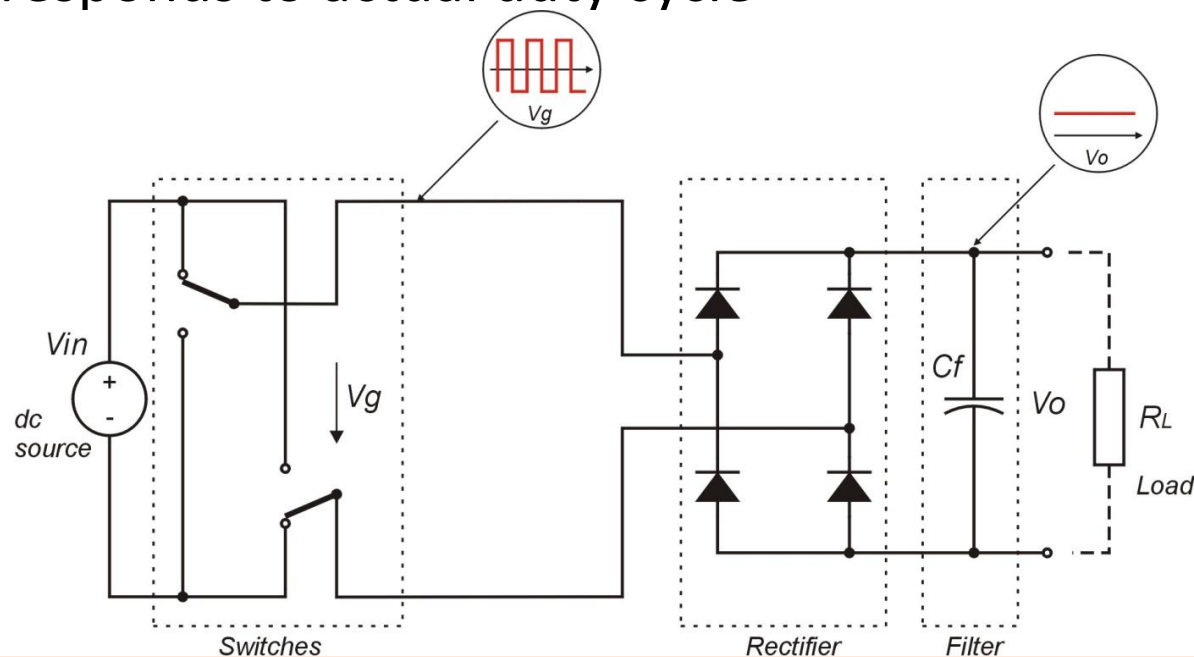
Agenda

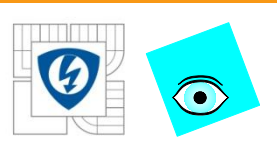
- Linear Regulator
- Non-Isolated SMPS
 - Buck (Step down) Converter
 - Boost (Step up) Converter
 - Buck – Boost (Inverting/Non-inverting) Converter
 - CÚK Converter
 - SEPIC Converter
- Isolated SMPS
- Resonant SMPS
- Digital Control of SMPS
- Hands on (Step down Converter)



Switched Mode Power Supply

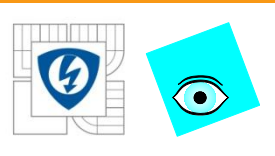
- The semiconductor switches generate square wave voltage output using PWM modulation - V_g
- The V_g is rectified by output rectifier and filtered by a low pass filter
- The V_o corresponds to actual duty cycle





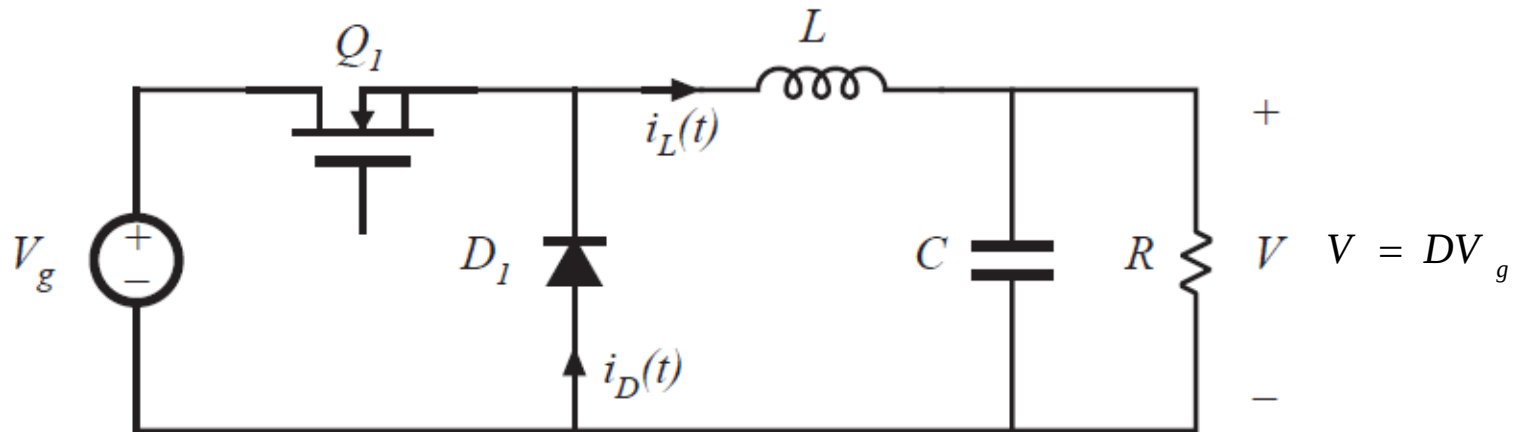
Switched Mode Power Supply

- The semiconductor switches work in ON and OFF state only
- Advantages
 - Very high efficiency
 - Lower/higher output voltage than input
 - Isolated/non isolated solution
 - Can handle very high output power
- Disadvantages
 - More complex design
 - More expensive
 - More noisy due to switching



Buck Converter

- Step down non isolated converter

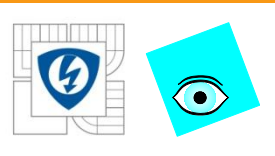


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

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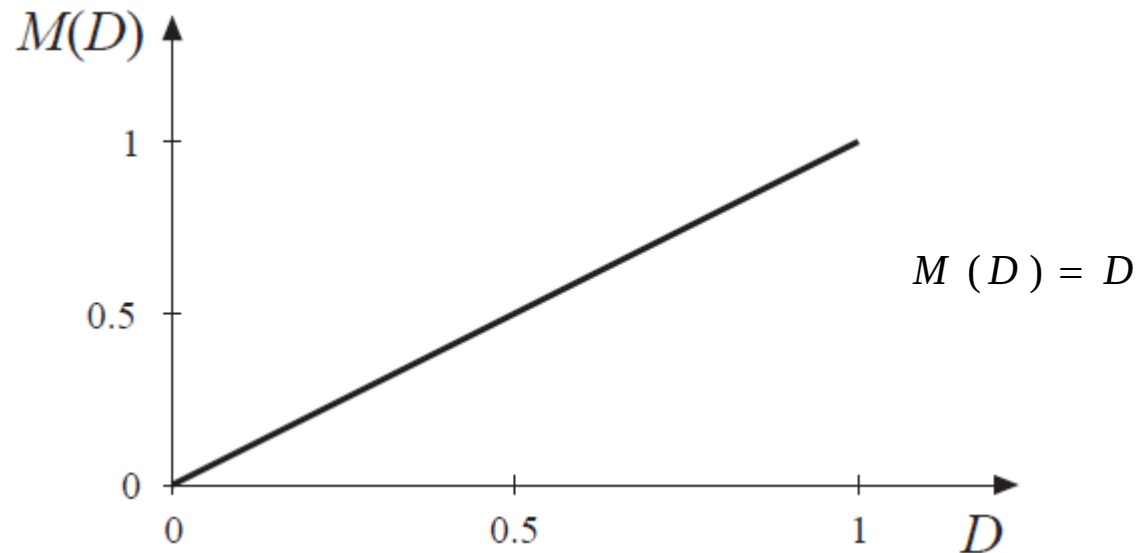
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Buck Converter

- Output transfer function of buck converter

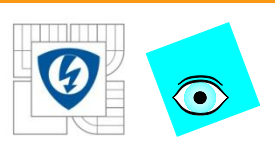


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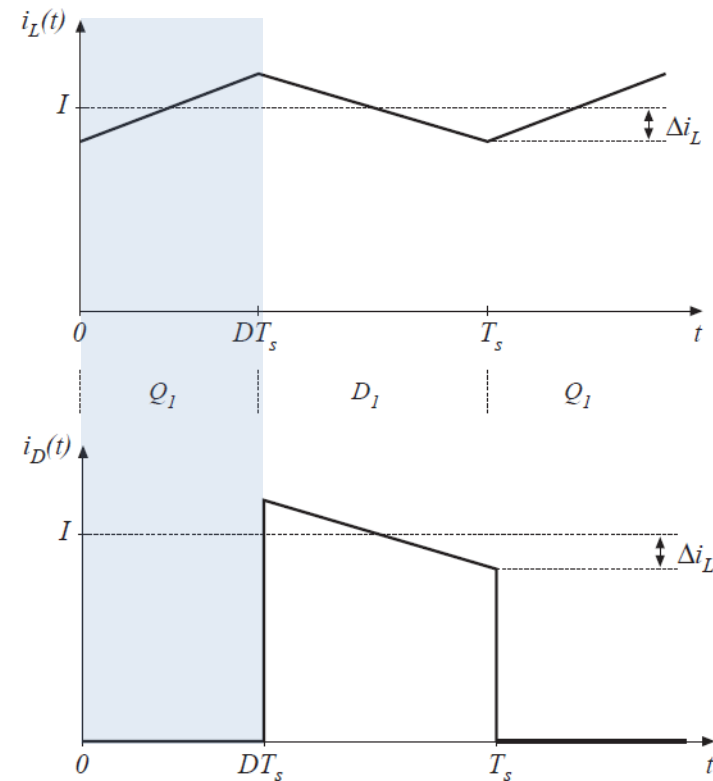
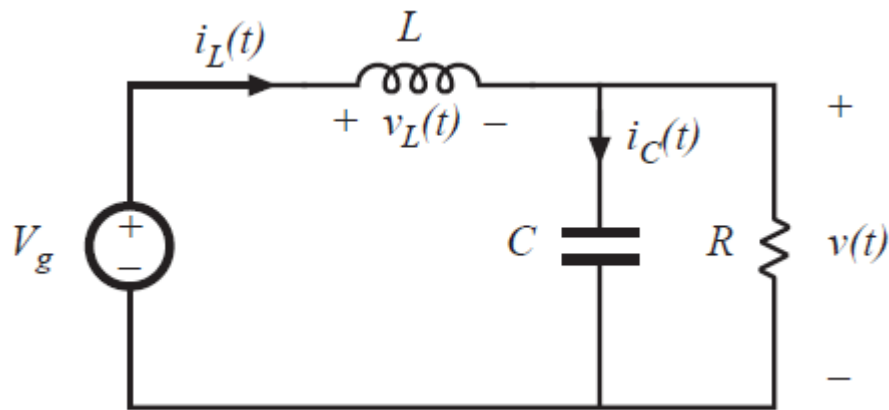




Buck Converter

- Continuous conduction operation of Buck Converter

First sub-interval

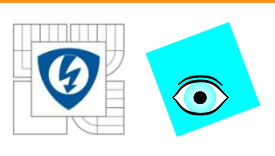


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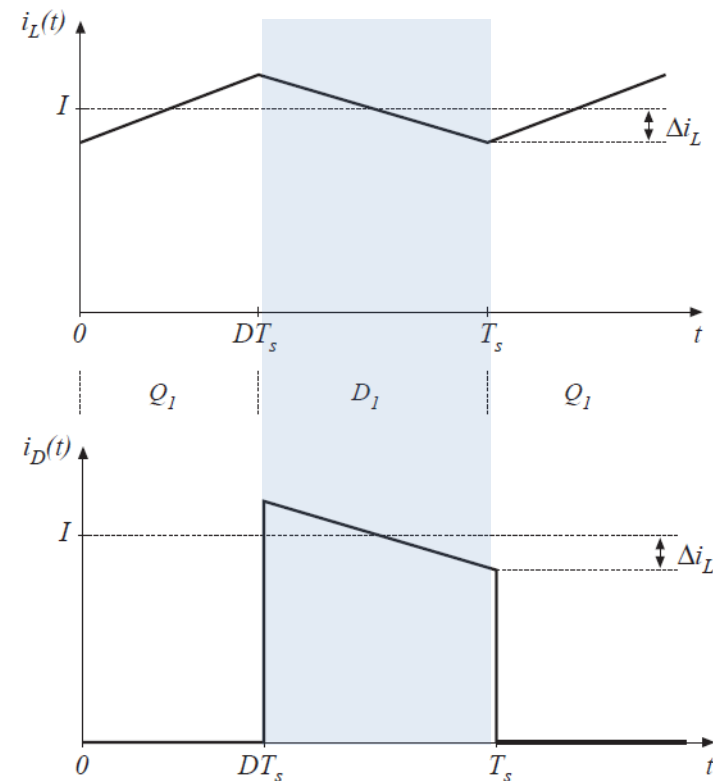
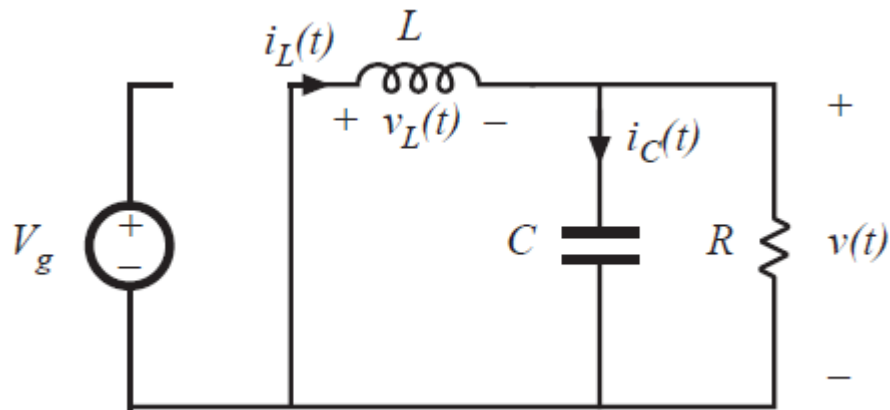




Buck Converter

- Continuous conduction operation of Buck Converter

Second sub-interval

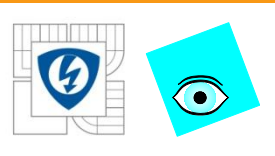


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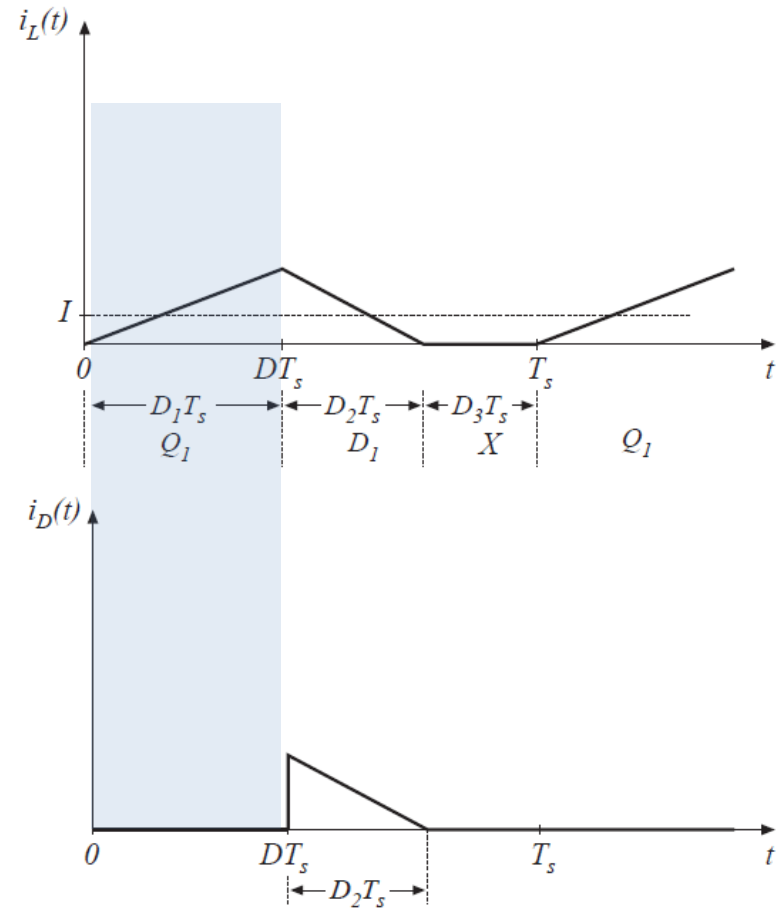
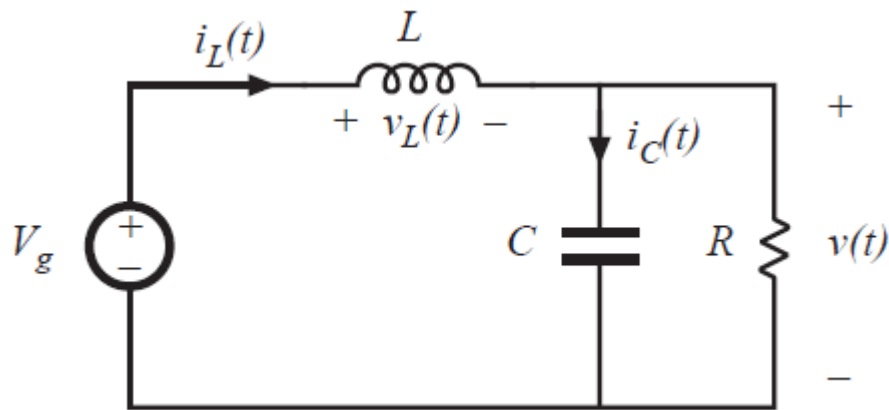




Buck Converter

- Discontinuous conduction operation of Buck Converter

First sub-interval

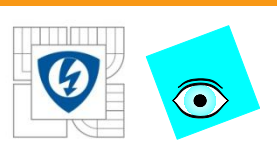


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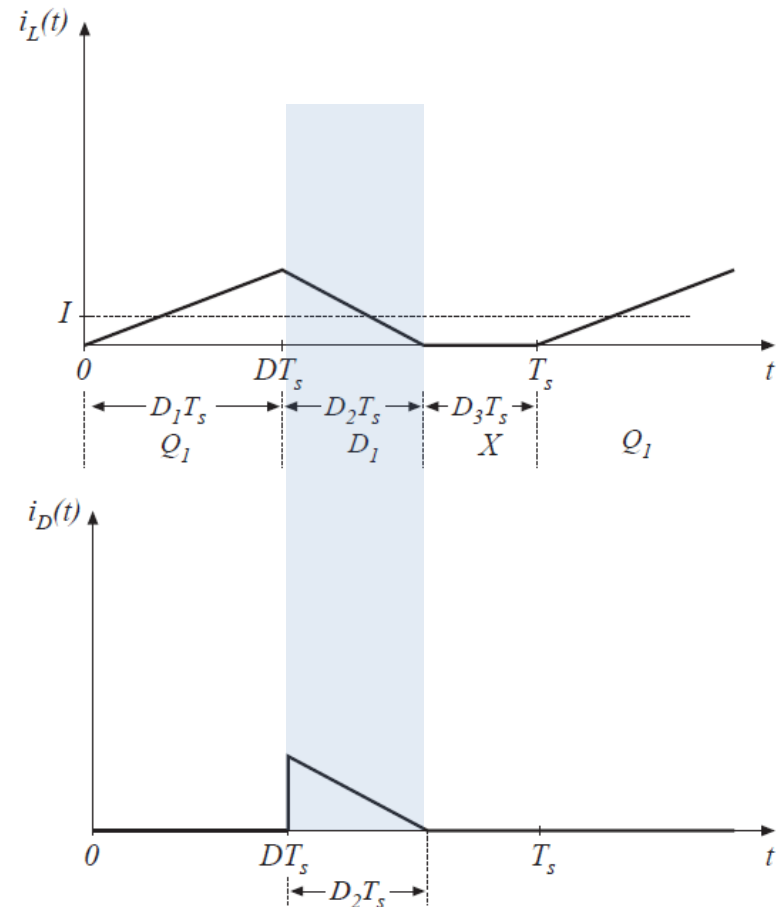
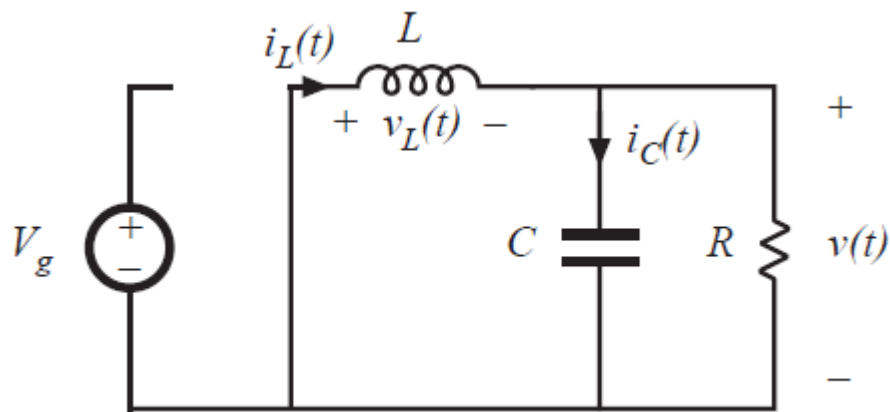




Buck Converter

- Discontinuous conduction operation of Buck Converter

Second sub-interval

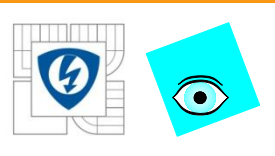


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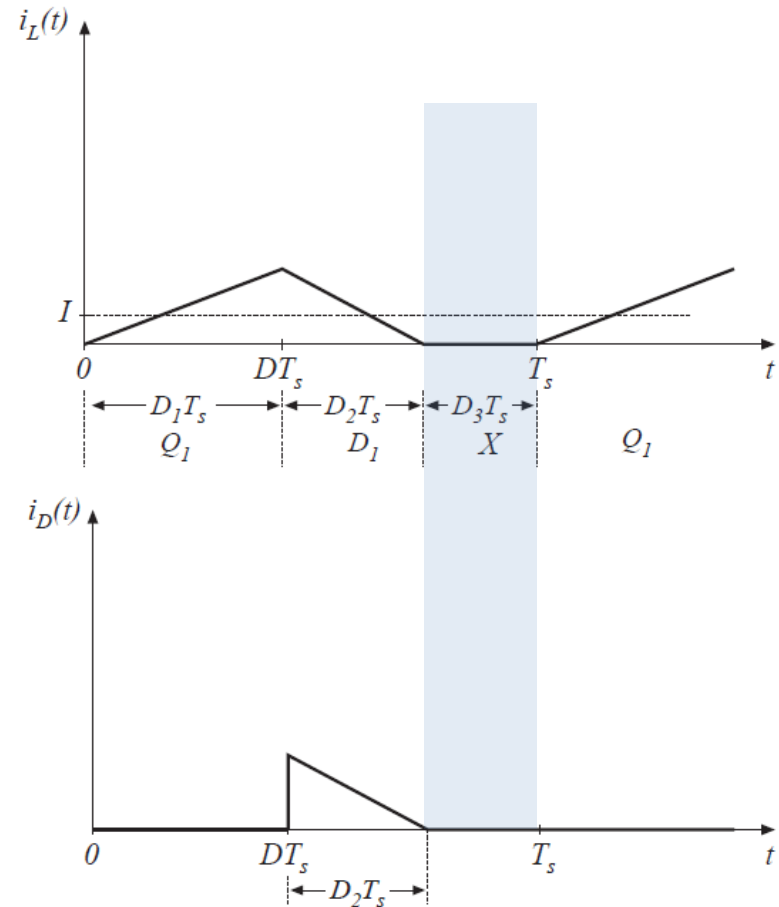
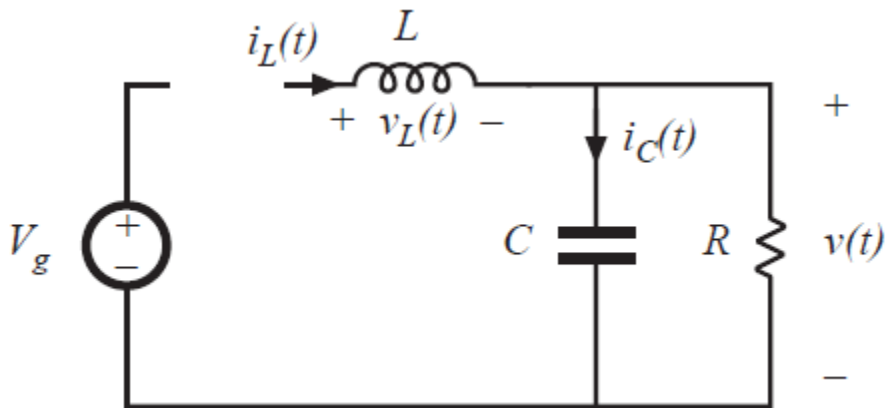




Buck Converter

- Discontinuous conduction operation of Buck Converter

Third sub-interval

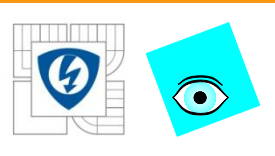


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

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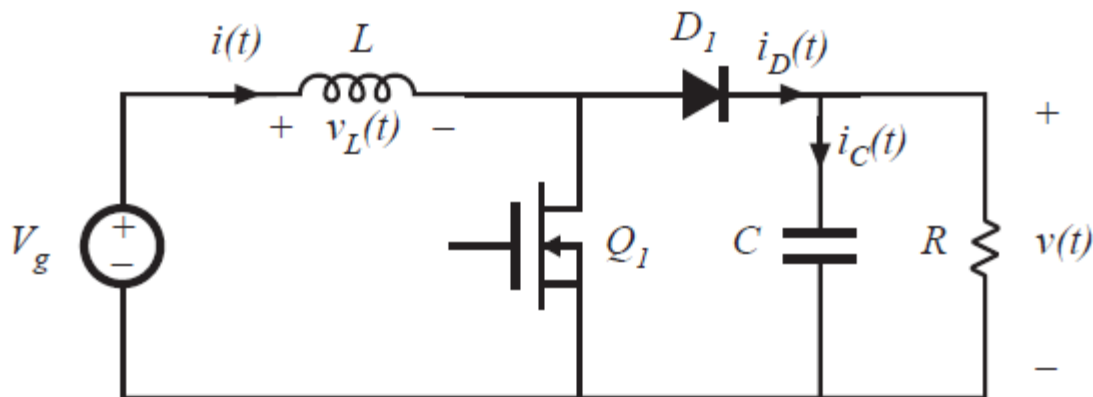
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Boost Converter

- Step up non isolated converter



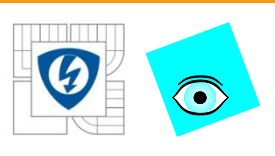
$$V = \frac{V_g}{1 - D}$$

Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

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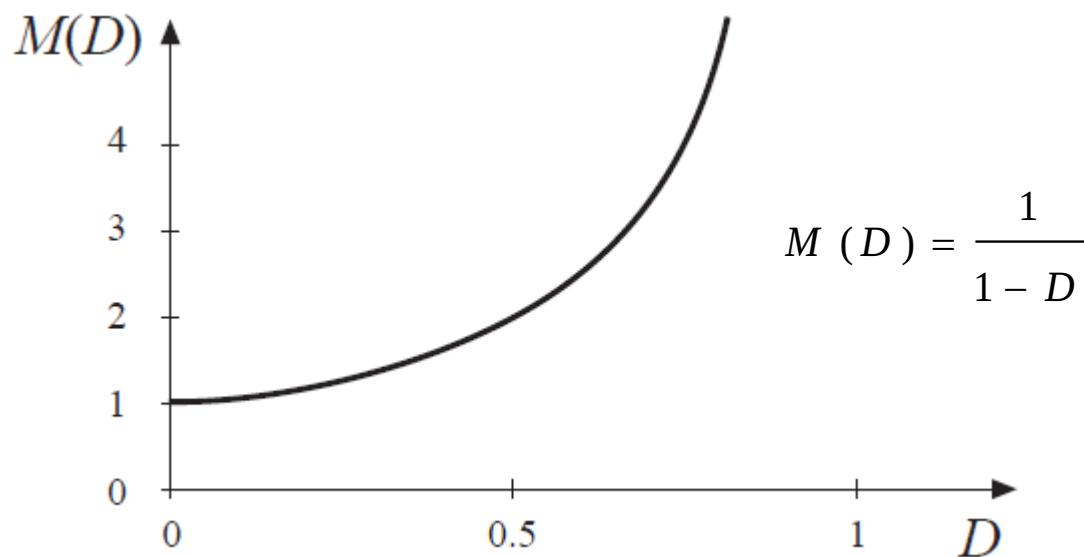
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Boost Converter

- Output transfer function of boost converter

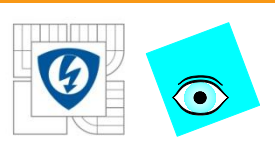


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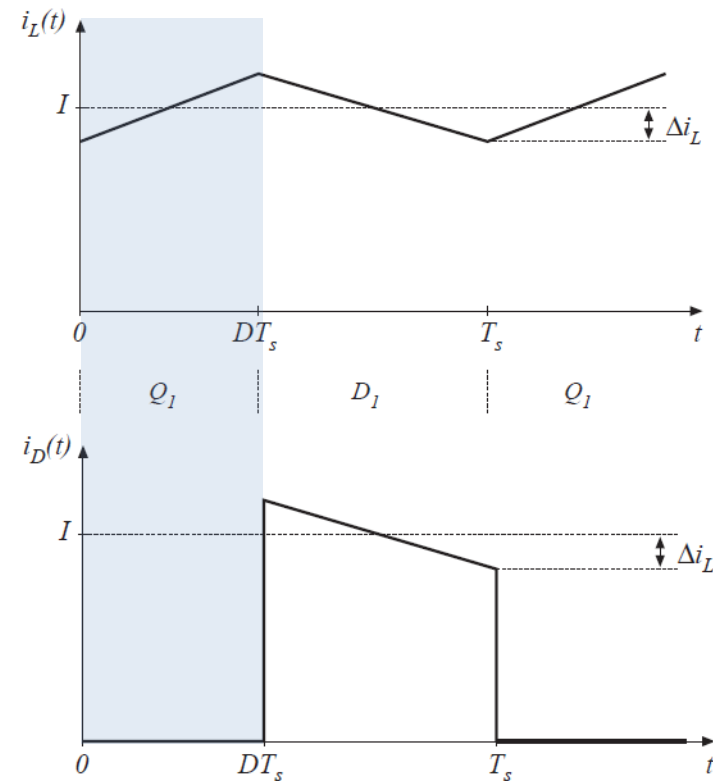
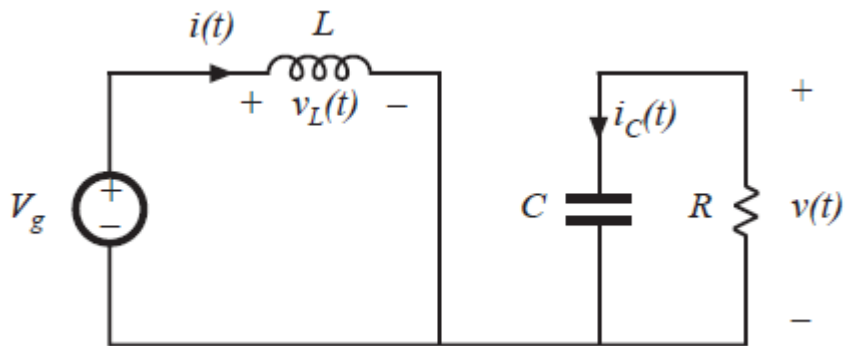




Boost Converter

- Continuous conduction operation of Boost Converter

First sub-interval

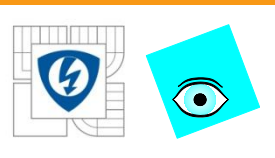


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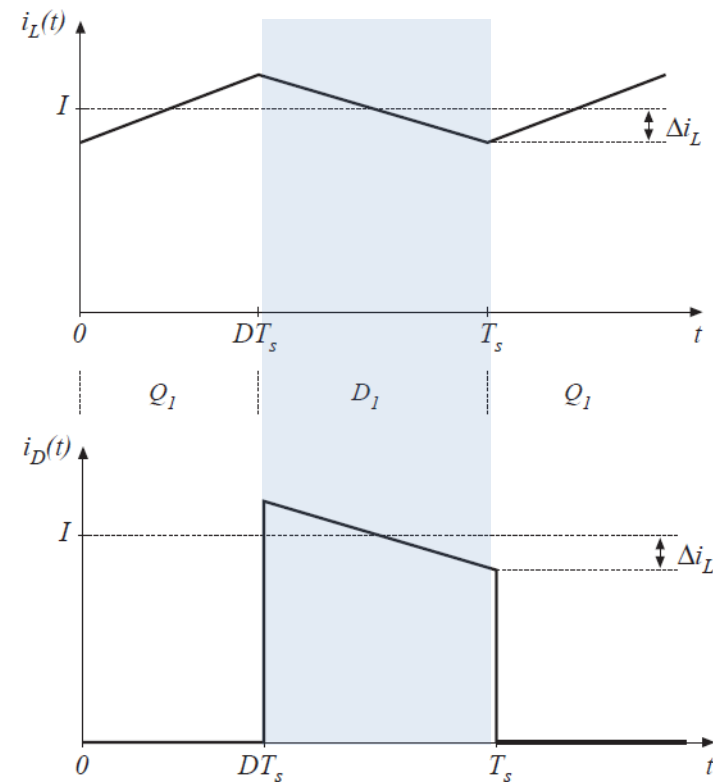
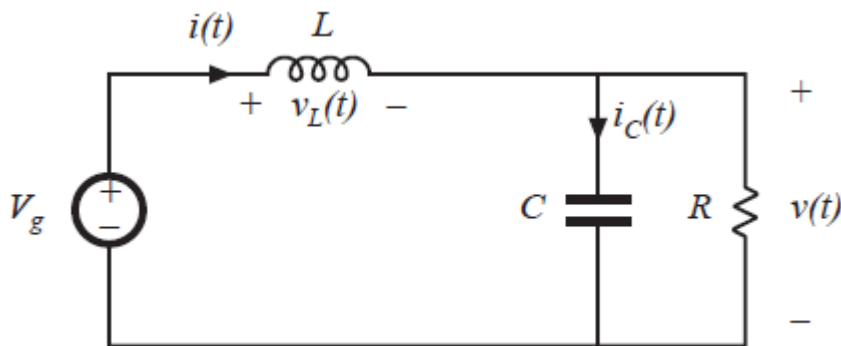




Boost Converter

- Continuous conduction operation of Boost Converter

Second sub-interval

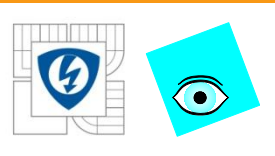


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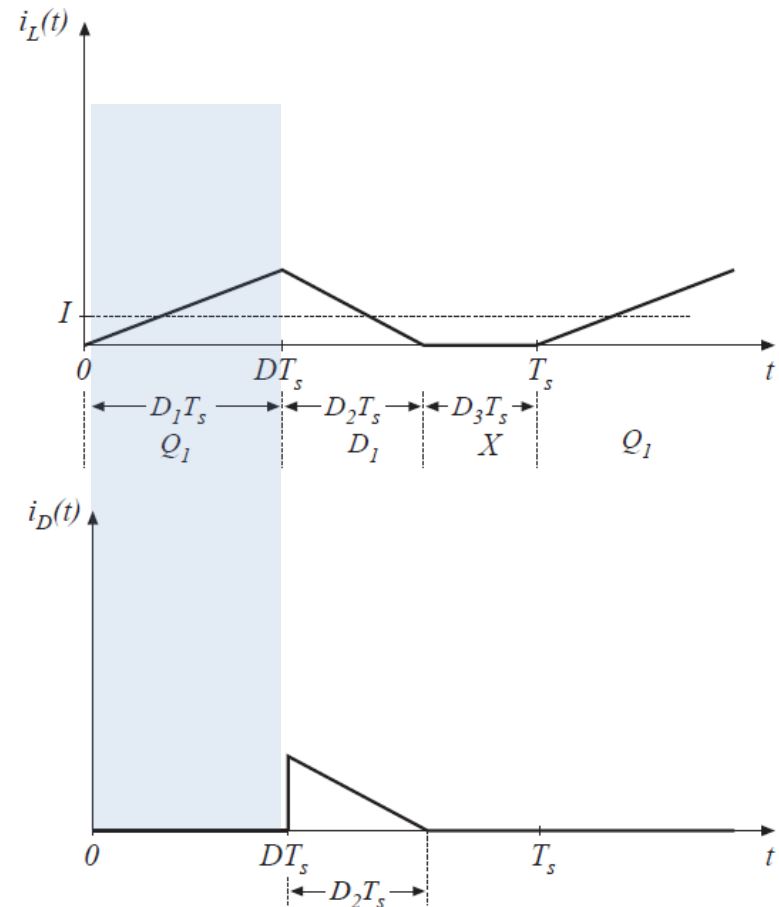
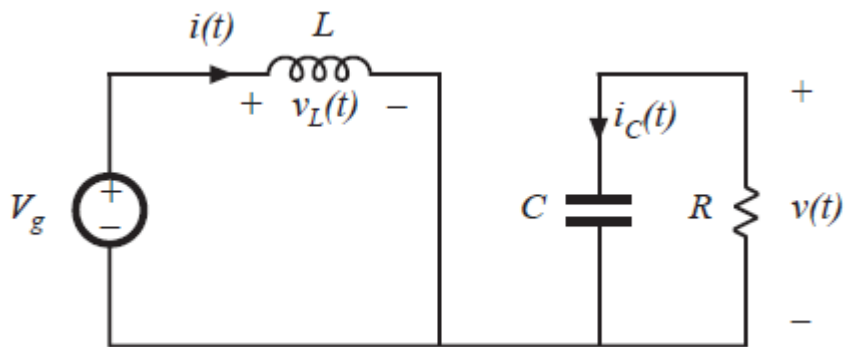




Boost Converter

- Discontinuous conduction operation of Boost Converter

First sub-interval

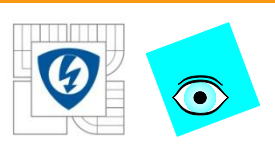


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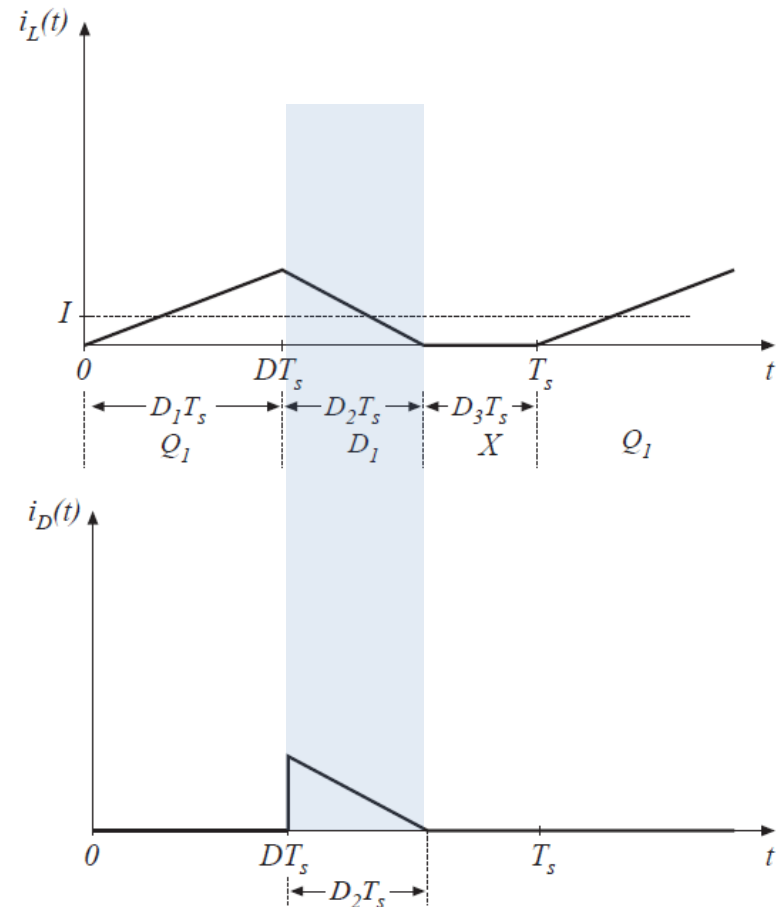
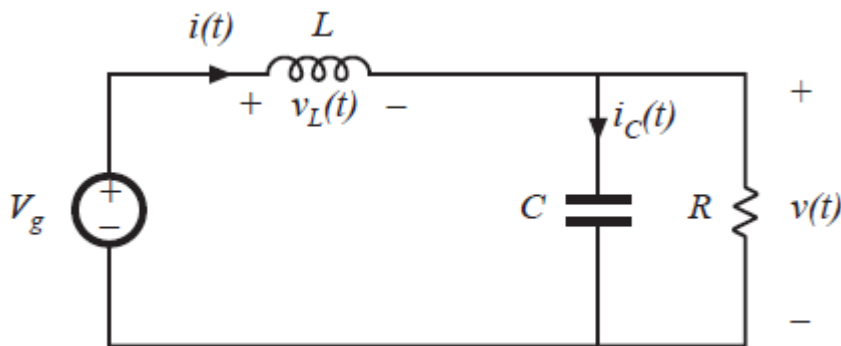




Boost Converter

- Discontinuous conduction operation of Boost Converter

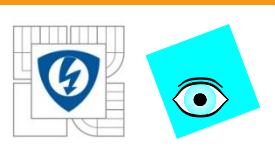
Second sub-interval



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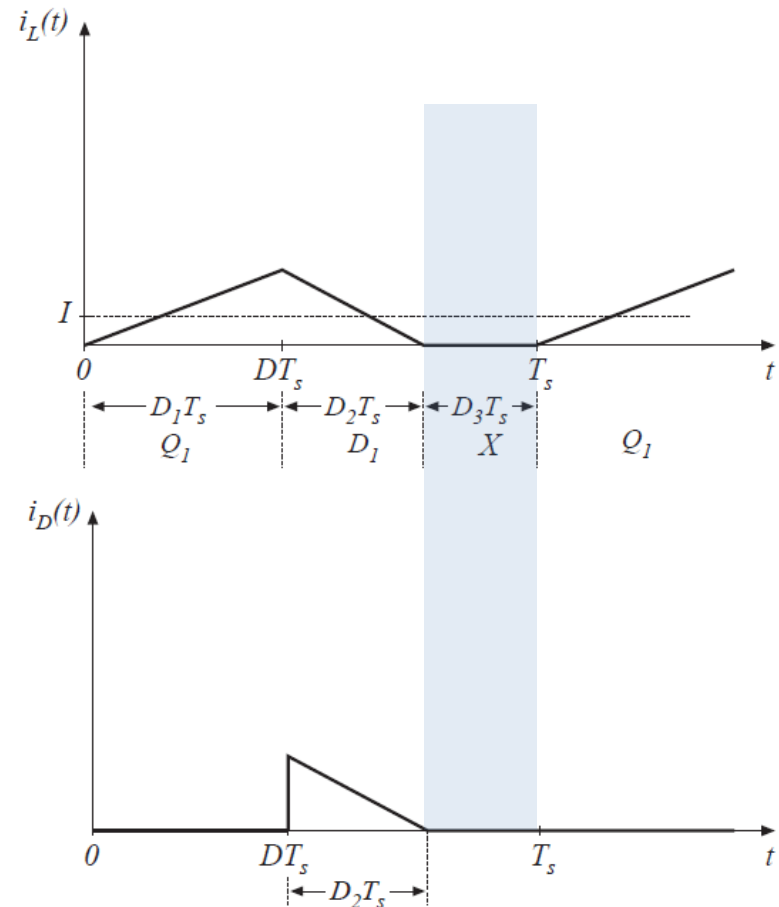
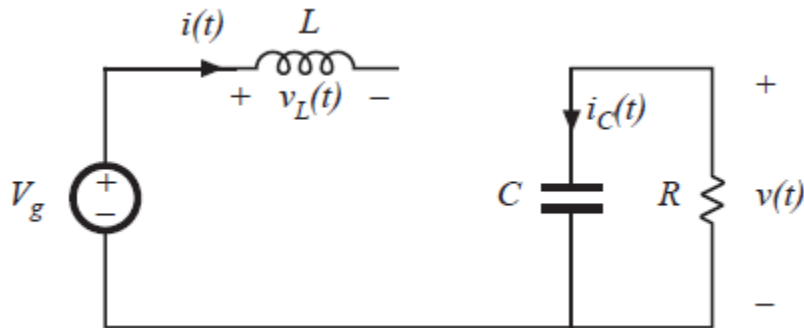
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Boost Converter

- Discontinuous conduction operation of Boost Converter

Third sub-interval

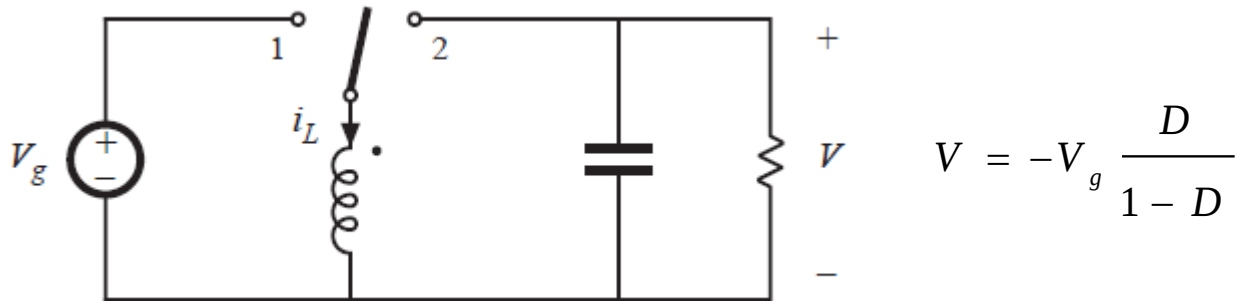


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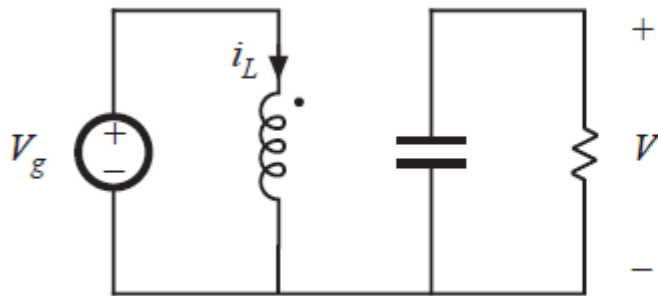
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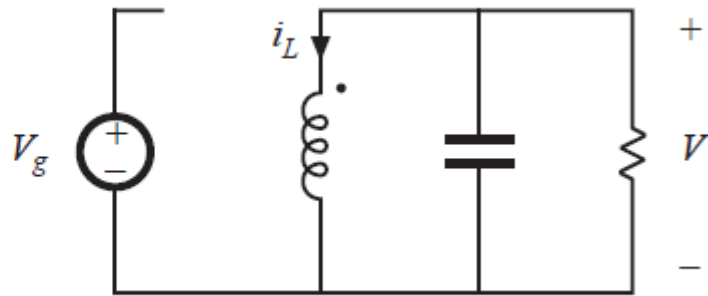
Buck-Boost Converter (inverting)



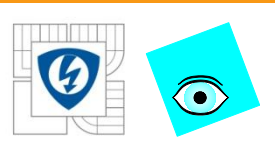
First sub-interval



Second sub-interval

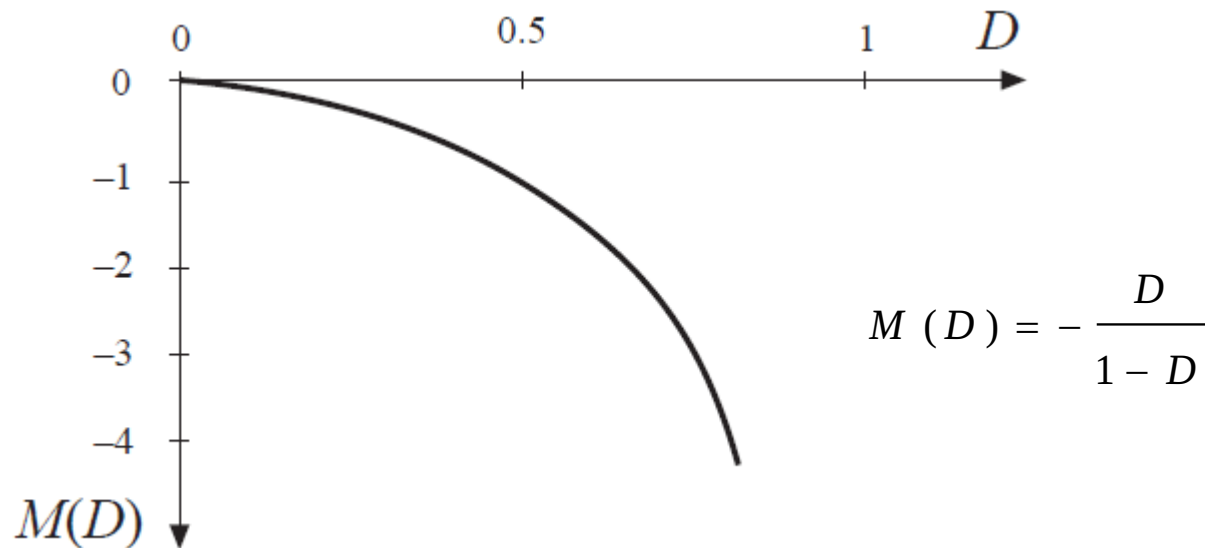


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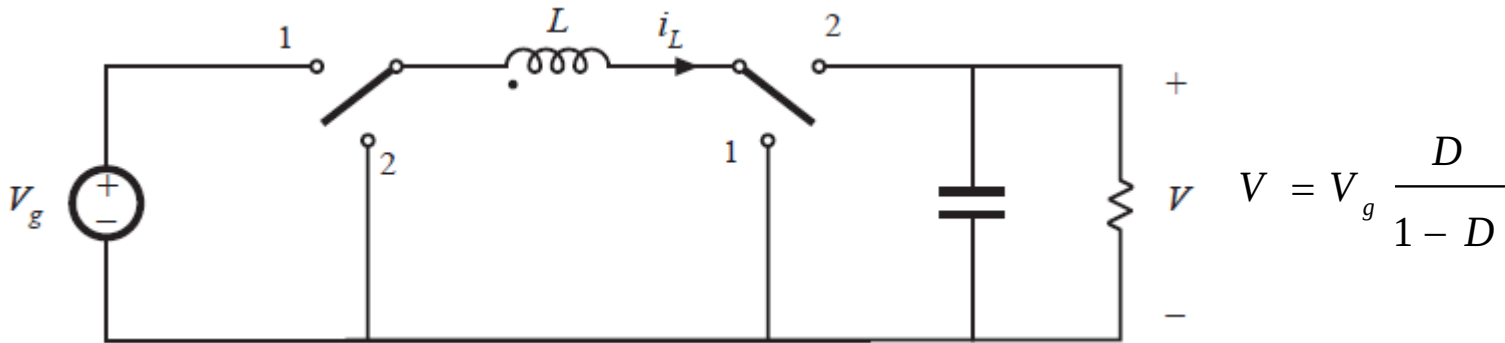
Buck-Boost Converter (inverting)

- Output transfer function of buck-boost Converter

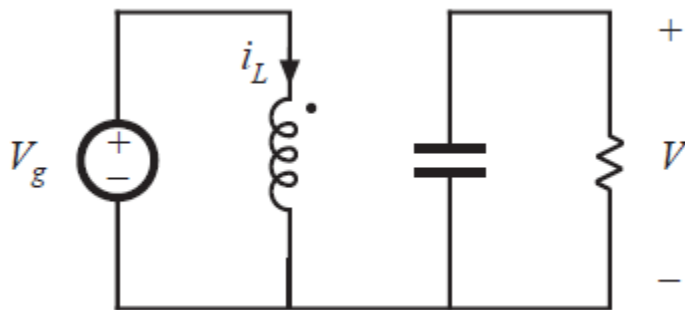


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

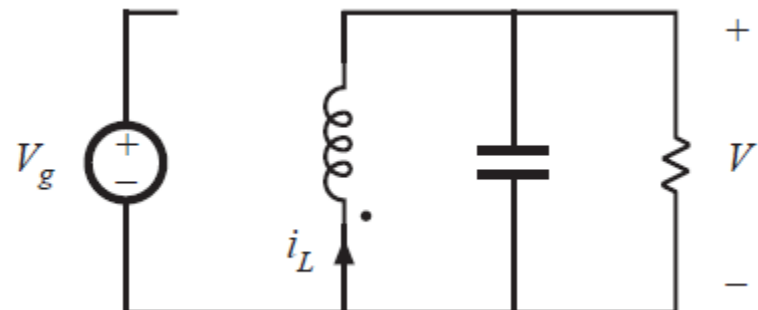
Buck-Boost Converter (non inverting)



First sub-interval



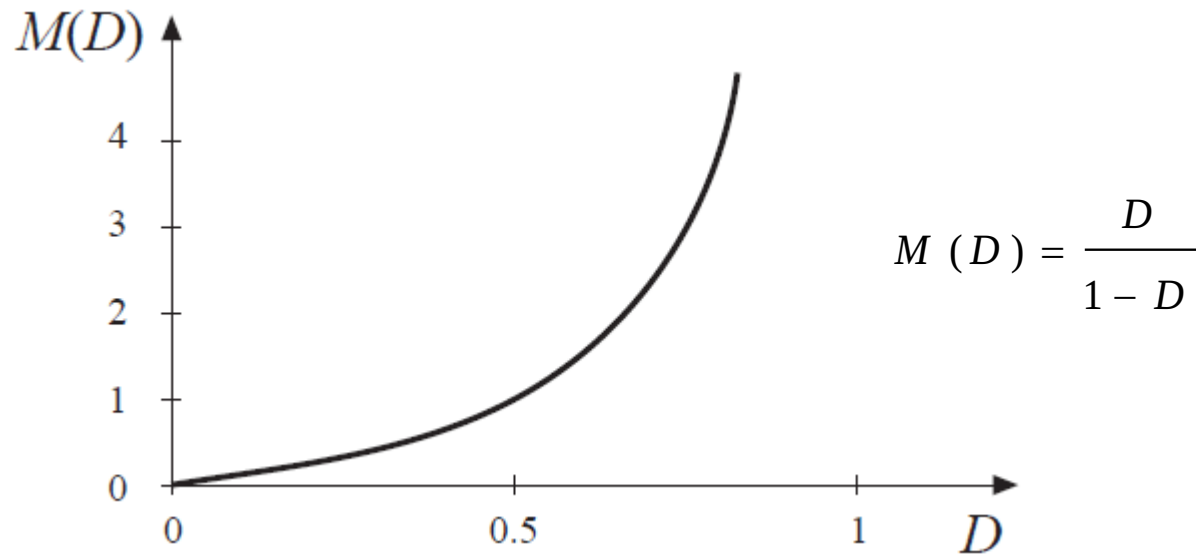
Second sub-interval



Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

Buck-Boost Converter (non inverting)

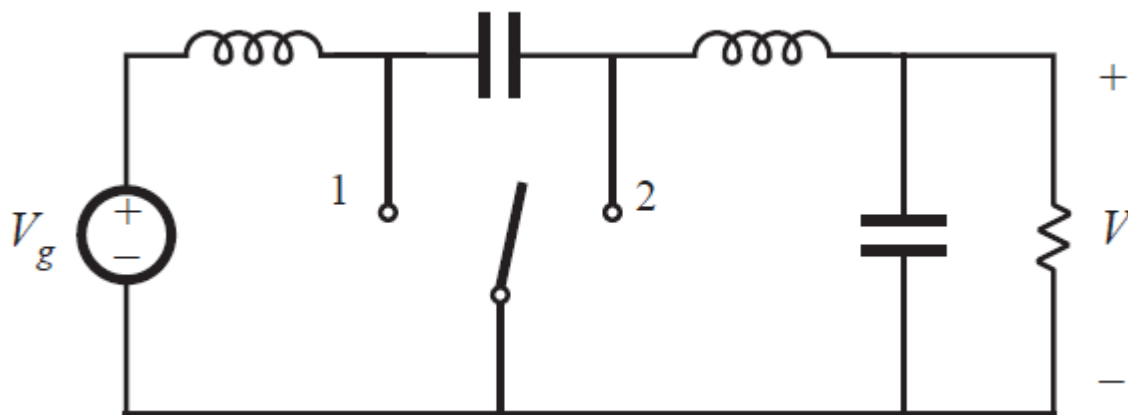
- Output transfer function of buck-boost Converter



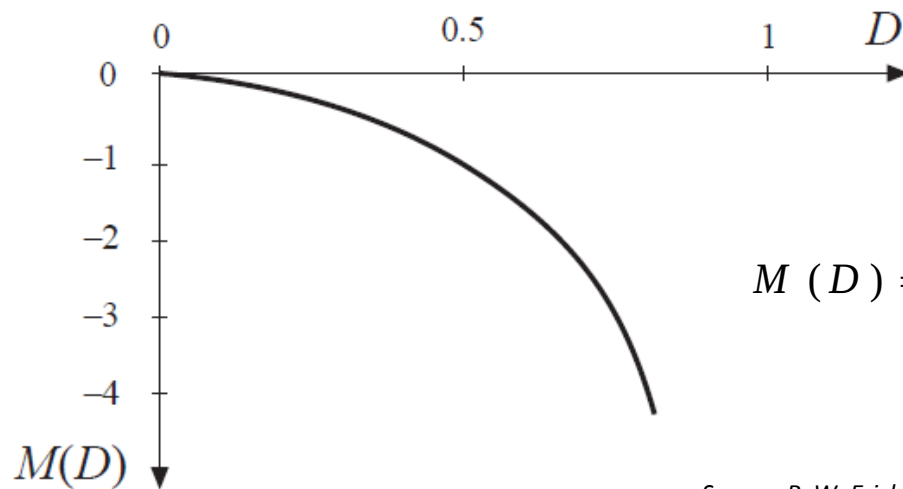
Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*



CÚK Converter

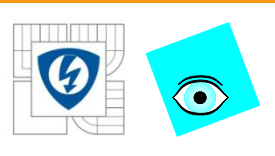


$$V = -V_g \frac{D}{1 - D}$$

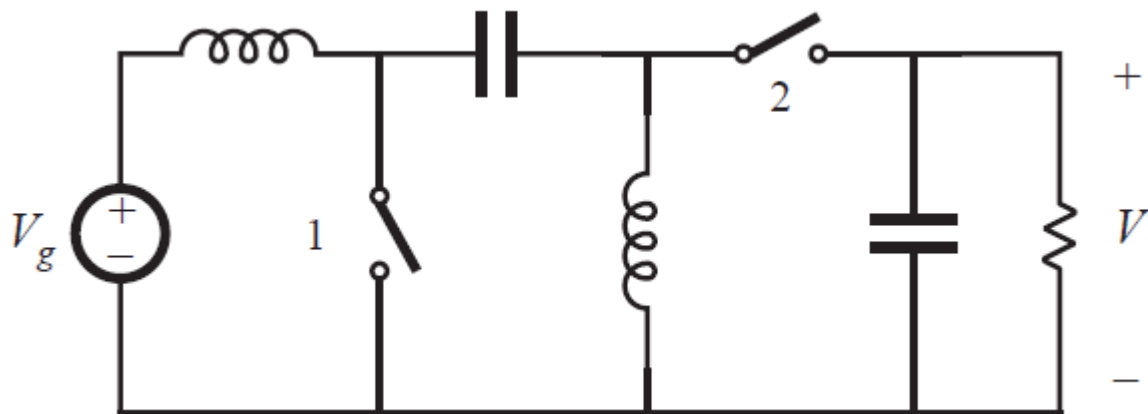


$$M(D) = - \frac{D}{1 - D}$$

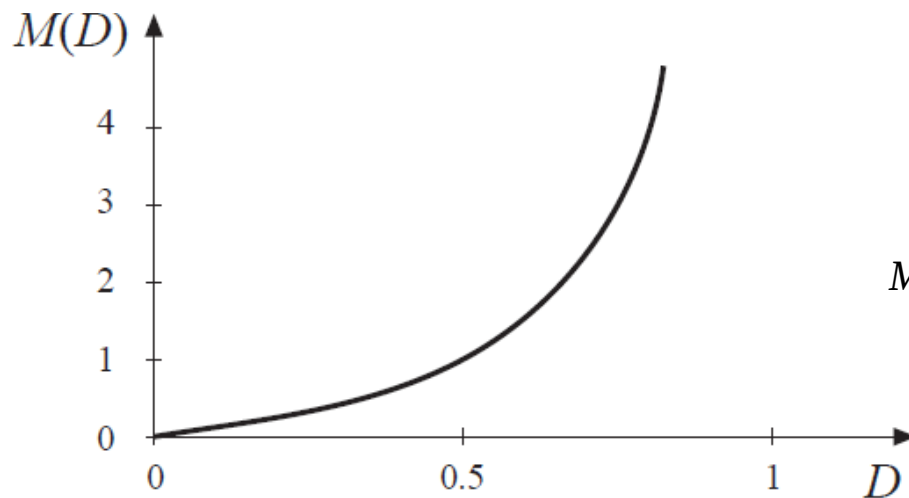
Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*



SEPIC Converter

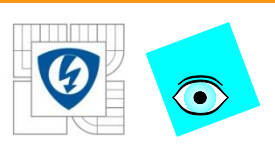


$$V = V_g \frac{D}{1 - D}$$



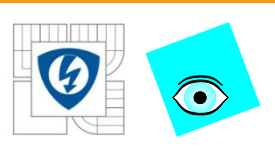
$$M(D) = \frac{D}{1 - D}$$

Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*



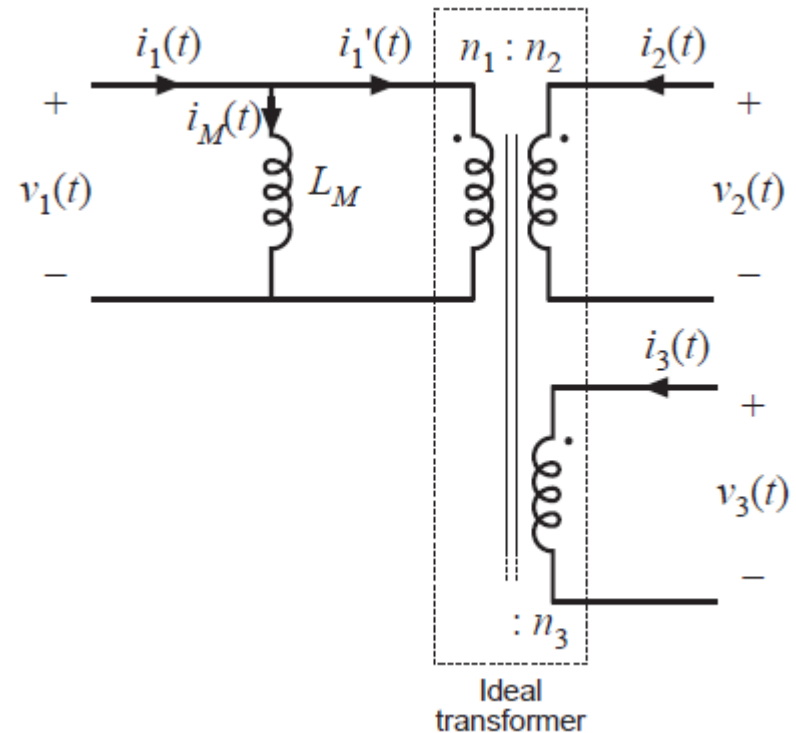
Agenda

- Linear Regulator
- Non-Isolated SMPS
- Isolated SMPS
 - Flyback Converter
 - Forward Converter
 - Push Pull Converter
 - Half Bridge
 - Full Bridge
- Resonant SMPS
- Digital Control of SMPS
- Hands on (Step down Converter)



Transformer in SMPS

- When use the transformer?
 - Isolated SMPS
 - To high ratio between input/output voltage (optimize operation conditions)
 - Multiple output SMPS

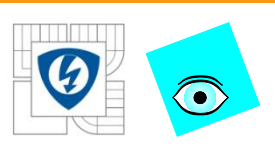


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

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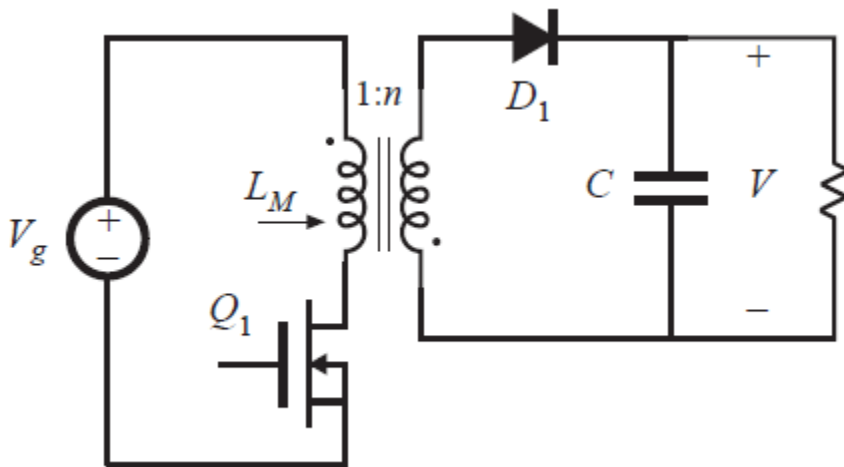
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





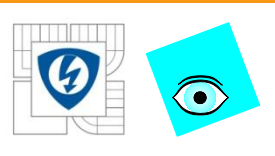
FlyBack Converter

- The primary and secondary windings have opposite polarity
- The energy is stored in the magnetic core gap
- The least number of the components
- Suitable for output power <150W



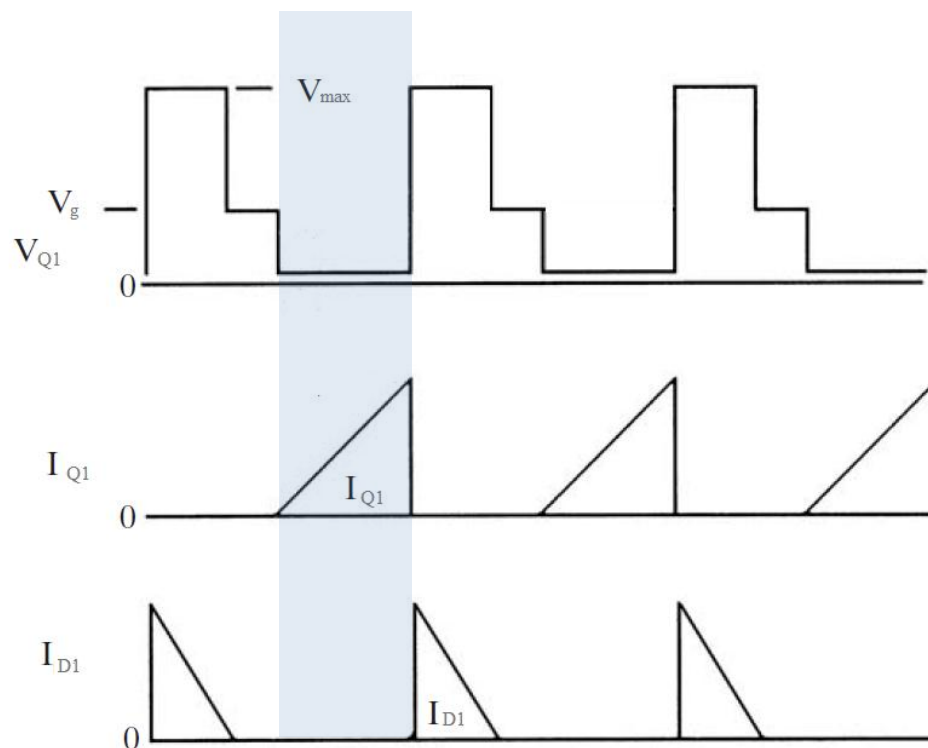
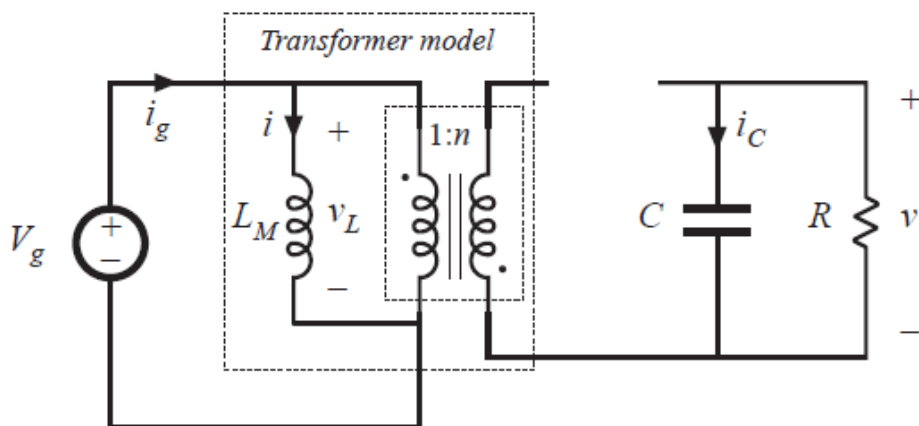
$$M(D) = D \sqrt{\frac{T_P V_{OUT}}{2 I_{OUT} L_P}}$$

Source: R. W. Erickson, D. Maksimović: Fundamentals of Power Electronics



FlyBack Converter

- Sub-interval 1

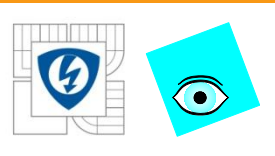


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

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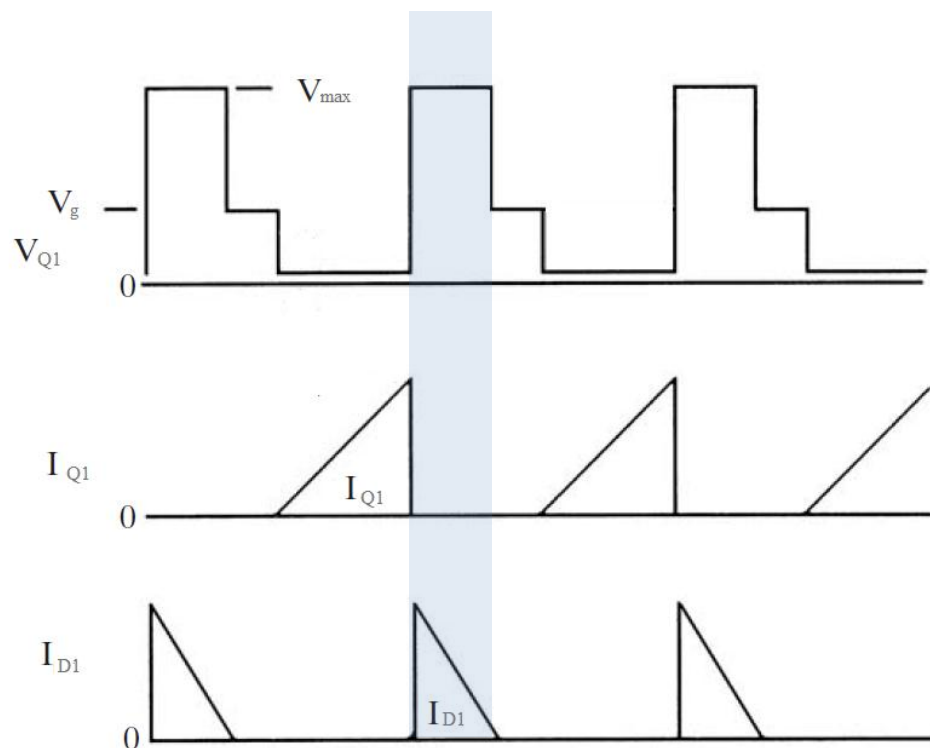
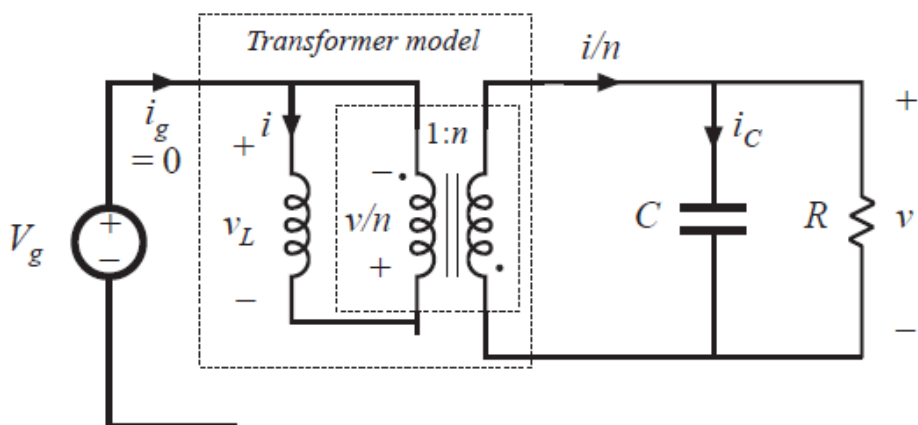
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





FlyBack Converter

- Sub-interval 2

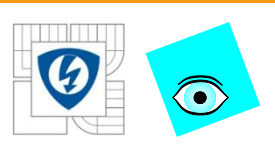


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

31.5-1. 6. 2012

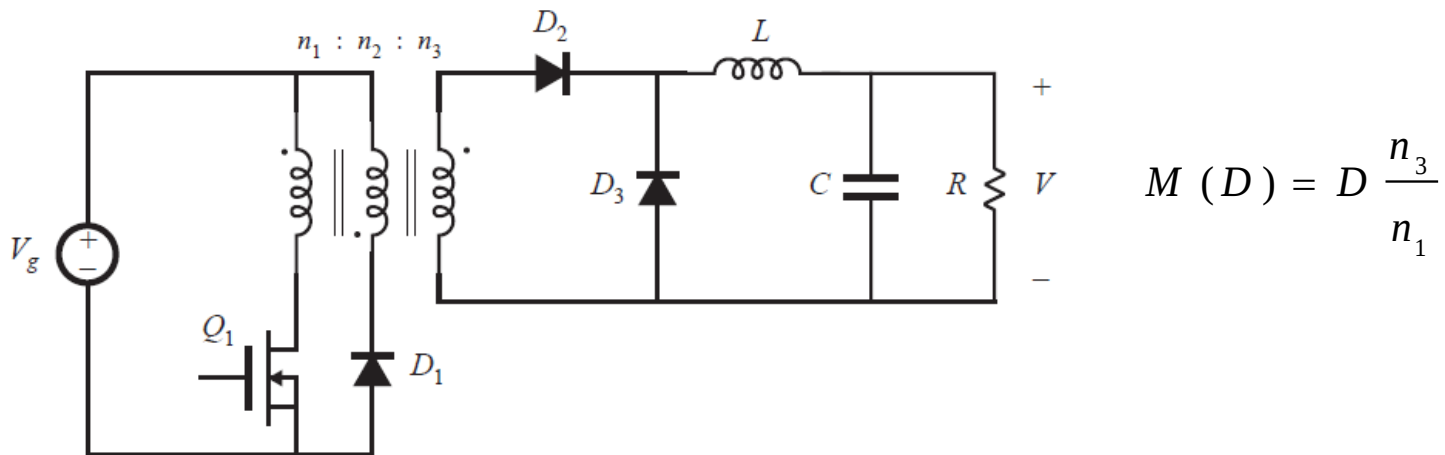
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Forward Converter

- Sub-interval 2

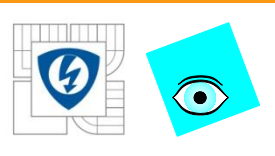


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

31.5-1. 6. 2012

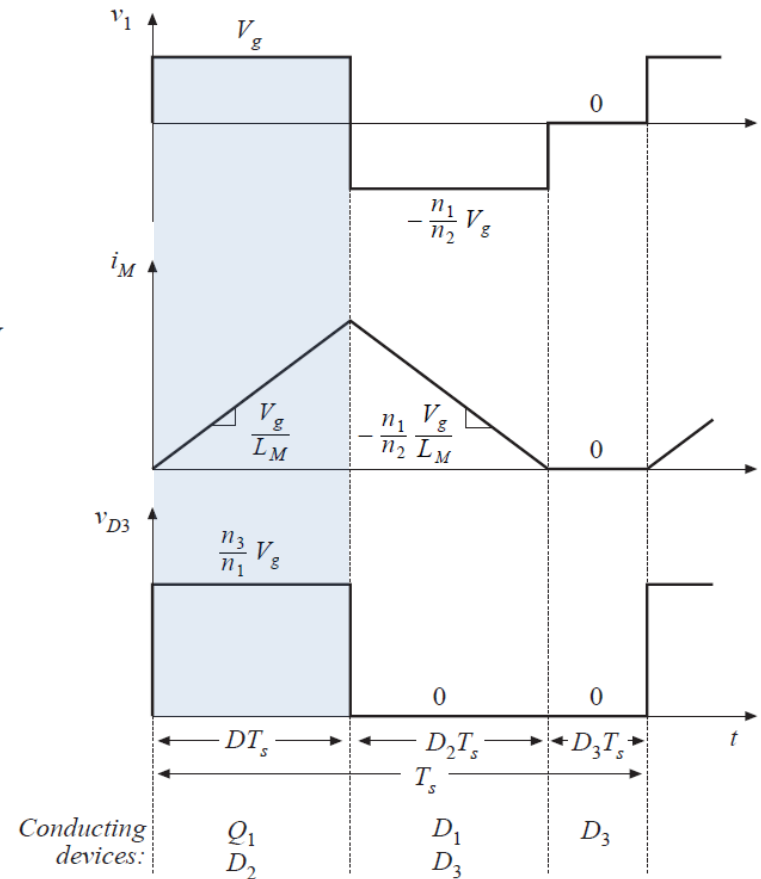
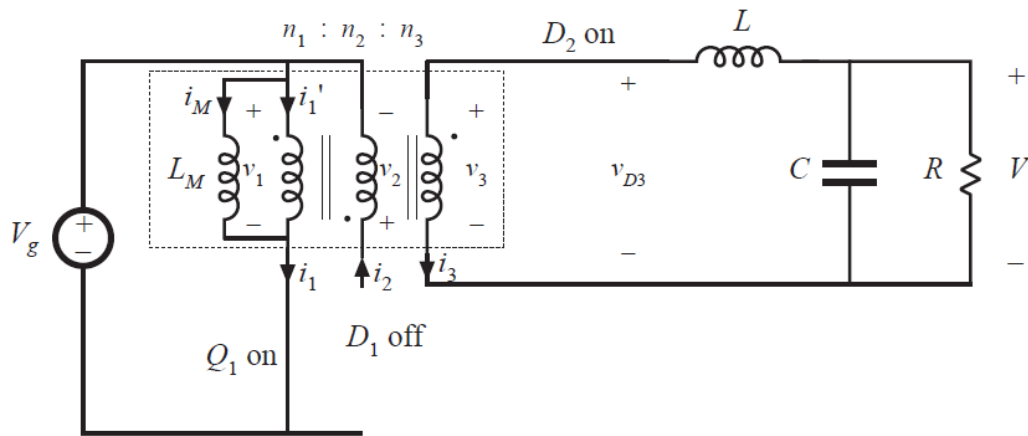
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Forward Converter

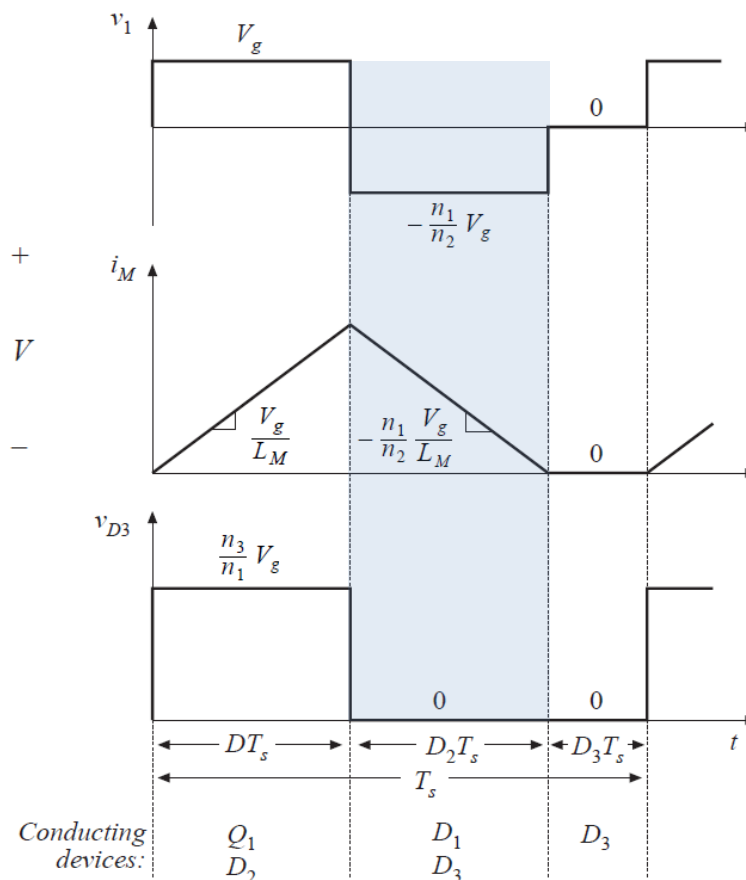
• Sub-interval 1



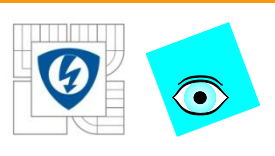
Source: R. W. Erickson, D. Maksimović: Fundamentals of Power Electronics

31.5-1. 6. 2012

INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ

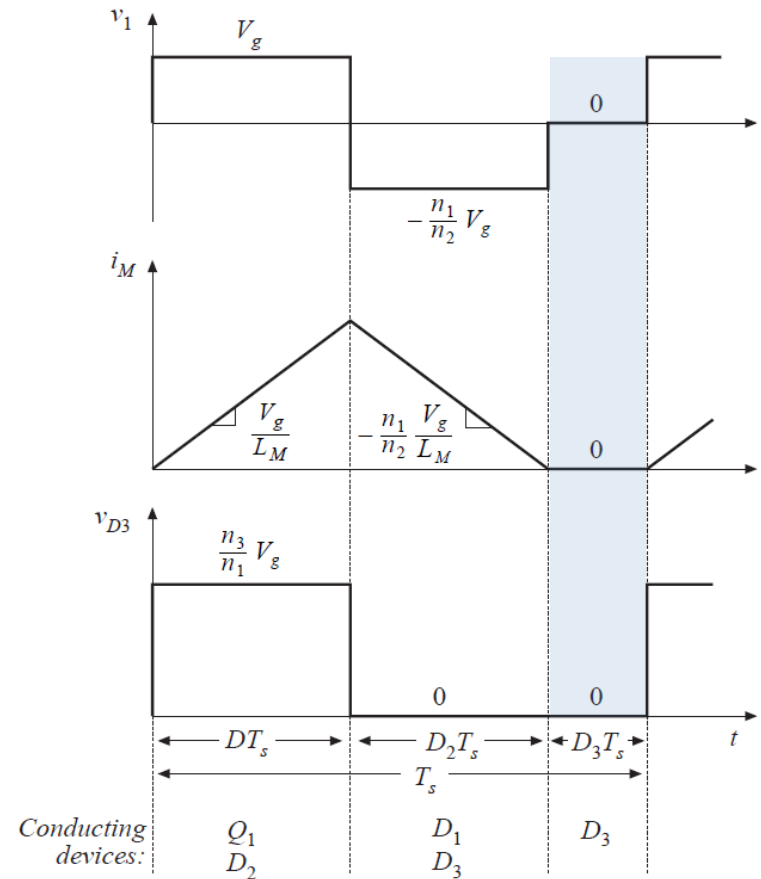
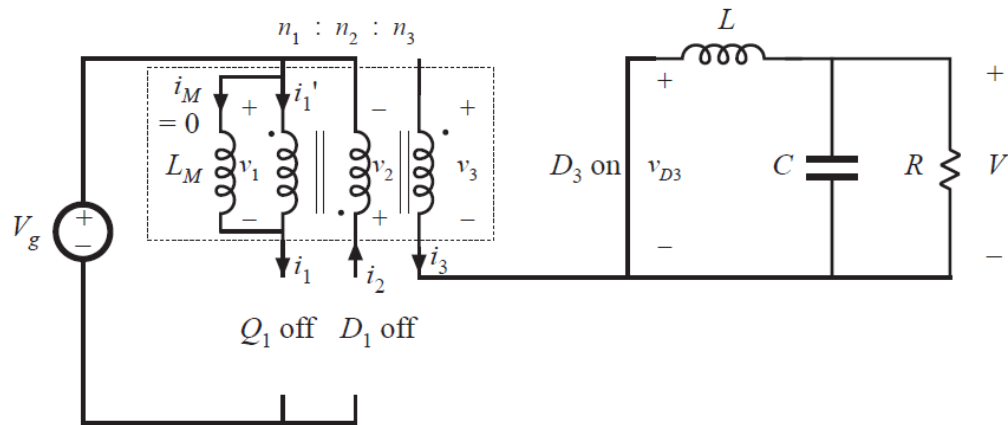


31.5-1. 6. 2012

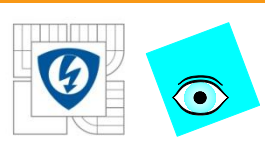


Forward Converter

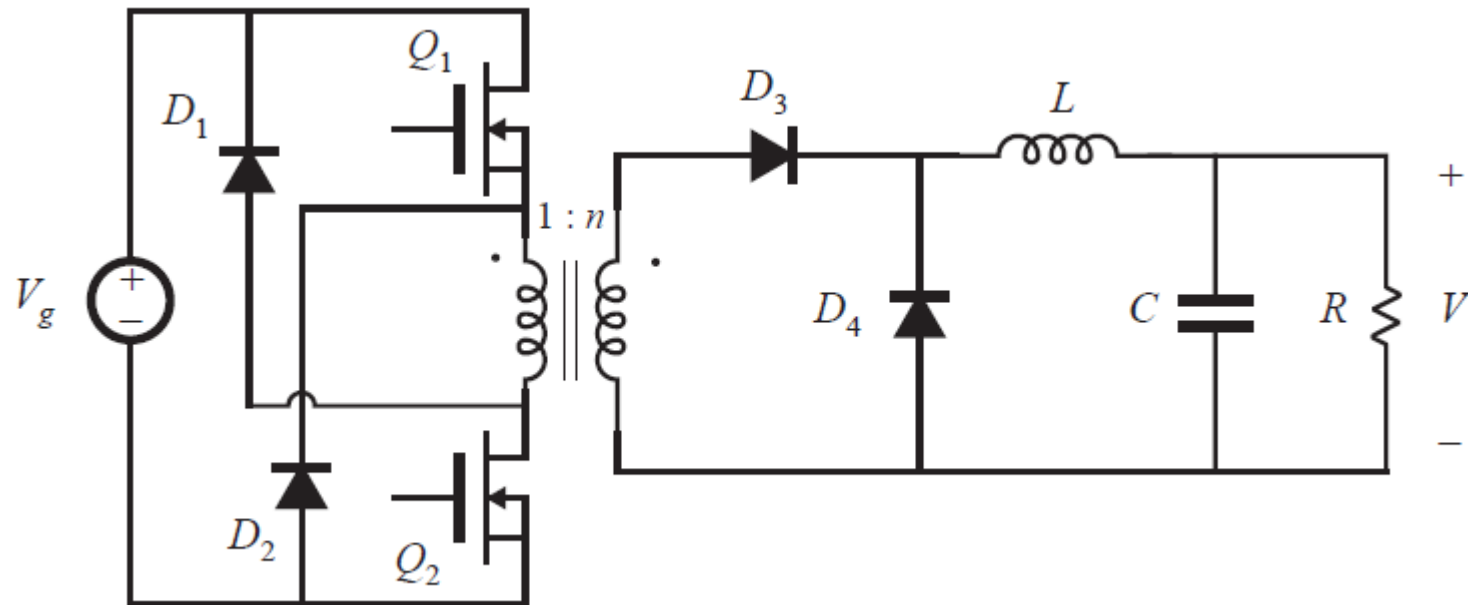
• Sub-interval 3



Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*



2-Switch Forward Converter

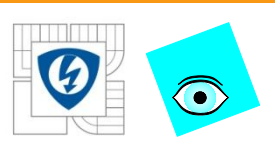


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

31.5-1. 6. 2012

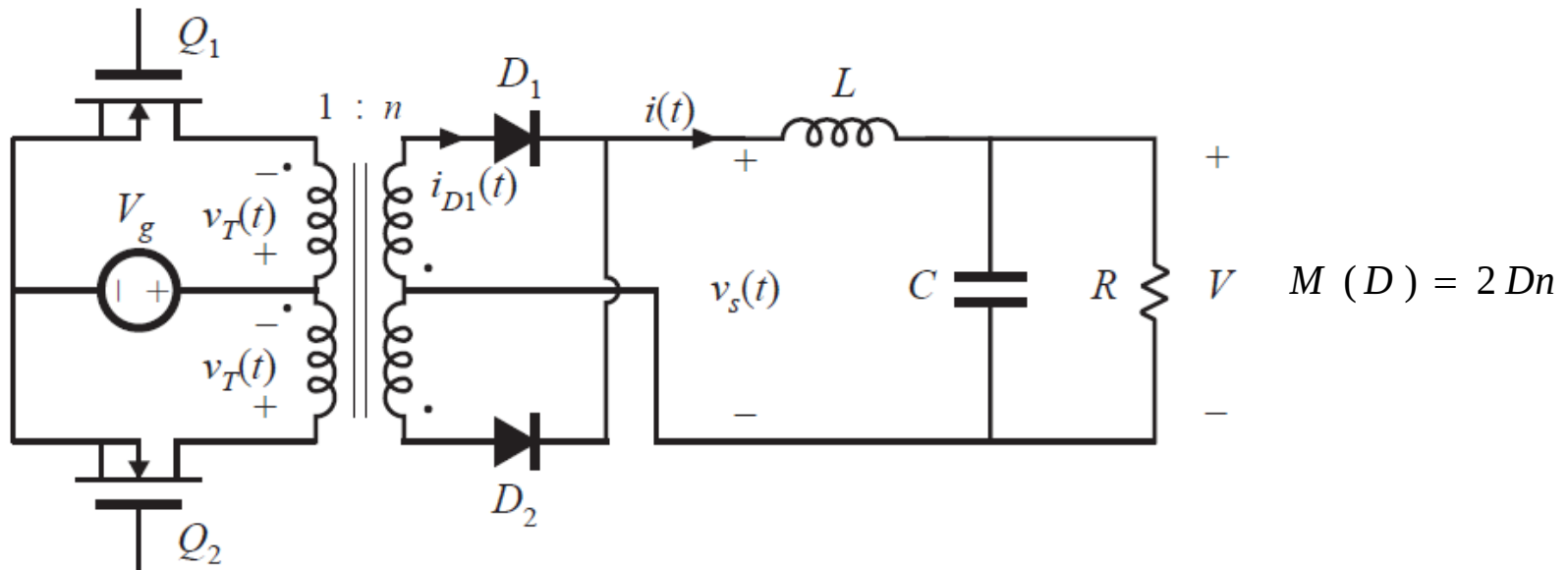
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



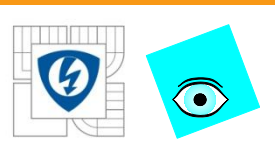


Push Pull Converter

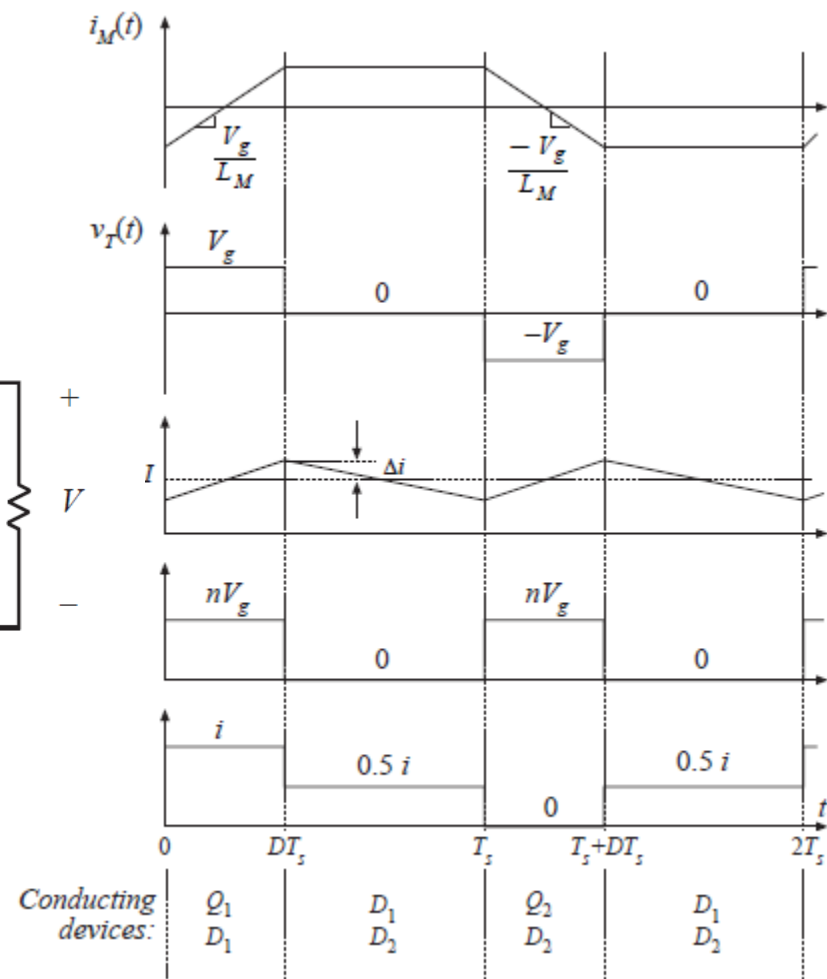
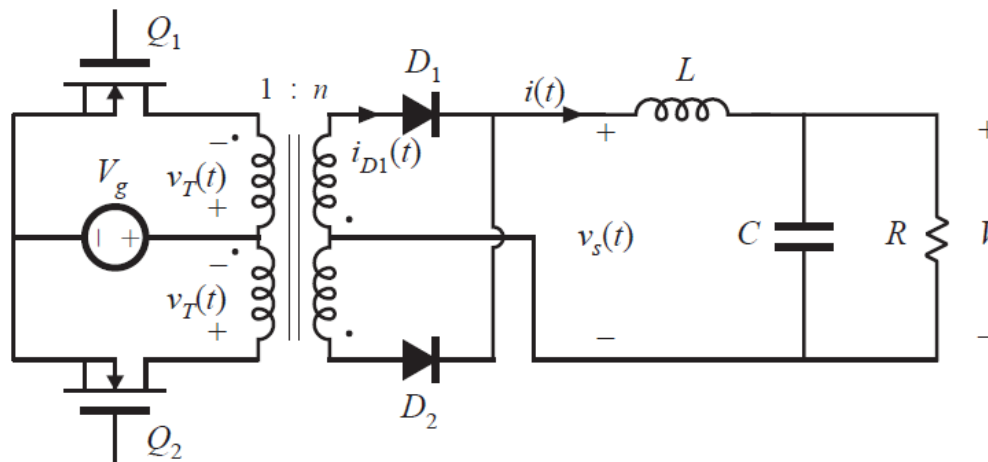
- Usually used as step up converter ($V > V_g$) or with low input voltage
- The transistors have to withstand $2V_g$



Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*



Push Pull Converter

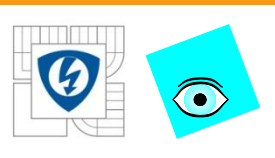


Source: R. W. Erickson, D. Maksimović: Fundamentals of Power Electronics

31.5-1. 6. 2012

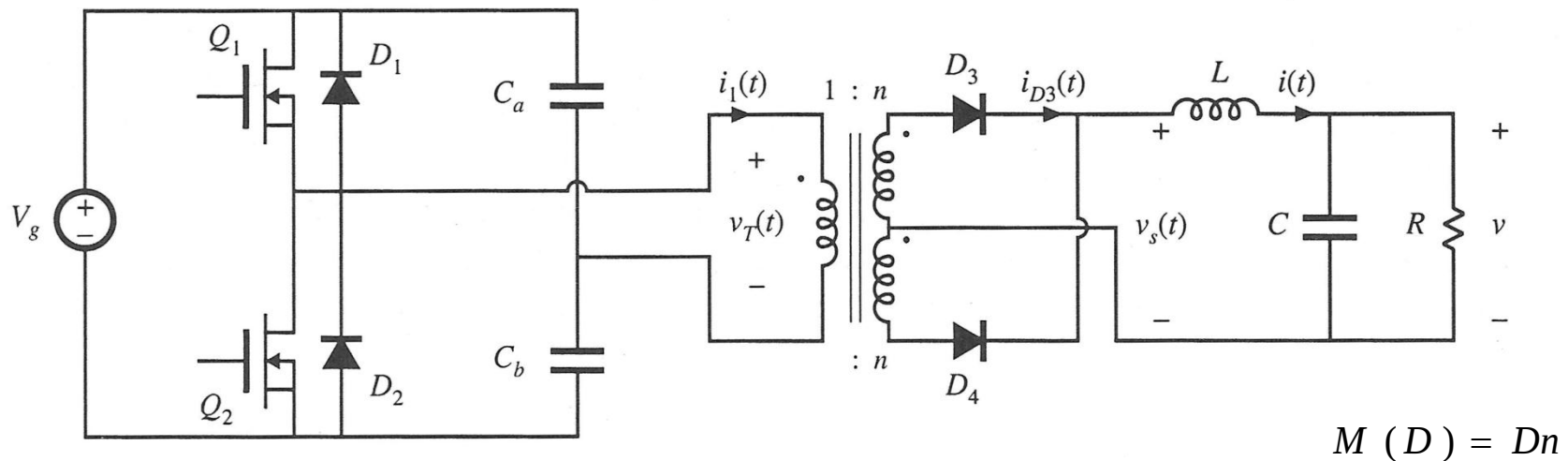
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Half Bridge Converter

- Advantage: Transistors have to withstand V_g only
- Disadvantage: floating gate driver

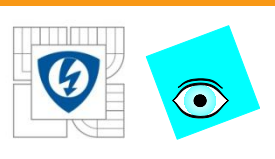


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

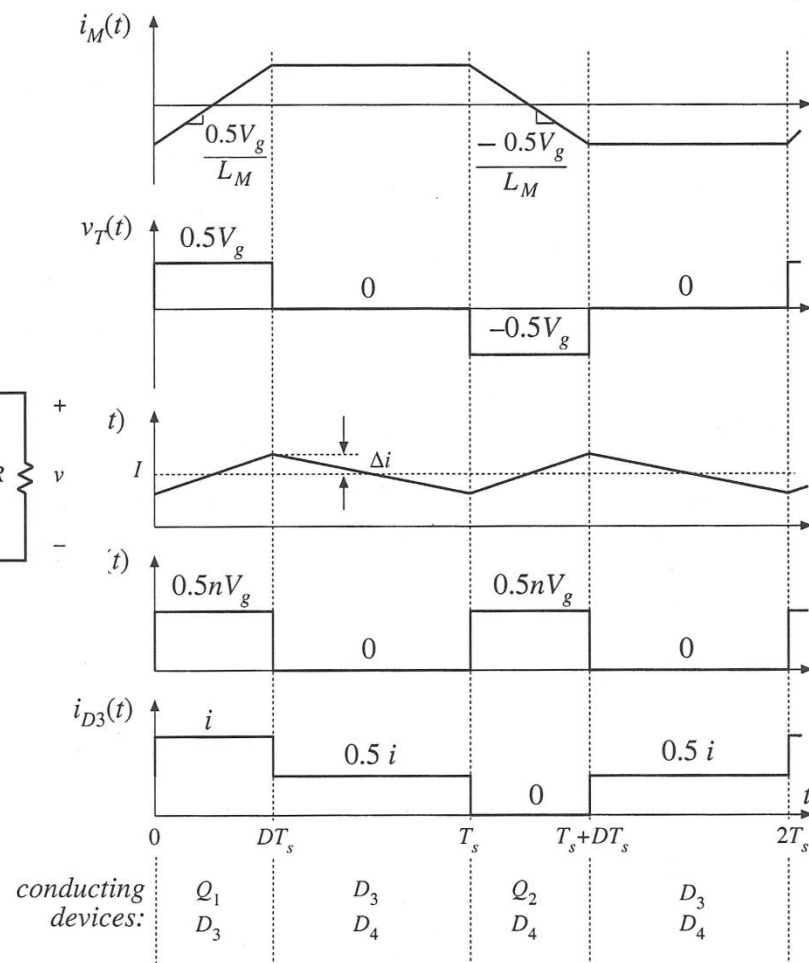
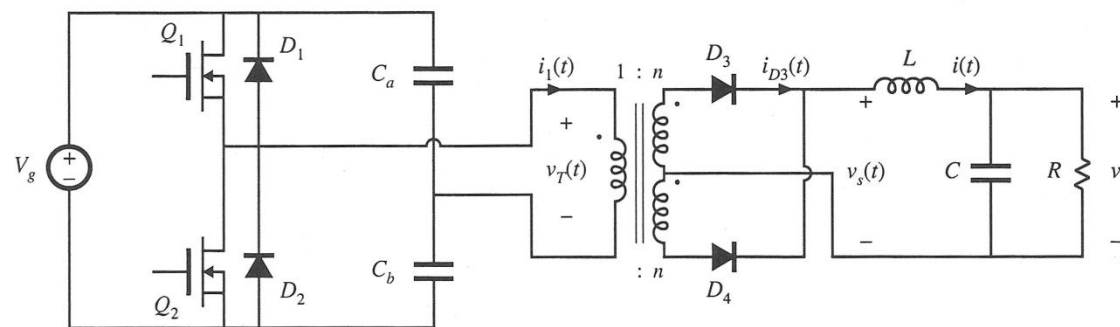
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Half Bridge Converter

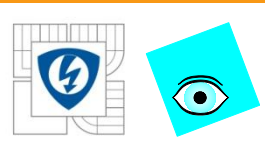


Source: R. W. Erickson, D. Maksimović: Fundamentals of Power Electronics

31.5-1. 6. 2012

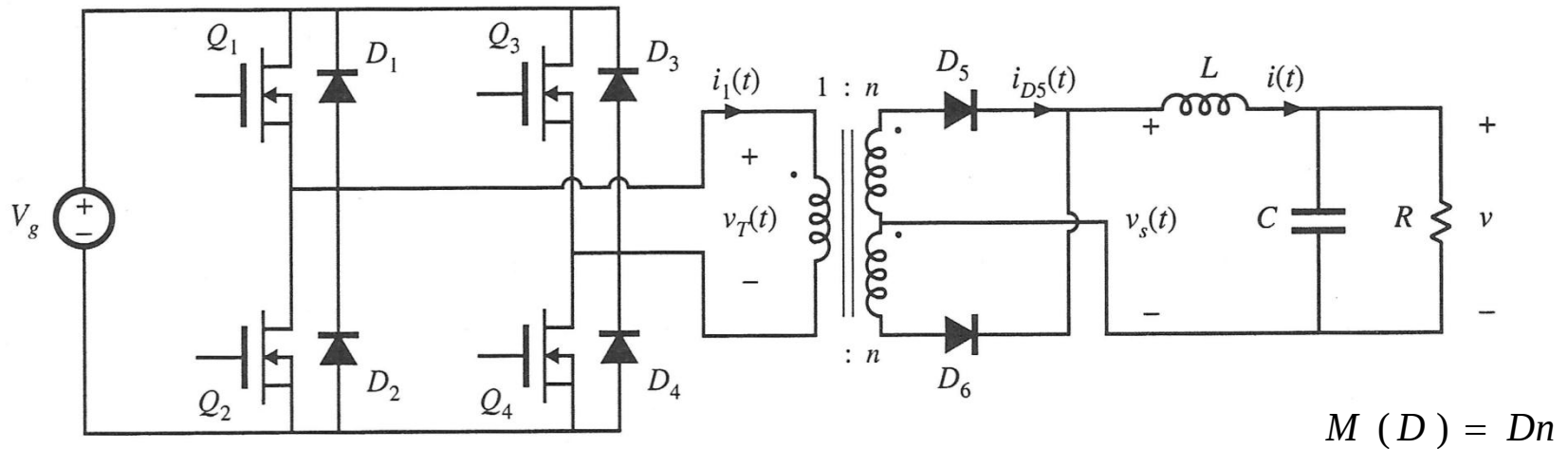
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ





Full Bridge Converter

- Advantage: More output power than half bridge

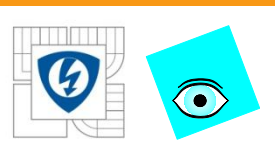


Source: R. W. Erickson, D. Maksimović: *Fundamentals of Power Electronics*

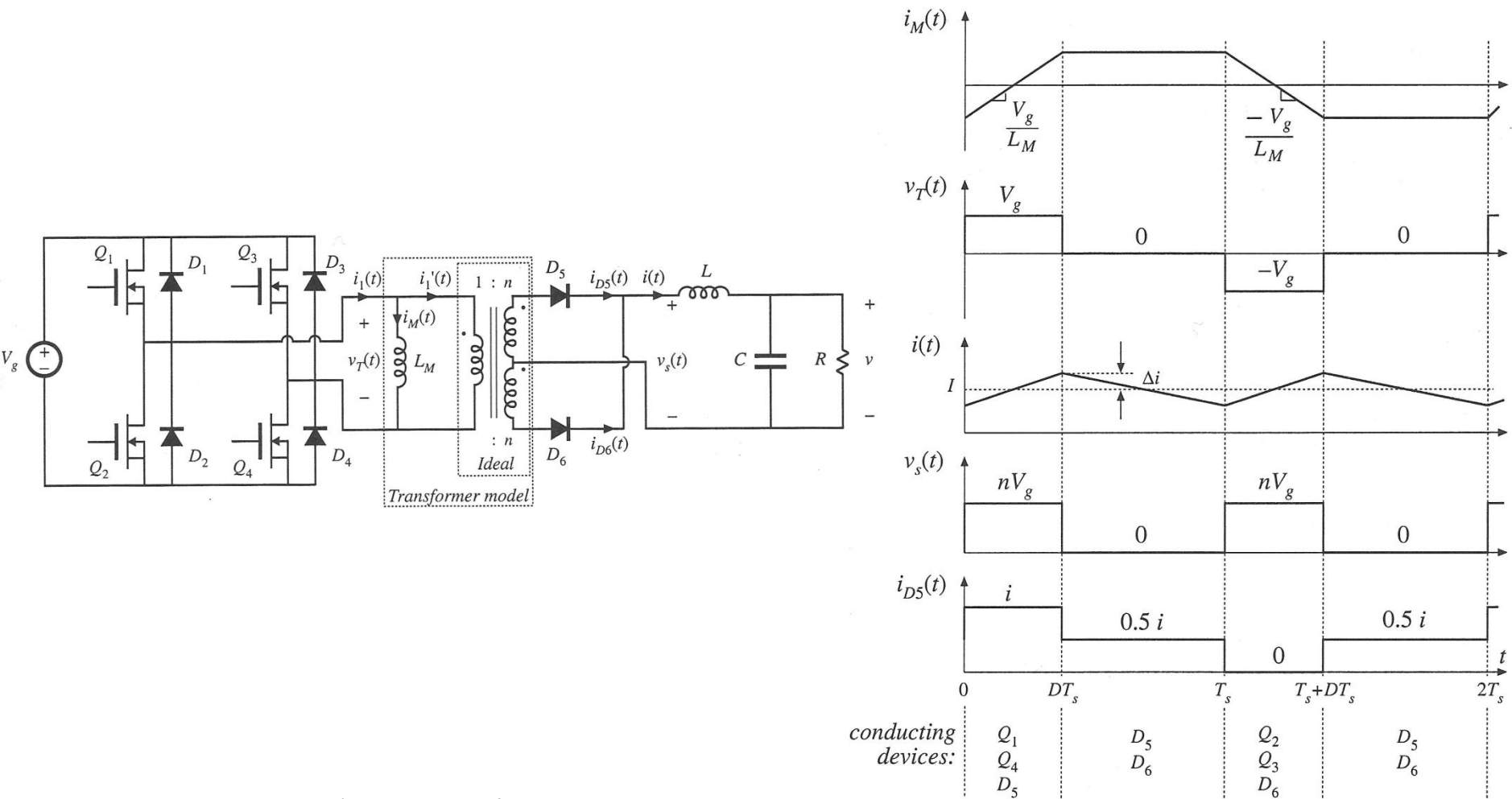
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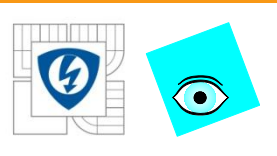




Full Bridge Converter

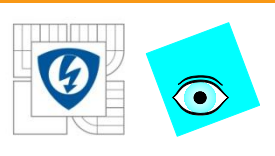


Source: R. W. Erickson, D. Maksimović: Fundamentals of Power Electronics



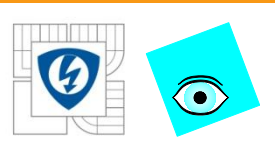
How to select right topology?

- To select right topology we need to consider:
 - Do we need isolation?
 - Input voltage / output voltage ration
 - Output power
 - Cost



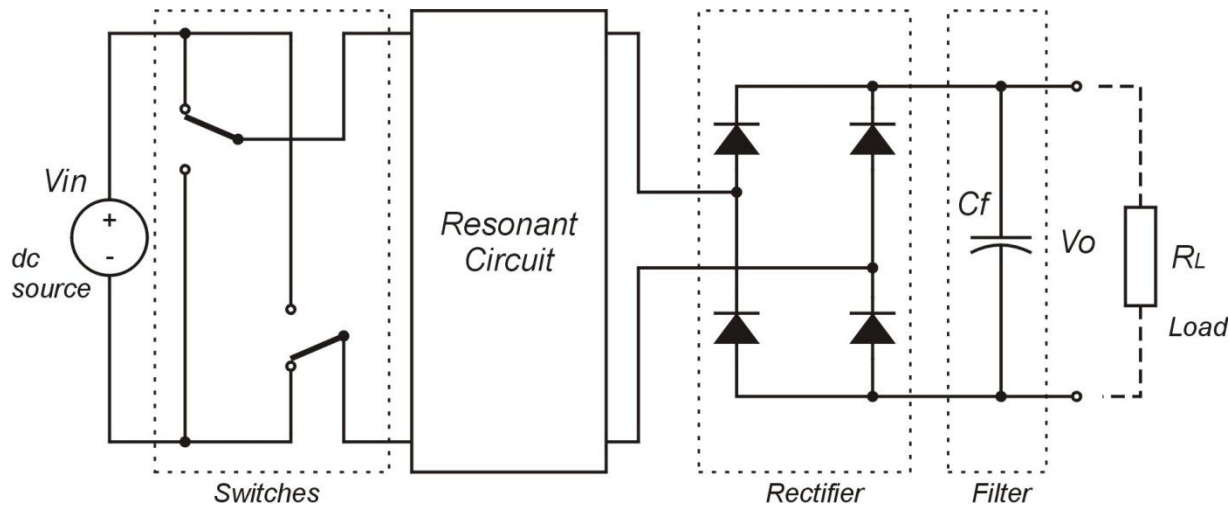
Agenda

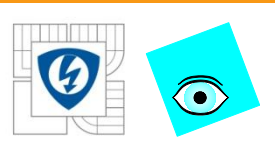
- Linear Regulator
- Non-Isolated SMPS
- Isolated SMPS
- **Resonant SMPS**
 - Series Converter
 - Parallel Converter
 - LLC Converter
- Digital Control of SMPS
- Hands on (Step down Converter)



Resonant Converter Introduction

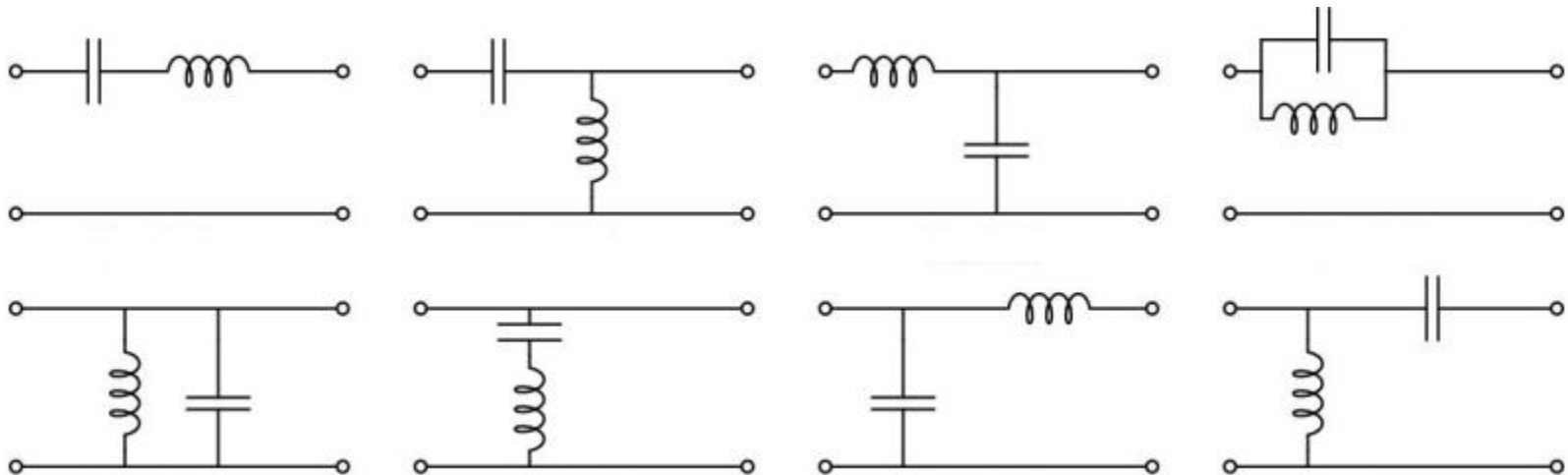
- The resonant converter employs **resonant circuit** between semiconductor switches and rectifier
- The **resonant circuit** consist of at least one capacitor and inductor



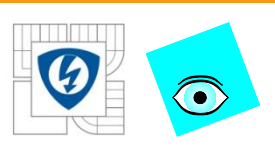


Resonant Converters

- There are many variants, how to implement resonant circuit (two and three components)
- This presentation focuses on widely used combinations:
 - Series resonant converter
 - Parallel resonant converter
 - LLC Resonant converter

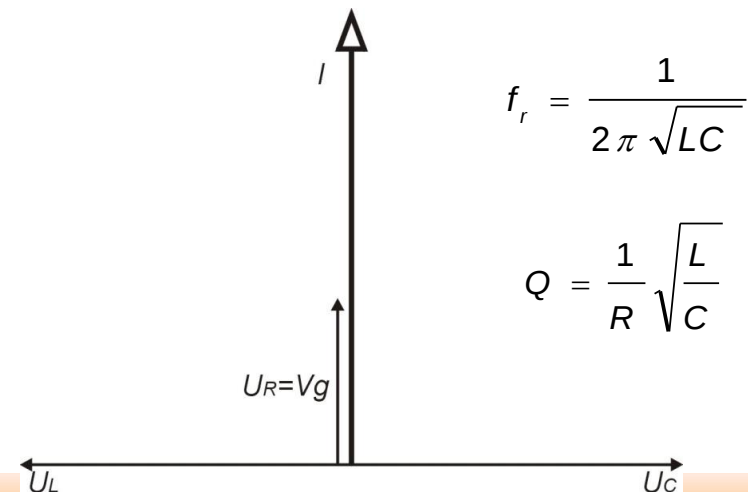
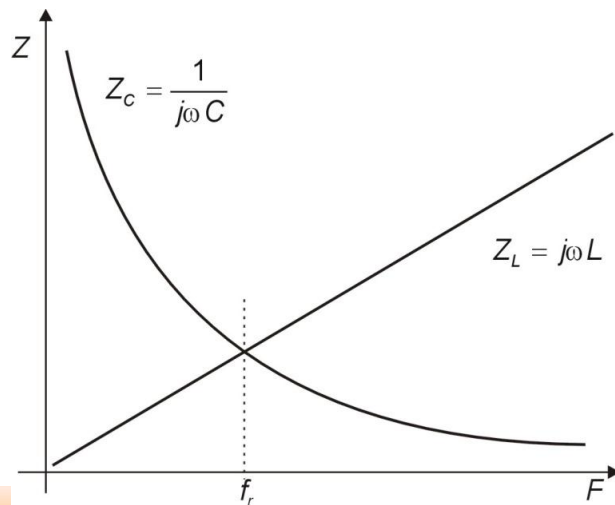


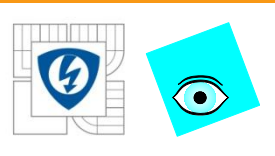
All possibilities for two components resonant circuit



Resonant Converter Introduction

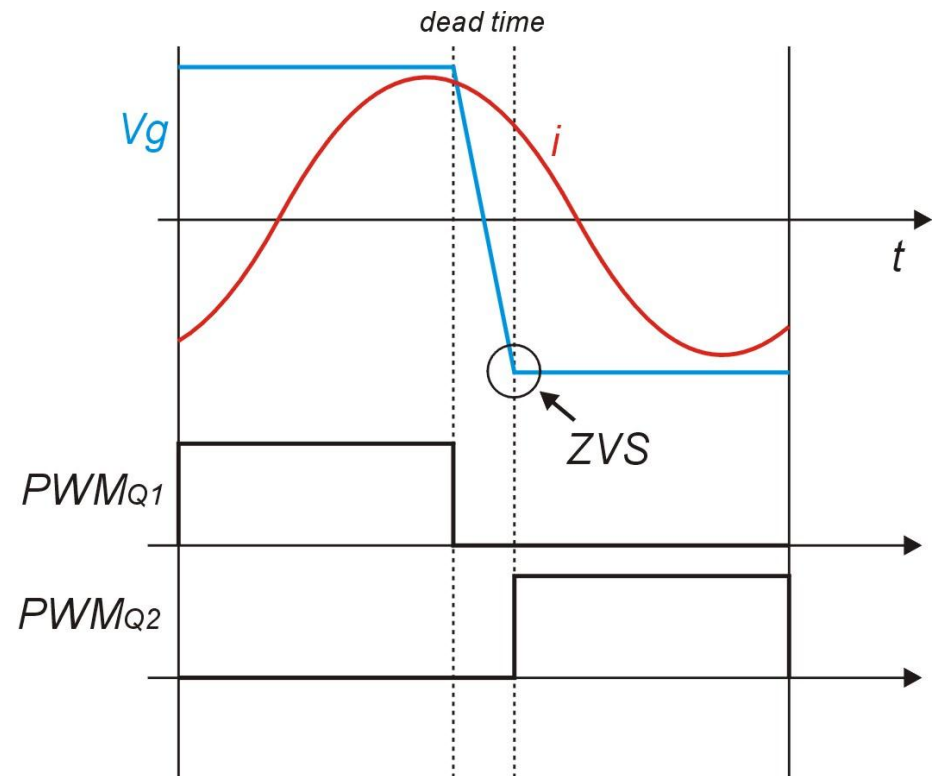
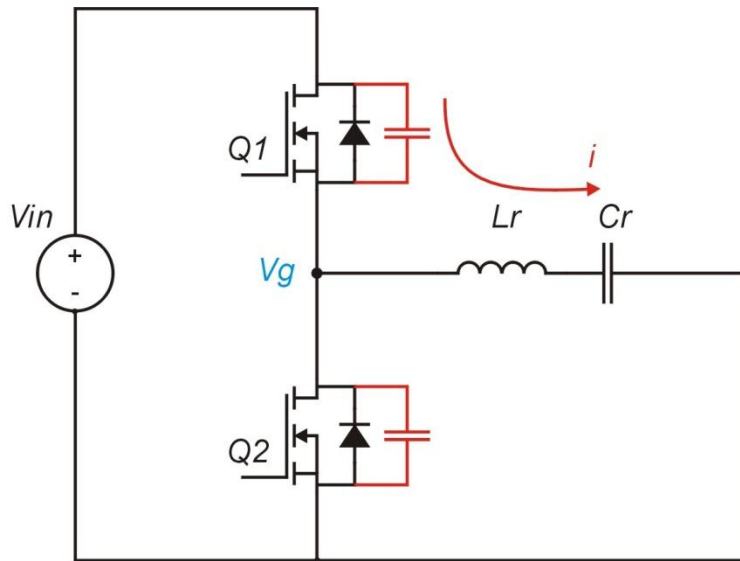
- Series LC (RLC) circuit features at resonant frequency f_r
 - The resonant tank **impedance is frequency dependent**
 - The resonant tank has minimal impedance
 - There is zero voltage drop on resonant tank (ideally)
 - **The voltage drop on L and C components is Q – times (Q - quality factor) higher than voltage on resonant tank**

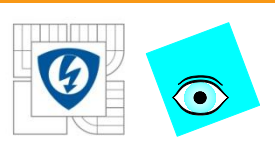




Resonant Converter Introduction

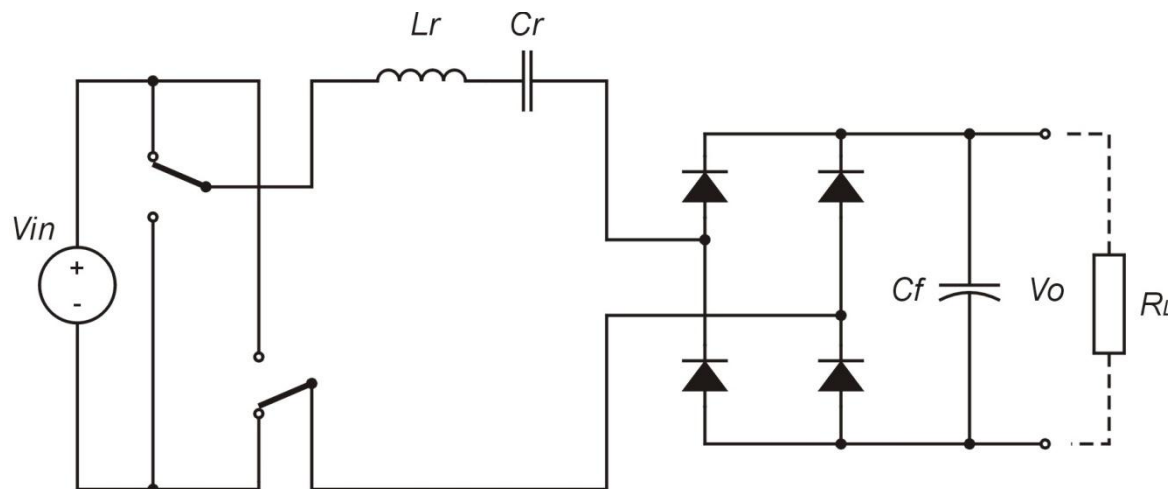
- Zero Voltage Switching (ZVS) of MOSFET transistor
 - The MOSFET transistor is switch on at zero drain-source voltage
 - There are no turn on losses

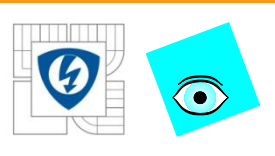




Resonant Converter Introduction

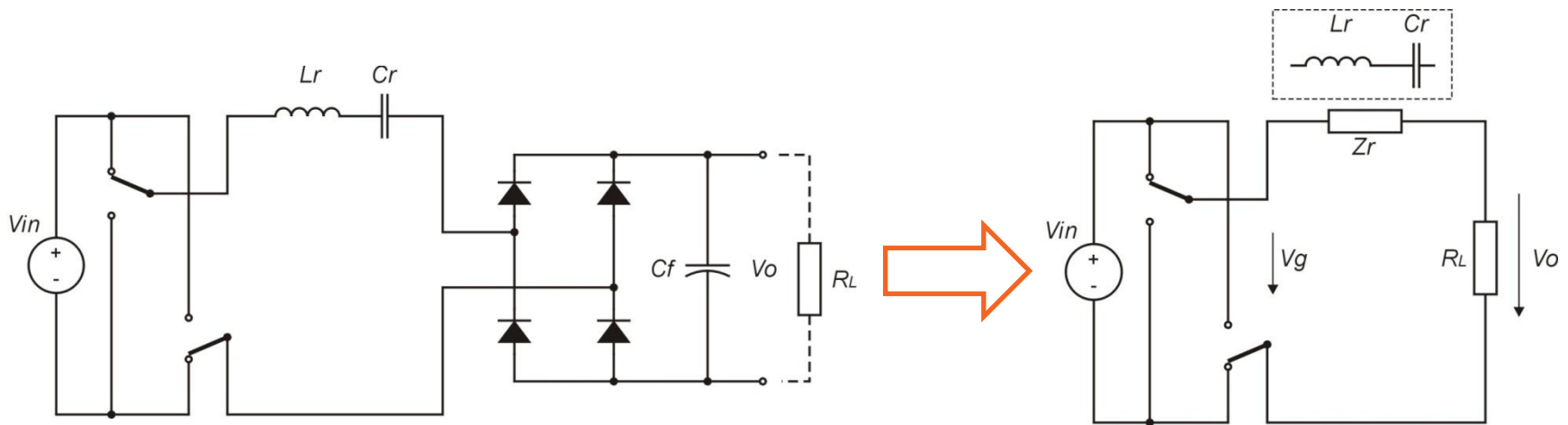
- Series Resonant Converter
 - The resonant tank is connected in series with the load R_L





Resonant Converter Introduction

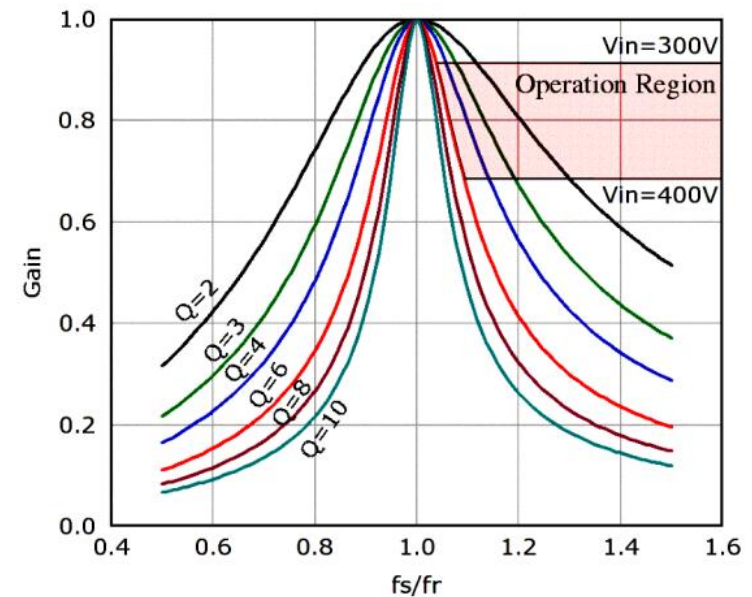
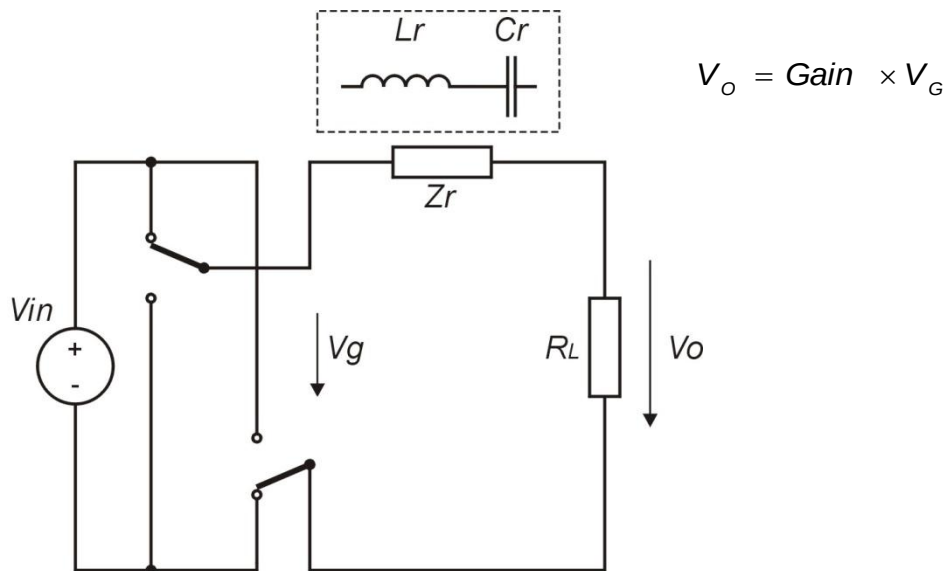
- Series Resonant Converter
 - The resonant tank is connected in series with the load R_L
 - The resonant tank creates voltage divider together with the load

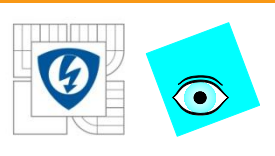


Resonant Converter Introduction

- Series Resonant Converter

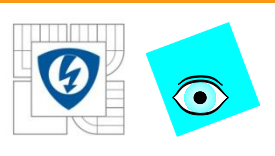
- The resonant tank creates voltage divider together with the load
- The resonant tank impedance is frequency dependent





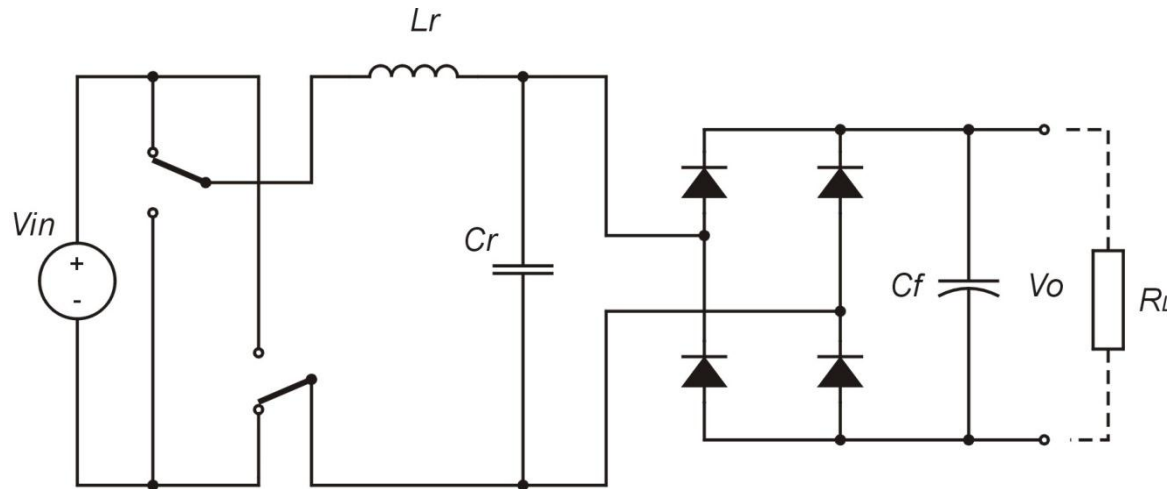
Resonant Converter Introduction

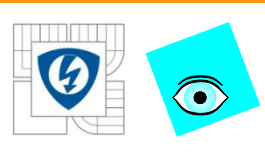
- Series Resonant Converter (SRC) - Summary
 - The SRC can run at ZVS over the resonant frequency
 - At light loads it is difficult to control output voltage
 - High conduction losses at high input voltage and light loads



Resonant Converter Introduction

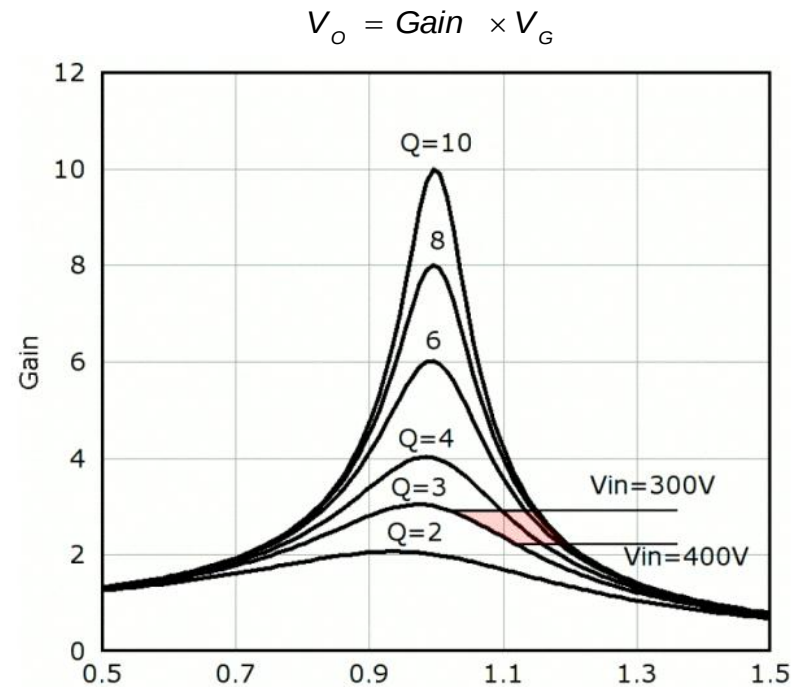
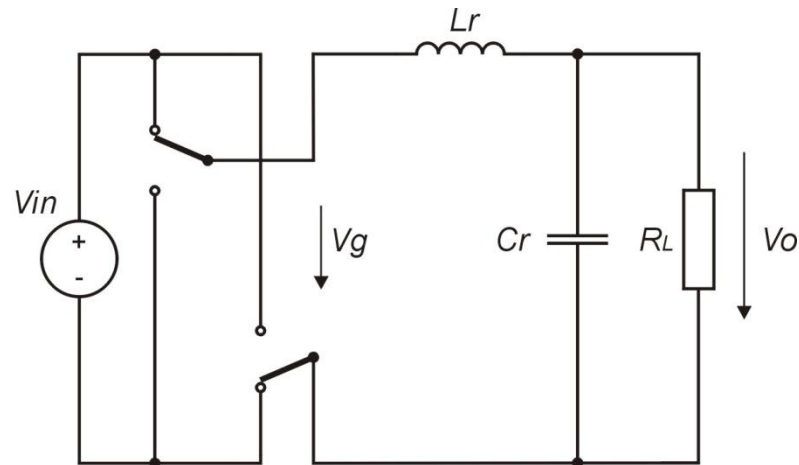
- Parallel Resonant Converter
 - The load R_L is connected in parallel to resonant circuit

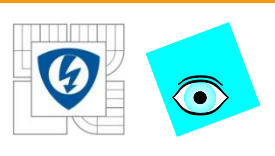




Resonant Converter Introduction

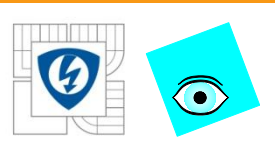
- Parallel Resonant Converter





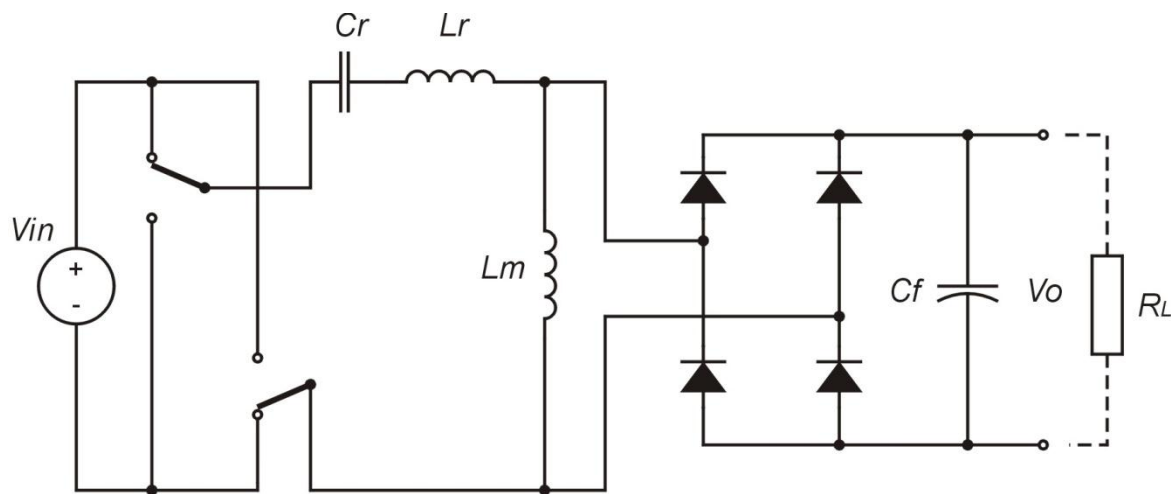
Resonant Converter Introduction

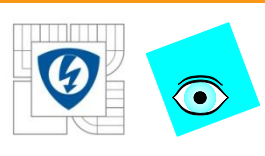
- Parallel Resonant Converter (PRC) - Summary
 - The PRC can also run at ZVS over the resonant frequency
 - The PRC can work at no load condition
 - High conduction losses at high input voltage and light loads



Resonant Converter Introduction

- LLC resonant Converter
 - Additional inductance is employed in resonant circuit
 - The load R_L is connected in parallel to this inductance

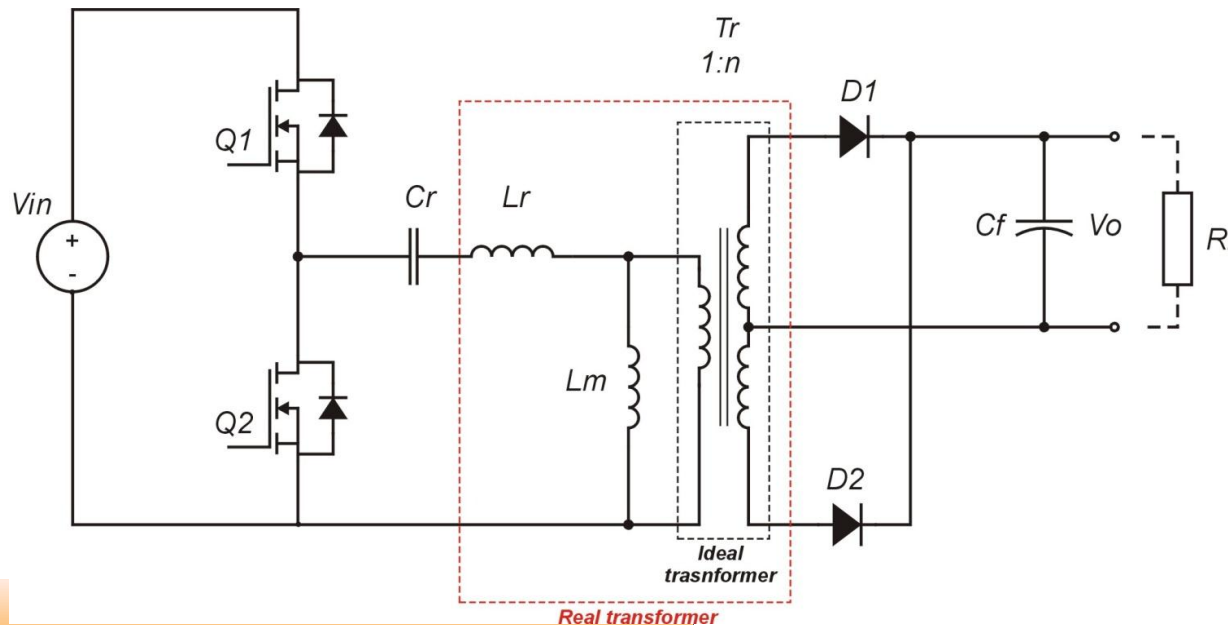


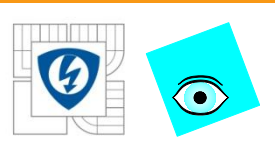


Resonant Converter Introduction

- LLC resonant Converter

- When transformer used in LLC converter, the magnetizing inductance and leakage inductance can be used in resonant circuit instead of external separate inductances
- This is one of the advantages of LLC resonant converter

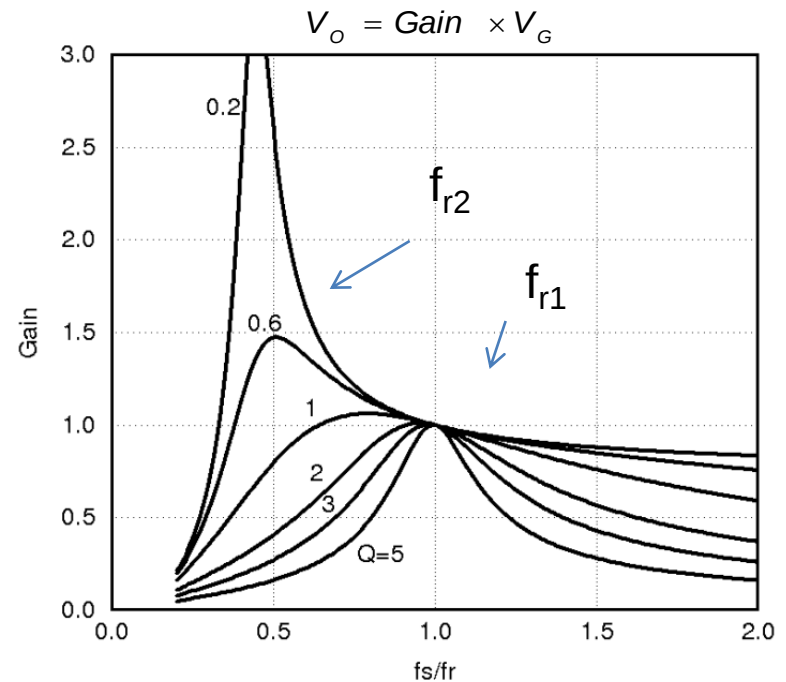
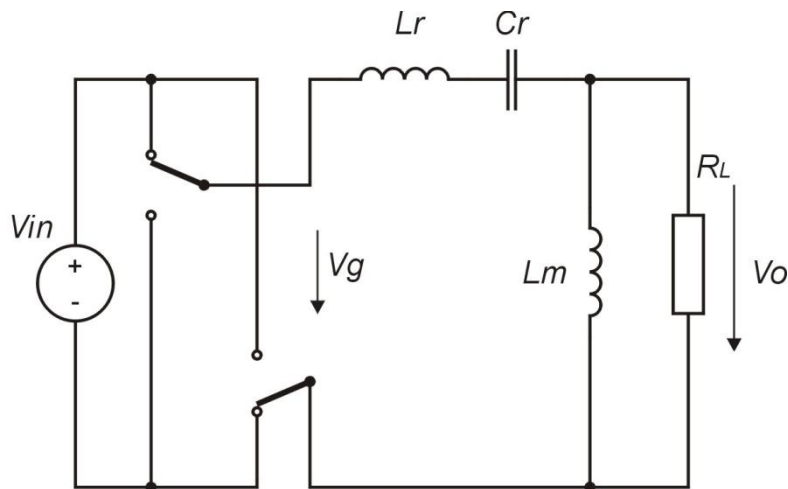




Resonant Converter Introduction

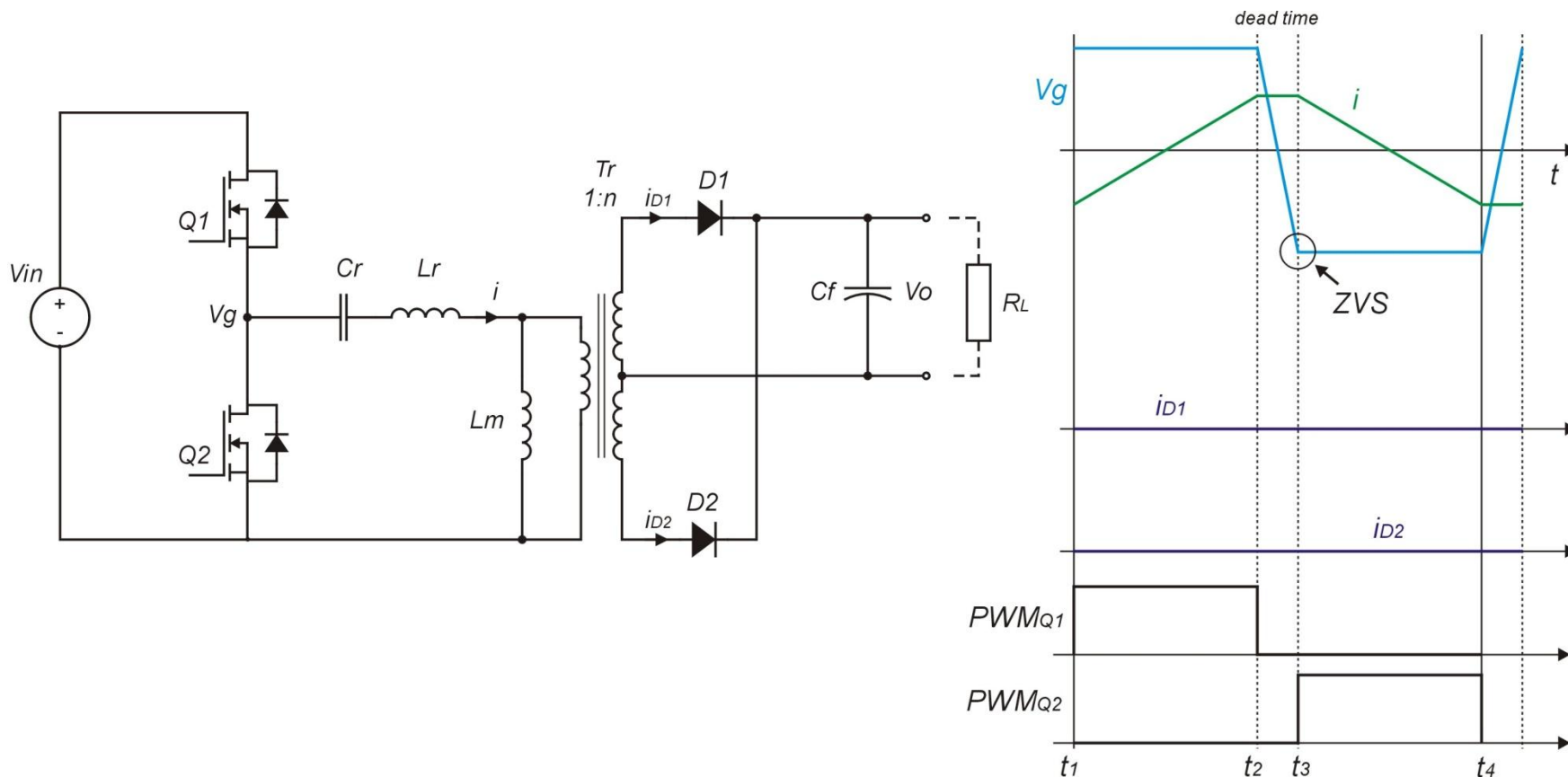
- LLC Resonant Converter

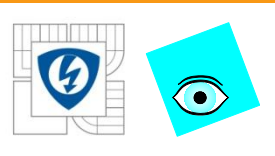
- There are two resonant frequencies: first one for L_r and C_r and second one for $(L_r + L_m)$ and C_r



Resonant Converter Introduction

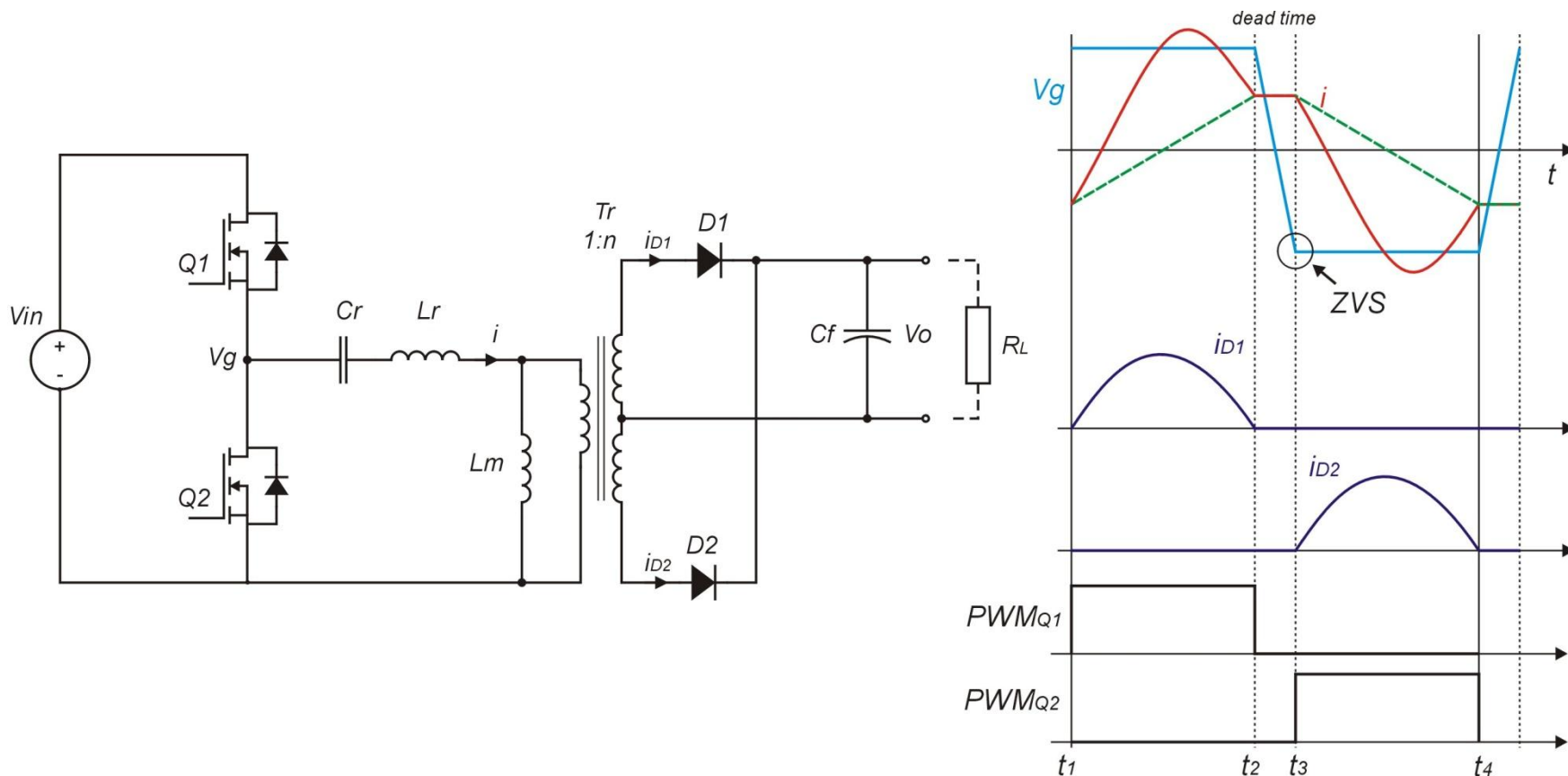
- LLC Resonant Converter – Operation at no Load

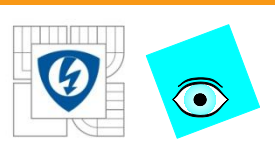




Resonant Converter Introduction

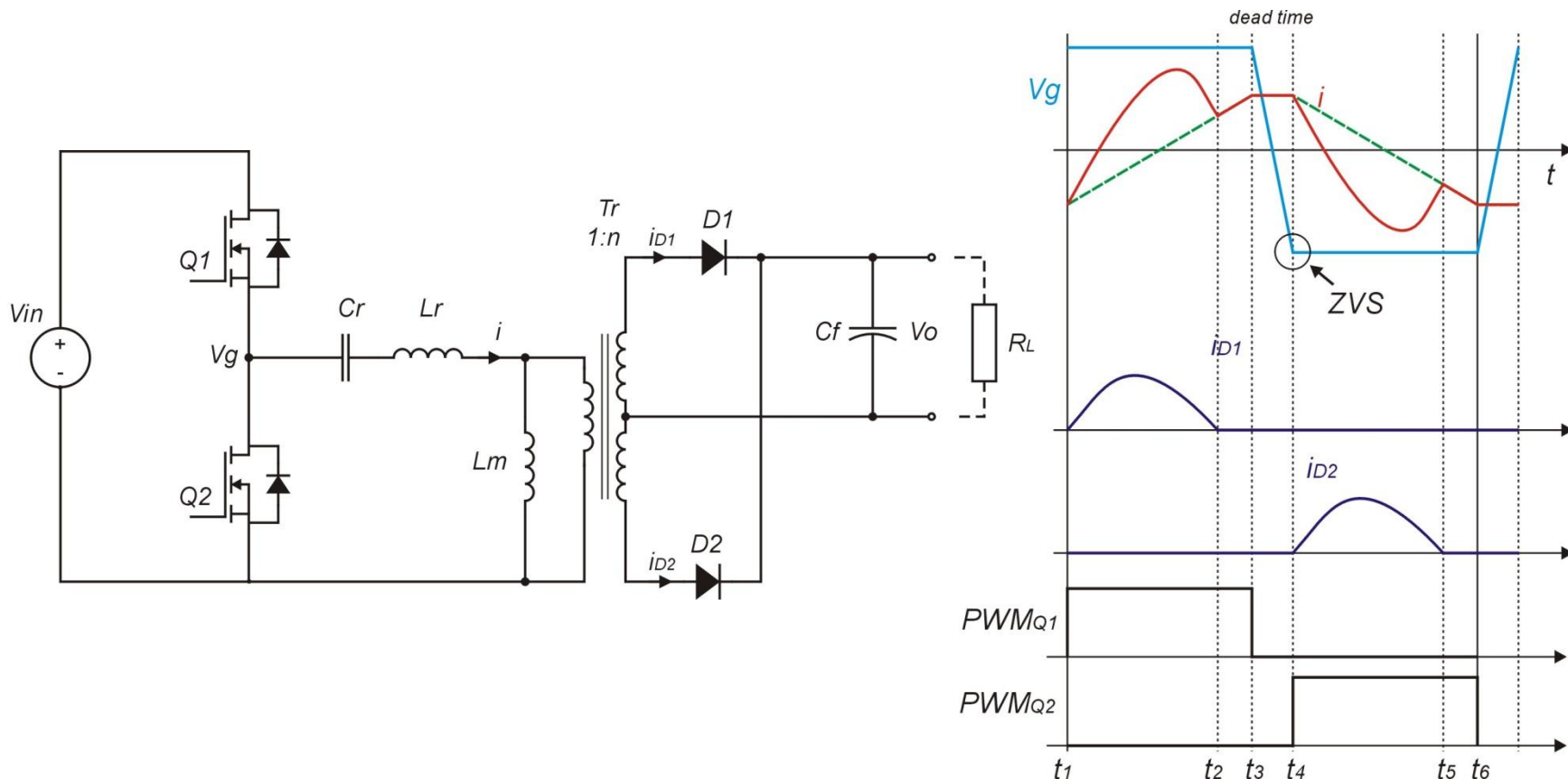
- LLC Resonant Converter – Operation at Resonance





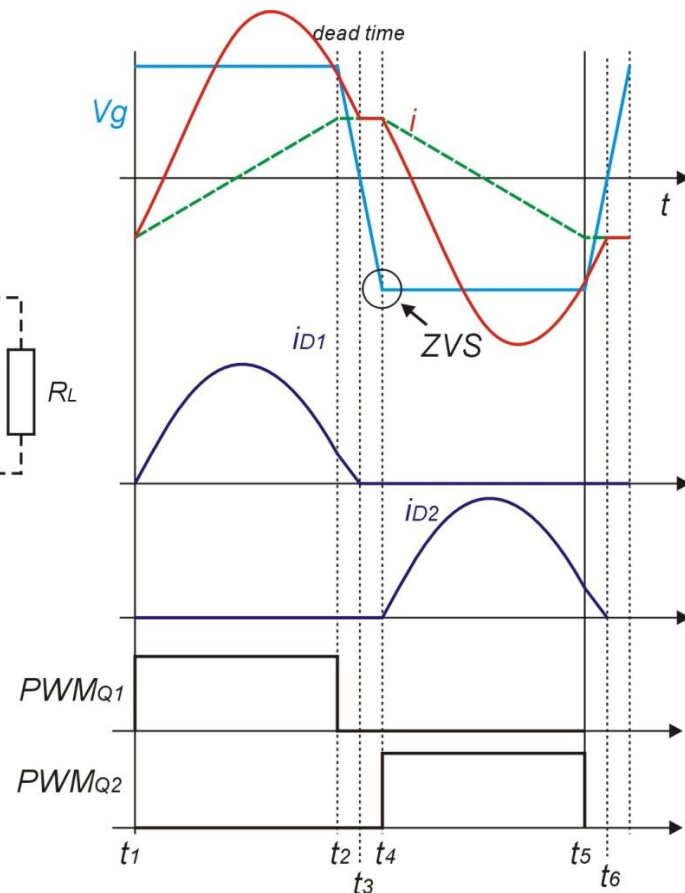
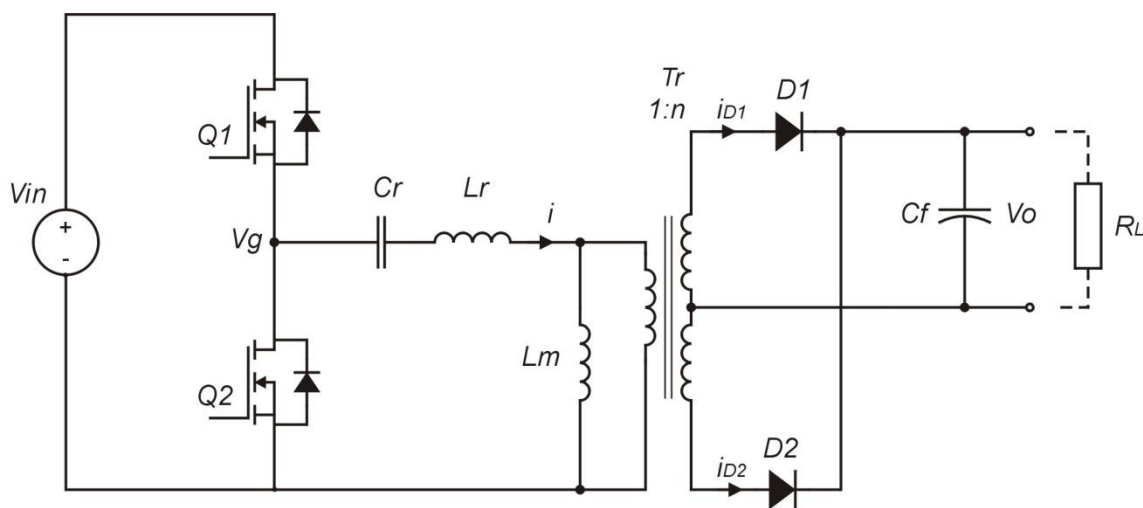
Resonant Converter Introduction

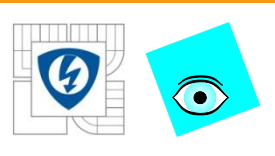
- LLC Resonant Converter – Operation below Resonance



Resonant Converter Introduction

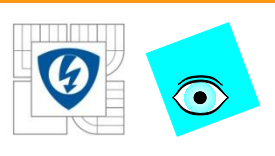
- LLC Resonant Converter – Operation above Resonance





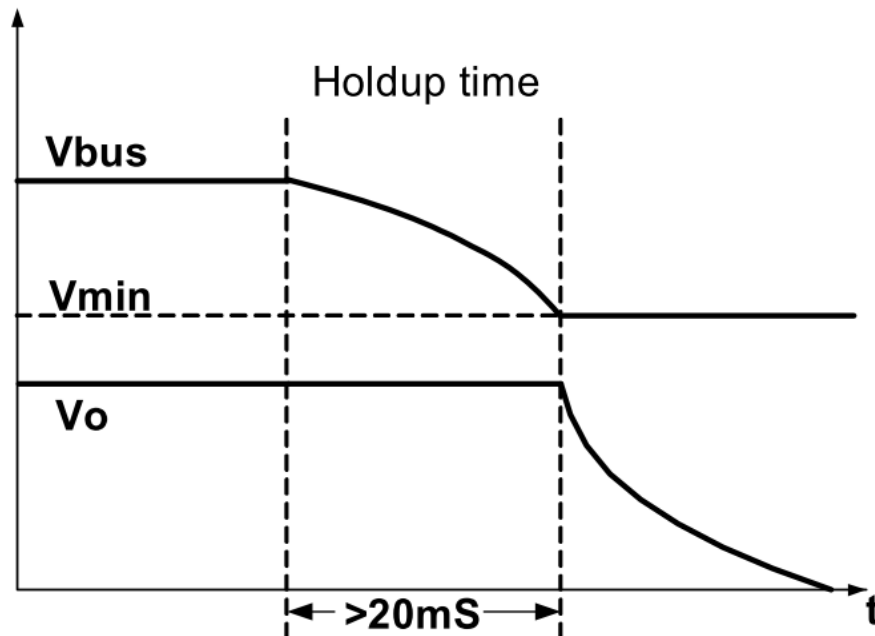
Resonant Converter Introduction

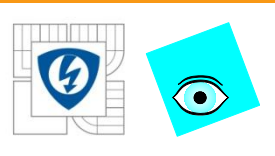
- LLC Resonant Converter - Summary
 - The LLC resonant converter can run at ZVS in whole range of the operating frequency (above even below resonant frequency)
 - The LLC resonant converter can work at no load condition. The turn off current can be controlled by L_m inductor
 - The LLC resonant converter works at resonant frequency at nominal input voltage
 - The LLC resonant converter can operate over wide range of operating input voltage



Resonant Converter Introduction

- Operation at wide input range
 - There is a requirement, that power supply must delivery output power during one whole period, if there is mains line drop out2





Resonant Converter Introduction

- Operation at wide input range – PWM modulated Converters
 - The PWM modulated converters are not able to increase gain by changing duty cycle. Therefore the $V_{BUS} - V_{min}$ has to be small (20-30V).
 - The whole energy has to be stored in DC bus capacitor
 - Example of DC bus capacitor calculation

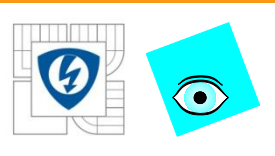
$$P_{out} = 500W$$

$$V_{BUS} = 400V$$

$$V_{min} = 370V$$

$$f_{min} = 45Hz$$

$$C \geq \frac{2P}{f_{min} (V_{BUS} - V_{min})} = 962 \mu F$$



Resonant Converter Introduction

- Operation at wide input range – Resonant Converters
 - Some resonant converters can increase gain over 1 by changing switching frequency. Therefore the $V_{BUS} - V_{min}$ can be much higher than for PWM modulated converters.
 - Example of DC bus capacitor calculation

$$P_{out} = 500W$$

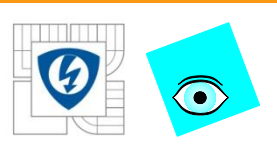
$$V_{BUS} = 400V$$

$$V_{min} = 200V$$

$$f_{min} = 45Hz$$

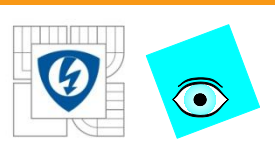
$$C \geq \frac{2P}{f_{min} (V_{BUS} - V_{min})} = 185 \mu F$$

- The DC Bus capacitor can be significantly smaller **185 μF versus 962 μF !!!**

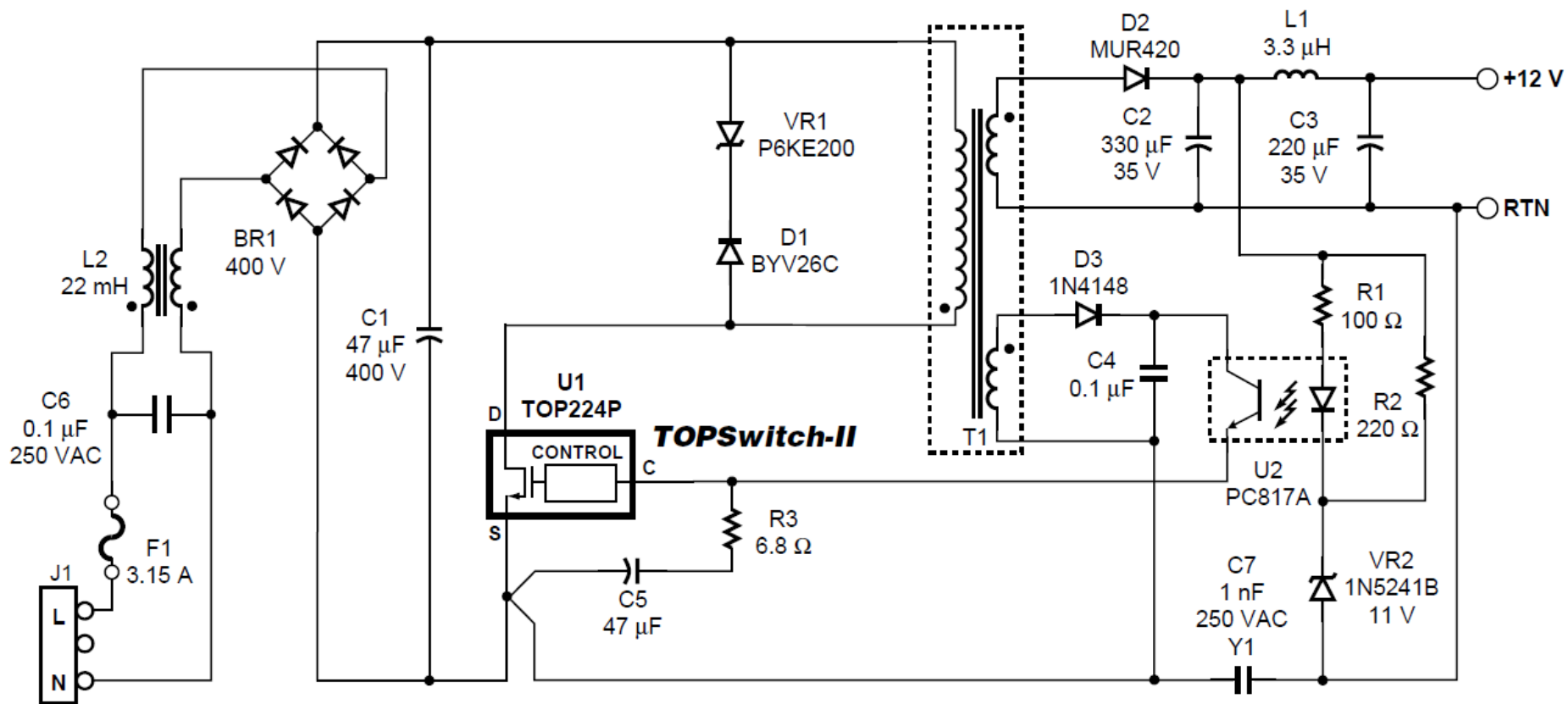


Agenda

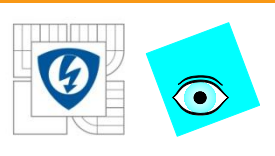
- Linear Regulator
- Non-Isolated SMPS
- Isolated SMPS
- Resonant SMPS
- Digital Control of SMPS
 - Advantages of Digital Control
 - MCU Requirements/Example of suitable MCU's
 - Key MCU Peripherals
 - Example of SMPS Application
- Hands on (Step down Converter)



Analog Control of SMPS



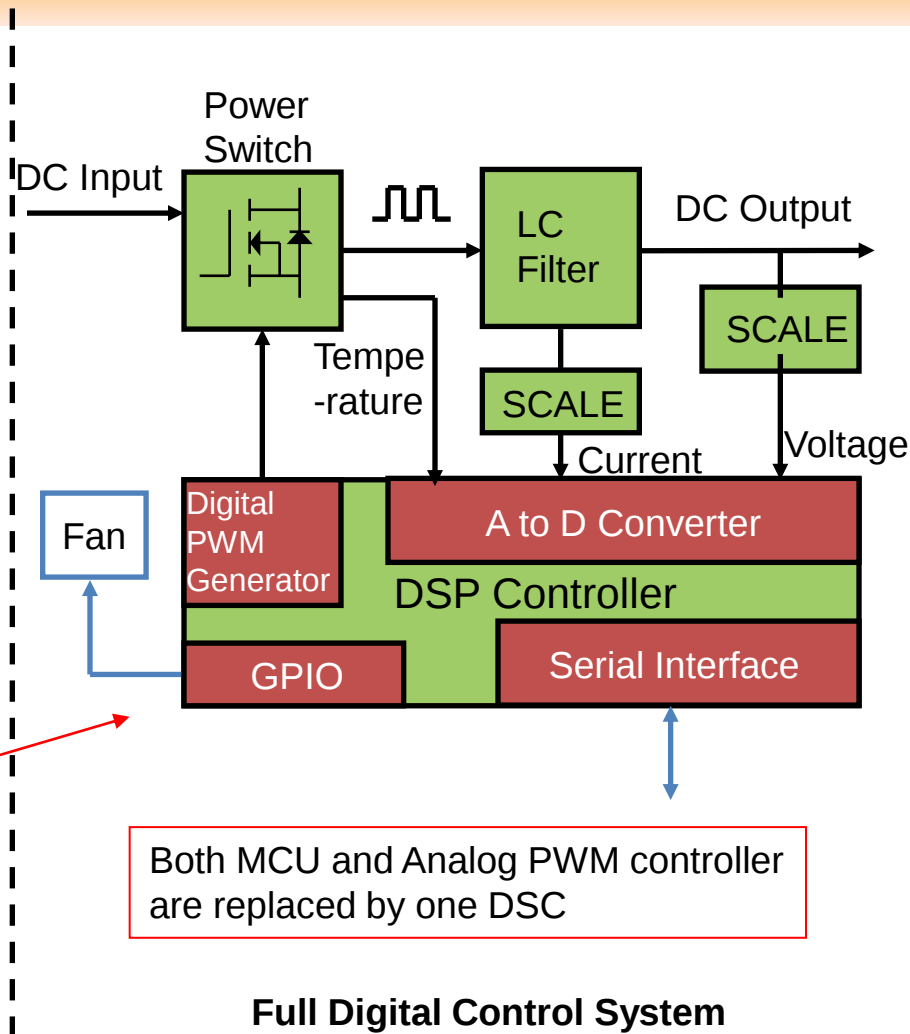
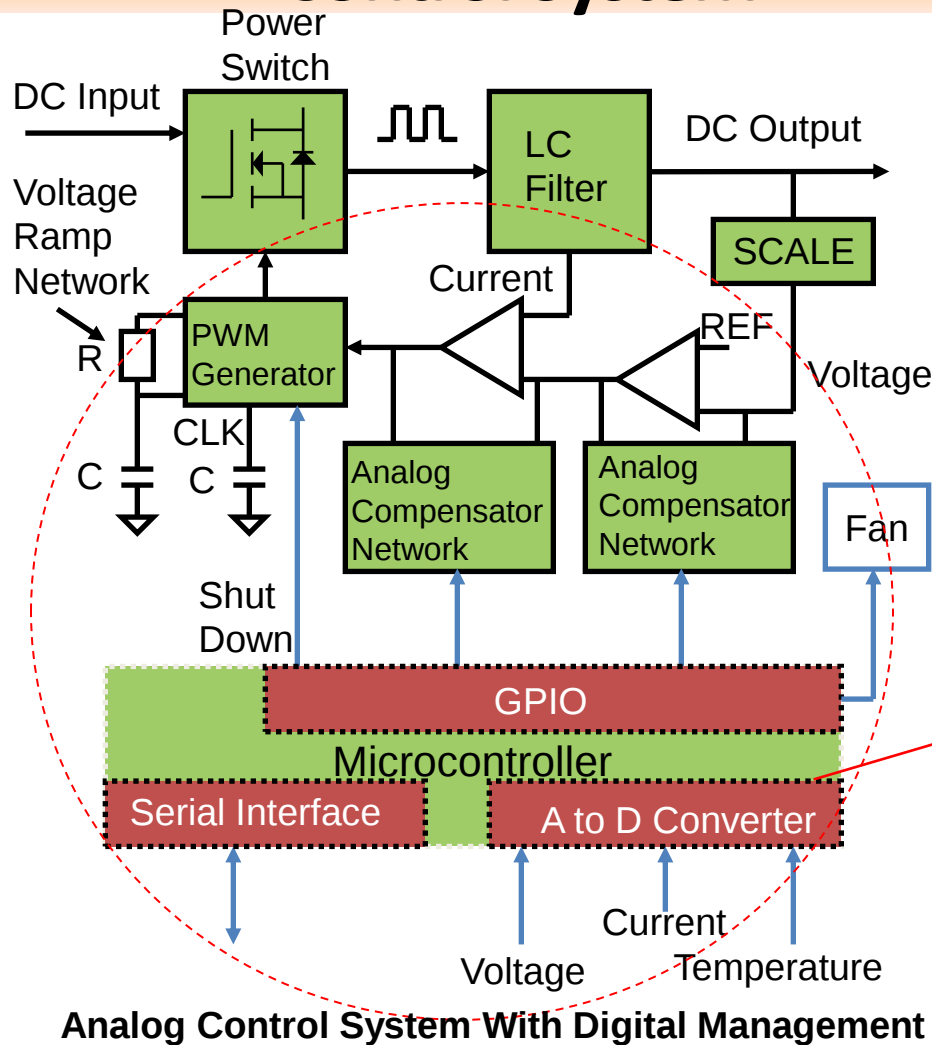
Analog Control of Flyback Converter (Power Integration)

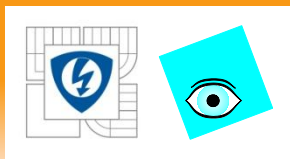


Where Is Digital Power Conversion Applied?

- “Digital power Conversion” is a power system that is controlled by digital circuits, in much the same way as would be with analog circuits, to monitor, supervise, communicate and control looping. A fully digitally controlled power system includes both digital control and digital power management.
- Digital Control
 - The control feedback or feed-forward loop, which is controlled by the digital circuit or programmable controller, regulates the output of the power system by driving the power switch duty cycle using pulse width modulation techniques.
 - The control circuits combine A/D conversion, Pulse Width Modulation, and Communication interfaces, operating entirely or mostly in digital mode.
- Digital Power Management
 - A Digital circuit or **programmable controller** provides the functions of configuration, tracking, monitoring , protection, supply sequencing, and communication with the environment.

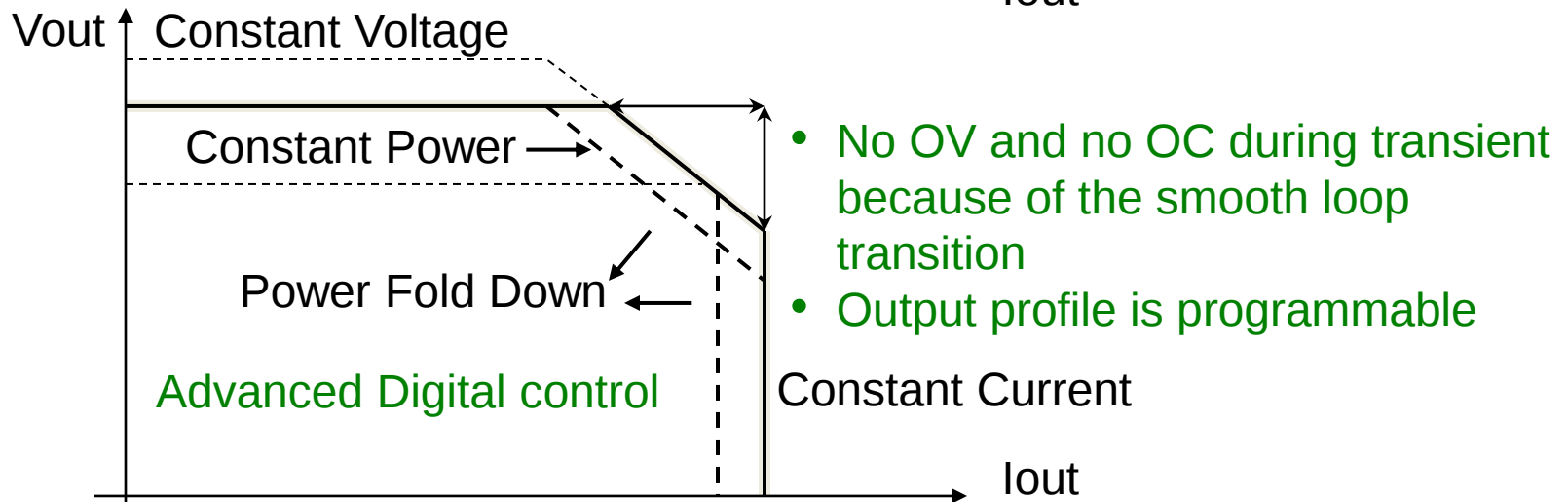
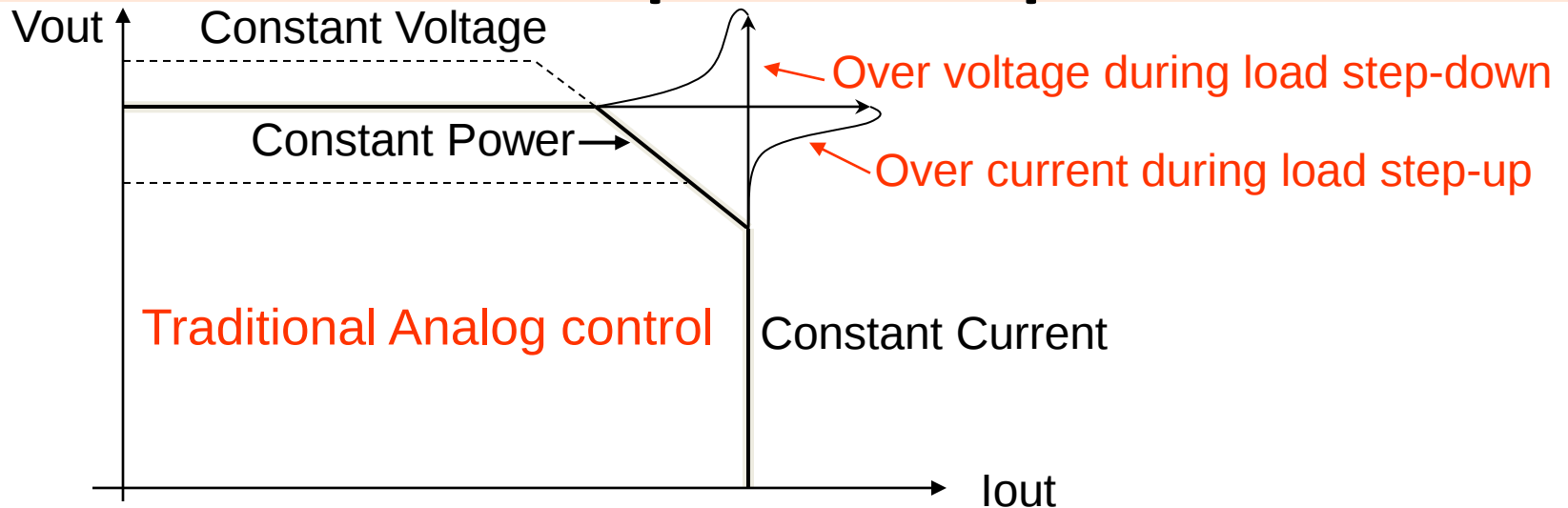
Comparison of Analog and Digital Power Control System

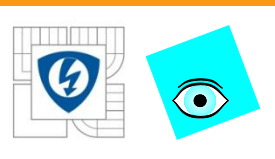




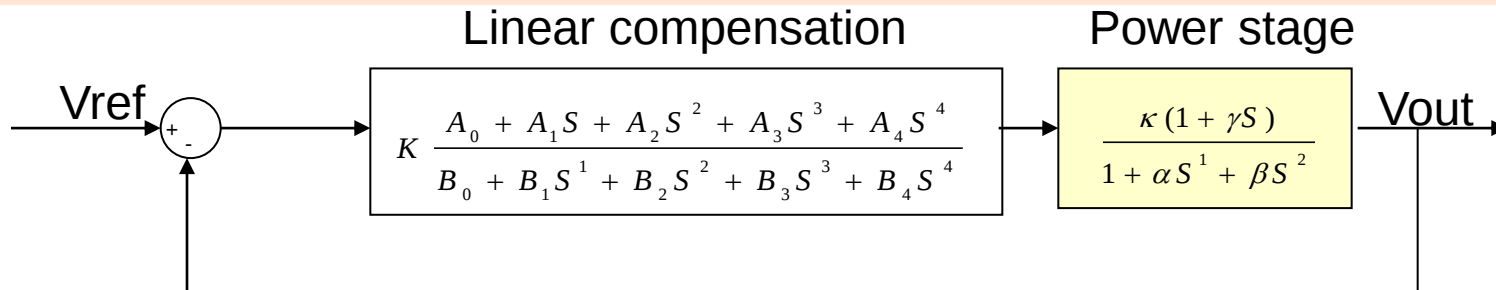
Analog Control vs. Digital Control

- Transient Response Comparison

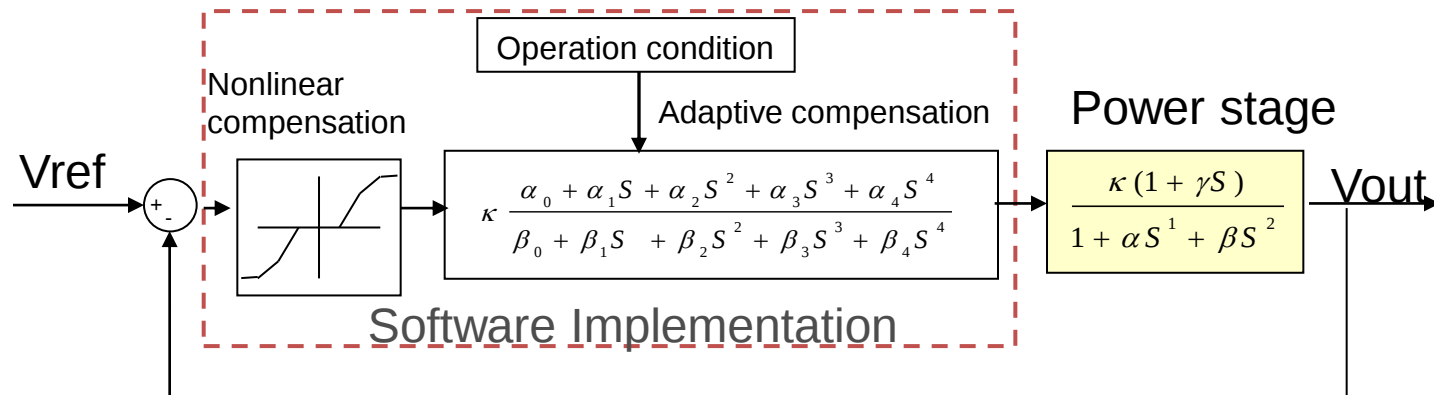




Digital vs. Analog Control Loop



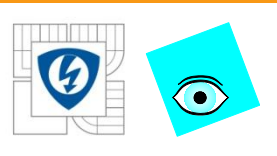
A typical control loop implemented by an analog circuit



A digital control loop implemented by Digital Signal Controller (DSC)

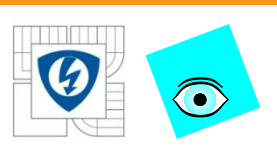
Benefit of digital control:

- 1) Optimize feedback loop to meet application requirements
- 2) Runtime changes to compensation parameters according to operating conditions

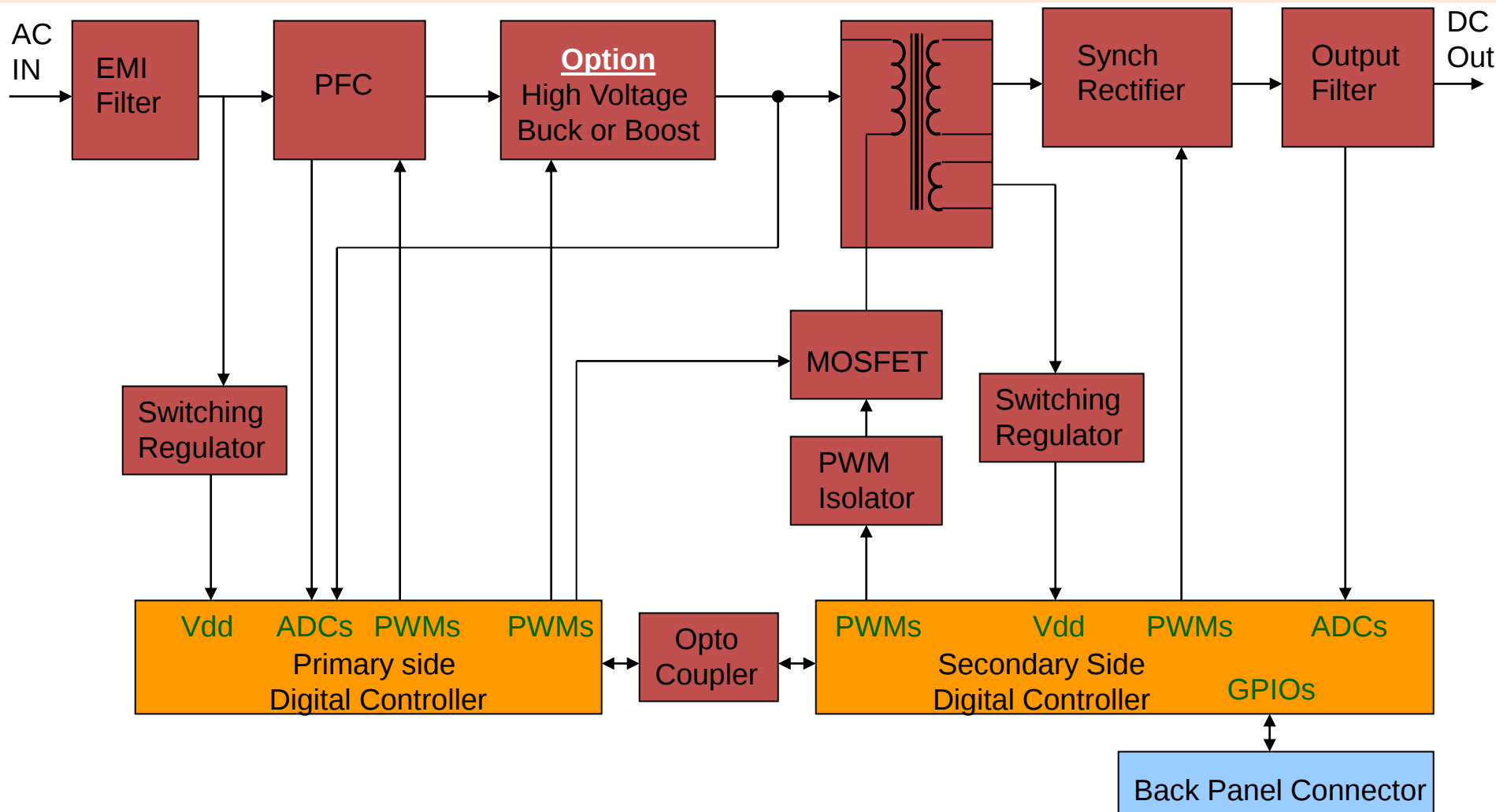


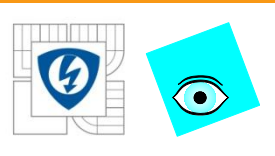
Compare Digital Control To Analog Control

	Analog Control	Digital Control
Control Circuit	Complex, Bulky	Simple, Programmable, Integrated
Flexibility	Bad	Good
Design Continuity	Bad	Good
Sample Mode	Continuous	Digitalization Error
Processing	Continuous	Control Delay



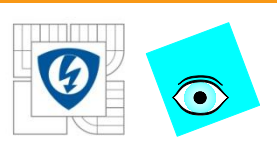
Digital Controlled Power Supply





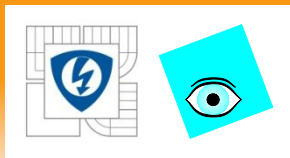
Benefits of Digital Power

- **Free from** the effects of **component tolerance**, parametric drift, aging, etc.
- **Configurable** feedback loop **structure** for specific application requirements
- **Adaptive control** to meet changing operating conditions
- **Flexible** Pulse Width **Waveform-generation** module
- **Programmable relationships** among **PWM** outputs
- **Upgradeable** with new features **without hardware** changes
- **Retainable** operational **data** for diagnostic and record keeping
- **Diverse communications** capabilities
- **Reduced** component count and **cost**
- **Higher** power density due to over all **integration**
- **Shorter R&D cycle**, fewer turns of board prototyping
- **Portable Projects** for faster reuse
- **Defendable firmware**—protects IP and differentiating technology



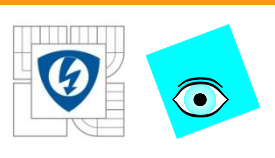
Agenda

- Linear Regulator
- Non-Isolated SMPS
- Isolated SMPS
- Resonant SMPS
- Digital Control of SMPS
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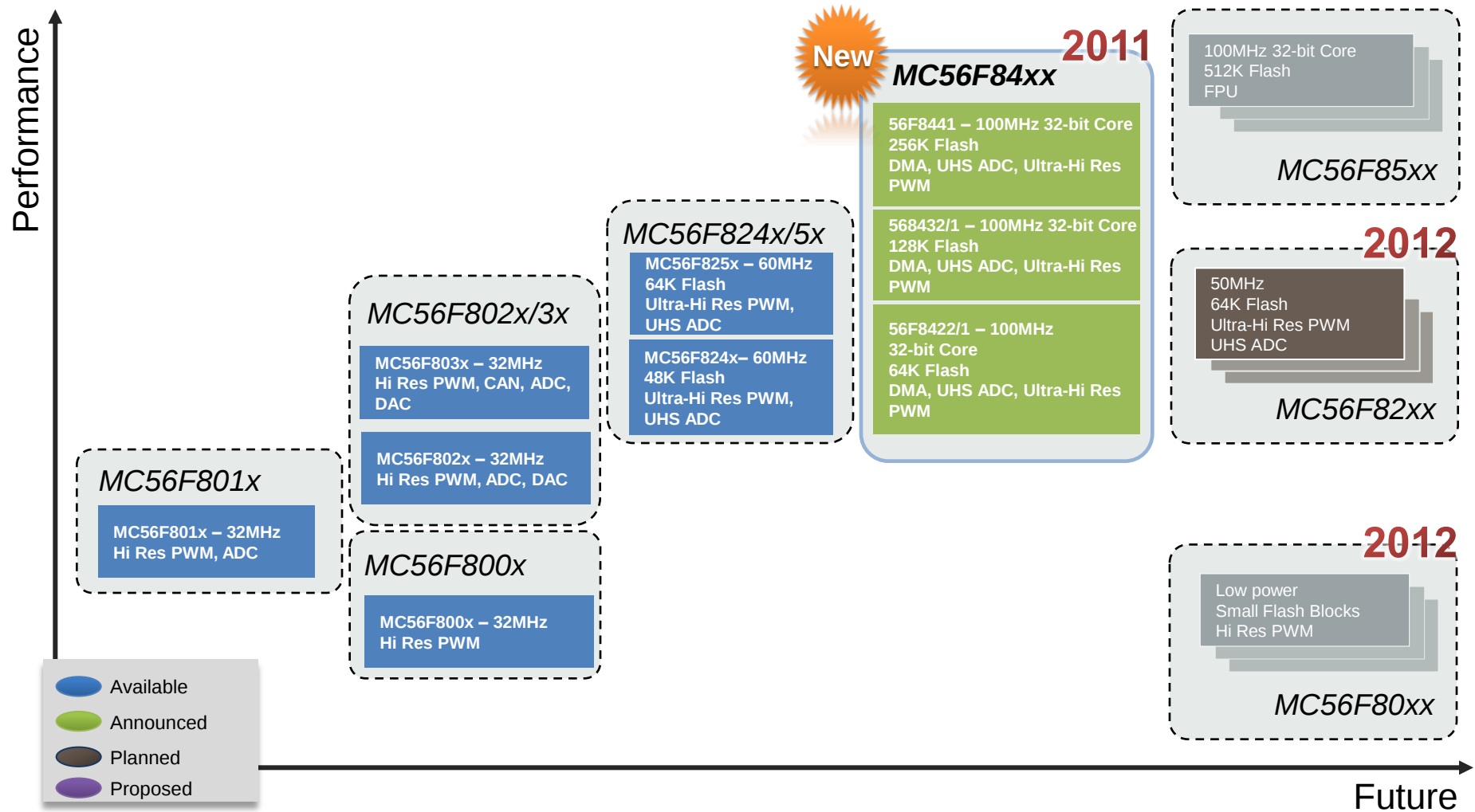


Digital Control of Power Conversion Applications

- General requirements
 - **Powerful Core**
 - The control loop is calculated every 5-20 μs (motor control application 50 – 200 μs)
 - Very **fast A/D Converter** (better than 1 μs conversion, capable of parallel conversion)
 - **PWM module** capable of **high resolution frequency** and **duty cycle** generation
 - The resolution should be comparable to resolution of ADC measurement
 - It means more than 10 bits for frequencies 100 – 400kHz



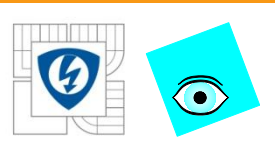
DSC Roadmap



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DSP56800E Version 3 Core Improvement

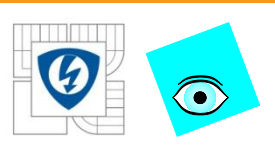
(the differences between V2 core and V3 core)

New Instructions

- 32 x 32 -> 32/64 Multiply and MAC Instructions
 - ✓ IMAC32 - Integer Multiply-Accumulate 32 bits x 32 bits -> 32 bits
 - ✓ IMPY32 - Integer Multiply 32 bits x 32 bits -> 32 bits
 - ✓ IMPY64 - Integer Multiply 32 bits x 32 bits -> 64 bits
 - ✓ IMPY64UU - Unsigned Integer Multiply 32 bits x 32 bits -> 64 bits
 - ✓ MAC32 - Fractional Multiply-Accumulate 32 bits x 32 bits -> 32 bits
 - ✓ MPY32 - Fractional Multiply 32 bits x 32 bits -> 32 bits
 - ✓ MPY64 - Fractional Multiply 32 bits x 32 bits -> 64 bits
- Multi-Bit Clear-Set instruction to improve flexibility of peripheral register handling.

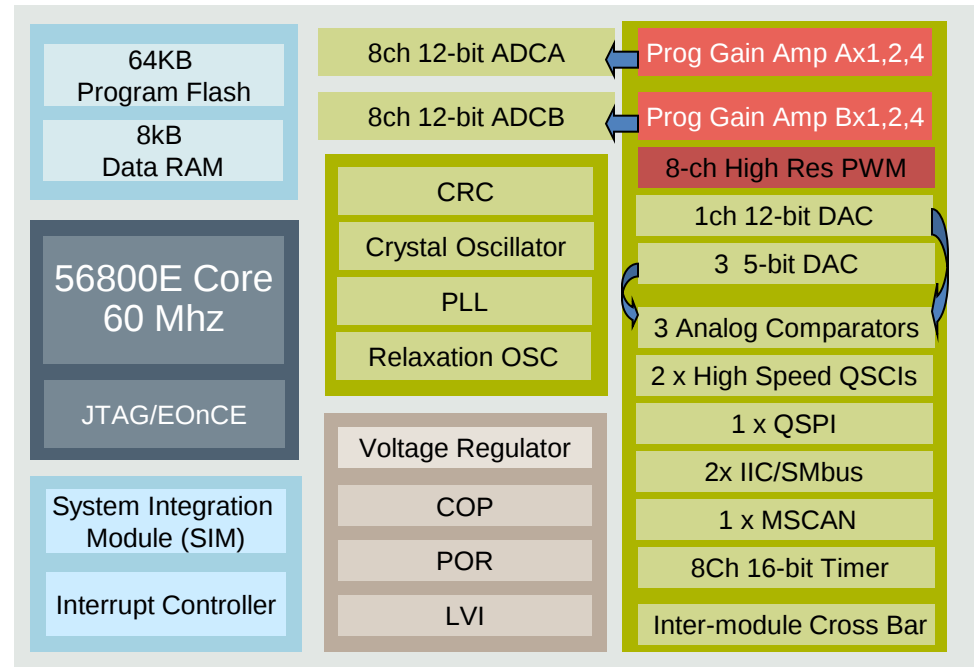
Other Features

- Bit Reversed Address Mode For FFT algorithms.
- Swap all address generation Unit Registers with Shadowed registers to reduce Interrupt context switch latency.

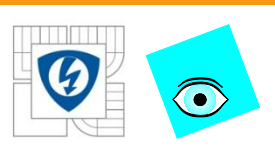


MC56F824x/MC56F825x Features

- 60 MHz/60 MIPS from 56800E core
- 2.7-3.6V operation
- 64K Bytes program FLASH
- 8K Bytes program/data RAM
- Flash security
- 8MHz/100KHz tunable internal relaxation oscillator
- Software programmable phase locked loop
- Up to 60 MHz peripherals – timers and PWMs
 - **8 output PWM module**
 - **520ps PWM and PFM resolution**
- 2-12-bit ADCs with total 16 inputs
 - **600ns conversion rate**
 - **built-in PGA with 1x, 2x, 4x, gains**
- 1 12-bit digital to analog converter
- 3 5-bit digital to analog converters
- 3 analog comparators
- 8 16-bit enhanced GP multifunction programmable timers
- Cyclic redundancy check generator (CRC)
- Computer operating properly timer
- 2 high speed serial communications interface (SCI)
- 1 queued serial peripheral interface (QSPI)
- 1 MS-CAN bus
- 2 I²C/SMBus communications interface
- Up to 54 GPIOs
- Inter module cross-bar
- JTAG/EOnCE™ debug port
- Industrial temperature range: -40°C to 105°C with 60 Mhz



44LQFP, 48LQFP 64 LQFP, Samples Available



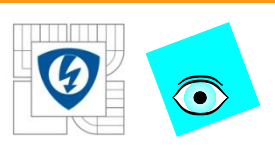
56F82xx Series Feature Summary

	56F8245	56F8246	56F8247	56F8255	56F8256	56F8257
Performance	60 MHz / MIP					
High Speed Peripheral Clock	120 MHz					
Program / Data Flash	48KB			64KB		
Program / Data RAM	6KB	6KB	8KB	8KB	8KB	8KB
Program Security	Yes					
eFlexPWM Channels	1 x 6ch	1 x 6ch	1 x 9ch	1 x 6ch	1 x 6ch	1 x 9ch
HiRes PWM Channels	6ch					
Enhanced FlexPWM w/ Input Capture	0	0	3	0	0	3
PWM Fault Inputs	4					
12-bit ADCs w/ PGA	2 x 4ch	2 x 5ch	2 x 8ch	2 x 4ch	2 x 5ch	2 x 8ch
12-bit DACs	1					
Analog Comparator w/ 5bit DAC Ref	3					
Cross Bar Module	Yes					
High Speed 16-bit Timer (TMR)	8					
GPIO (max 8mA)	35	39	54	35	39	54
IIC /SMBus	2					
QSCI (UART) / LIN Slave	2					
QSPI Synchronous	1					
CAN	0			1		
COP, POR, LVD, PLL CRC	Yes					
JTAG / EOnCE	Yes					
Operating Temperature Range	-40 °C to 105 °C					
Package	44 LQFP	48 LQFP	64 LQFP	44 LQFP	48 LQFP	64 LQFP

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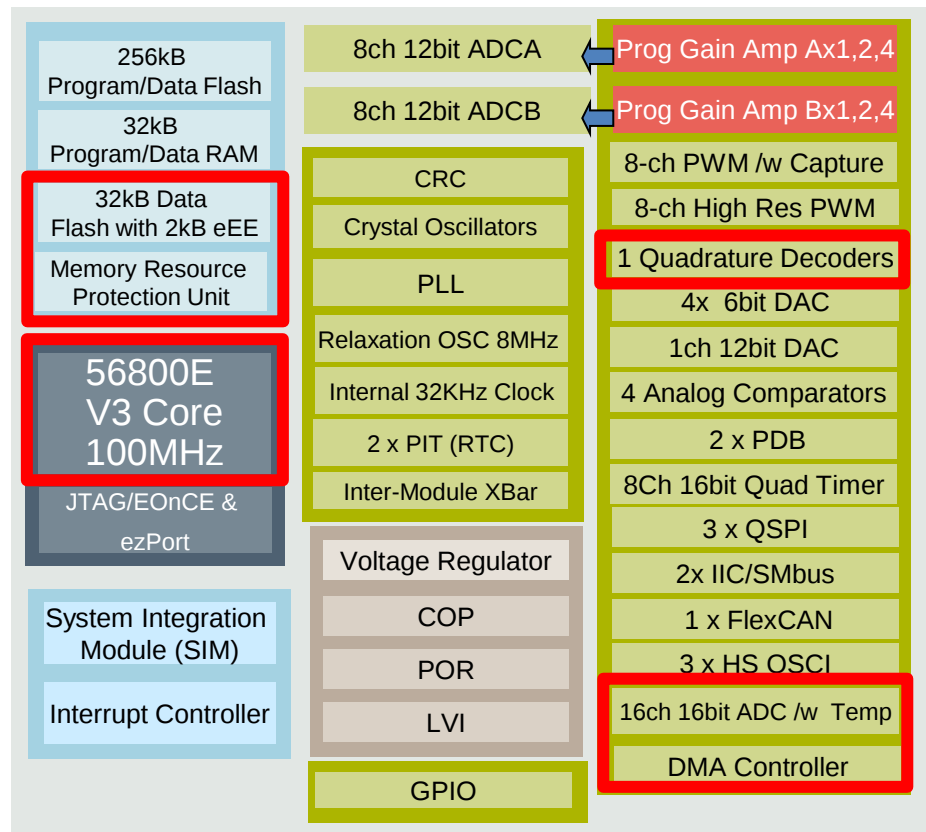




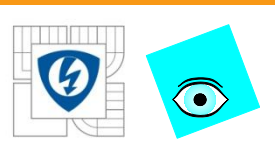
MC56F84xx Features

100 MHz/100MIPS 56800 V3 Core

- Harvard architecture
- **32 x 32bit MAC and 32bit arithmetic operation**
- 2.7-3.6V Operation
- 256kB Program/Data FLASH
- 32kB Data Flash with up to 2kB of eEE
- 32kB Data/Program RAM
- Resource Protection Unit
- 3 HS-QSCI (8MBS) , 3xQSPI, 2xIIC/SMBus, 1xFlexCAN
- Multi-purpose timers
 - 2 Periodic Timers with Real Time Interrupt Generation
 - 2 Programmable Delay Blocks
 - 8Ch multifunction timers
- 8ch High Resolution PWM Channels
 - **312ps PWM and PFM resolution**
- 8ch PWM Channels with Input Capture
- 8ch x 2 12-bit ADC converter with built-in PGA
 - **300ns/3.33Msps conversion time with 12bit resolution**
- 8ch 16bit SAR ADC with built-in temperature sensor and band gap.
 - 2us conversion time.
- 4 Analog Comparators
- 1 Quadrature Decoder
- 1ch 12bit DAC with external outputs + 4ch 6bit DAC
- DMA controller
- Inter-Module Crossbar
- On-chip voltage regulator (Single 3.3V Power Supply)
- System Integration : Internal relaxation oscillator, PLL, COP, 32kHz , EWM, auxiliary Internal clock, low voltage detect, EZPort
- 5V tolerant I/O
- **Temperature Range: -40°C to +105°C**

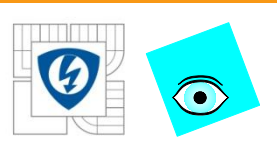


48 LQFP, 64 LQFP, 80LQFP, 100LQFP



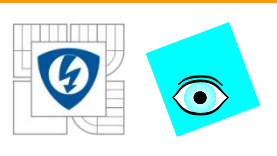
56F8400 Series Feature Summary

	Fully Featured Digital Control				Digital Control						Dual Motor				Single Motor			
Part Number																		
Core MHz	100	100	100	100	100	100	100	100	100	100	80	80	80	80	60	60	60	60
Flash Mem (kB)	256	256	128	128	128	128	64	64	128	128	256	256	128	128	128	128	64	64
SRAM Mem (kB)	32	32	24	24	24	24	16	16	24	24	32	32	16	16	16	16	8	8
Data Flash / EE Mem (kB)	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	0	0	32/2	32/2	32/2	32/2	0	0	0	0
Cyc ADC Chn	2x8	2x8	2x8	2x8	2x8	2x8	2x8	2x8	2x5	2x5	2x8	2x8	2x8	2x8	2x8/2x5	2x8/2x5	2x8/2x5	2x8/2x5
SAR ADC Chn	1x16	1x16	1x16	1x16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PWM uE Chn	8	8	8	8	8	8	8	8	8	8	8	8	8	8	0	0	0	0
PWM std Chn	8	8	8	8	0	0	0	0	0	0	8	8	8	8	8	8	8	8
DAC	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Quad Decoder	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	3	3	3	3	2	2	2	2	3	3	3	3	2	2	2	2
QSCI	3	3	3	3	3	3	2	2	2	2	3	3	2	2	2	2	2	2
QSPI	3	3	3	3	2	2	2	2	2	2	2	2	2	2	2	2	2	2
I2C	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
FlexCAN	1	1	1	1	1	1	1	0	0	0	1	1	1	1	0	0	0	0
Package	100	80	100	80	80	64	80	64	64	48	100	80	100	80	64	48	64	48



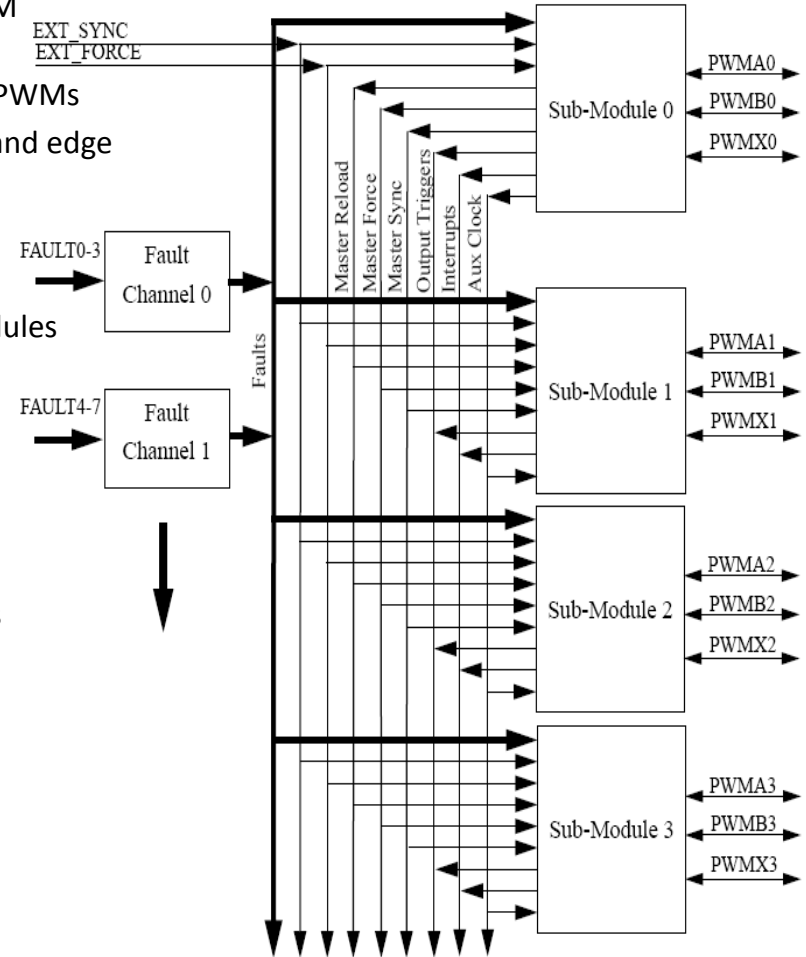
Agenda

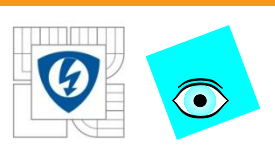
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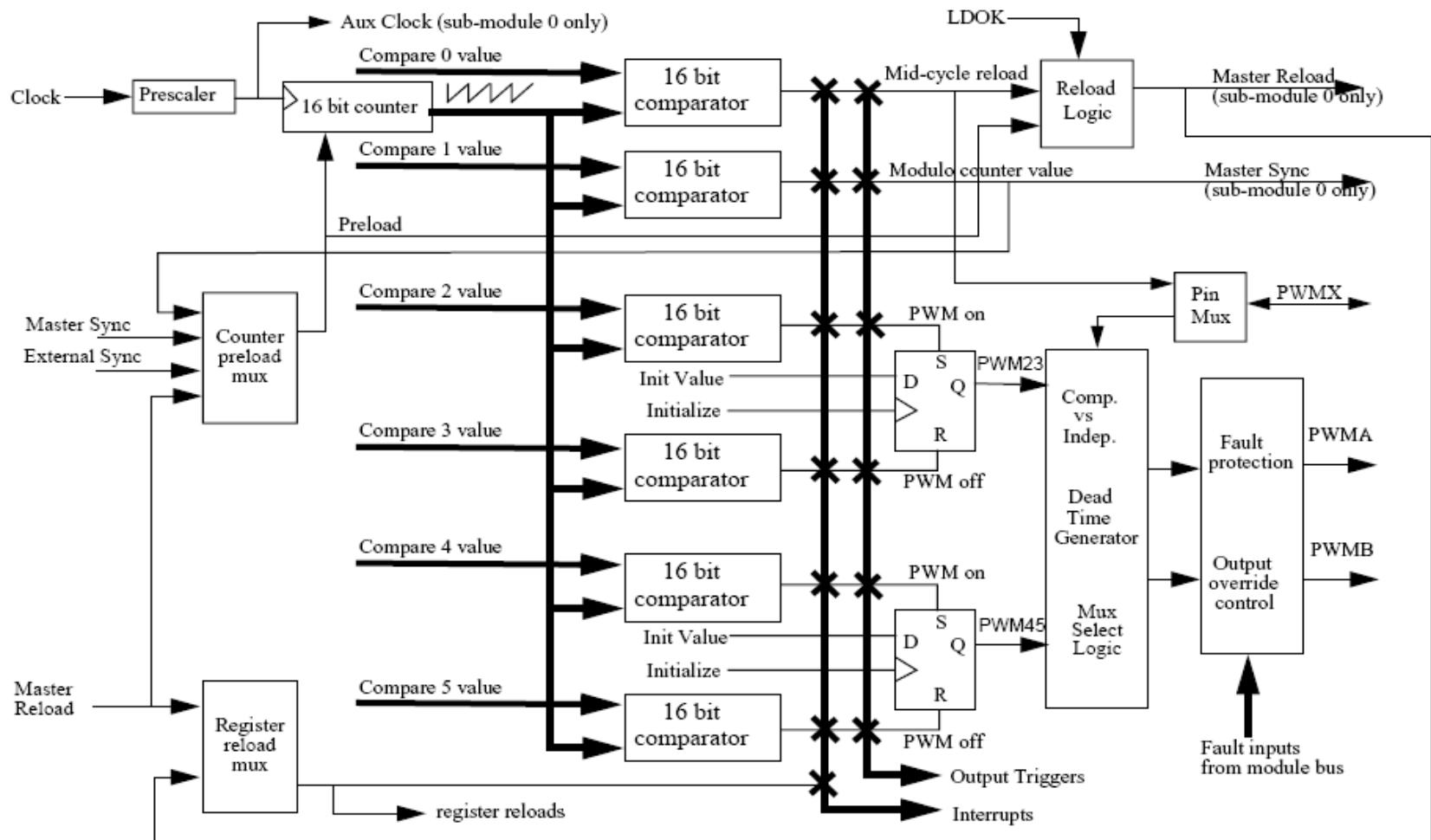
Enhanced Flex Pulse Width Modulator (eFlexPWM)

- Four independent sub-modules with own time base, two PWM outputs + 1 auxiliary PWM input/output
- 16 bits resolution for center, edge aligned, and asymmetrical PWMs
- Fractional delay for enhanced resolution of the PWM period and edge placement
- Complementary pairs or independent operation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM sub-modules
- Double buffered PWM registers
- Integral reload rates from 1 to 16 include half cycle reload
- Half cycle reload capability
- Multiple output trigger events per PWM cycle
- Support for double switching PWM outputs
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Individual software control for each PWM output
- Software control, and swap features via FORCE_OUT event
- Compare/capture functions for unused PWM channels
- Enhanced dual edge capture functionality

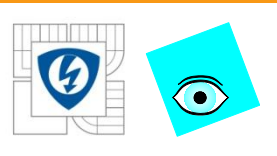




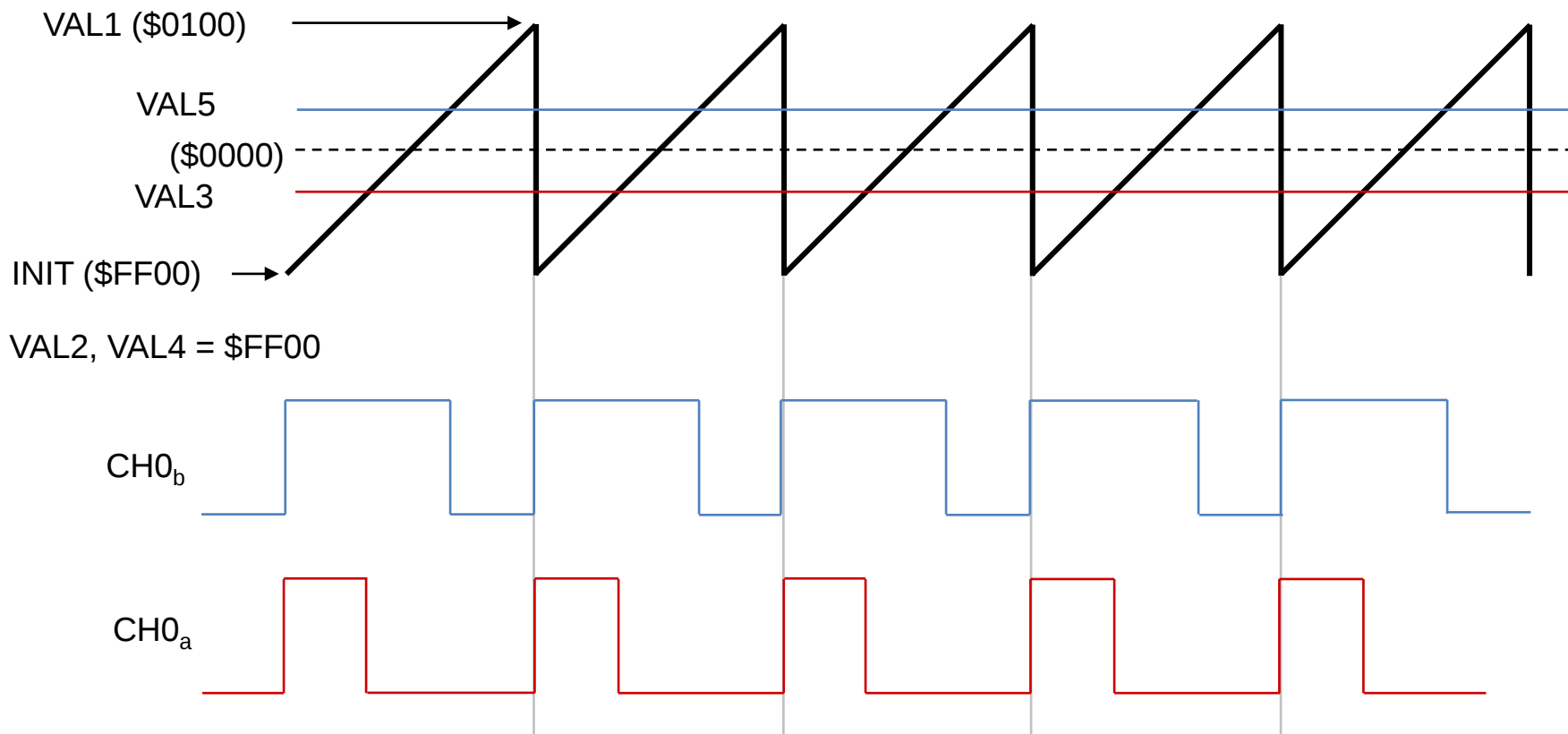
eFlexPWM - Sub-Module Detail





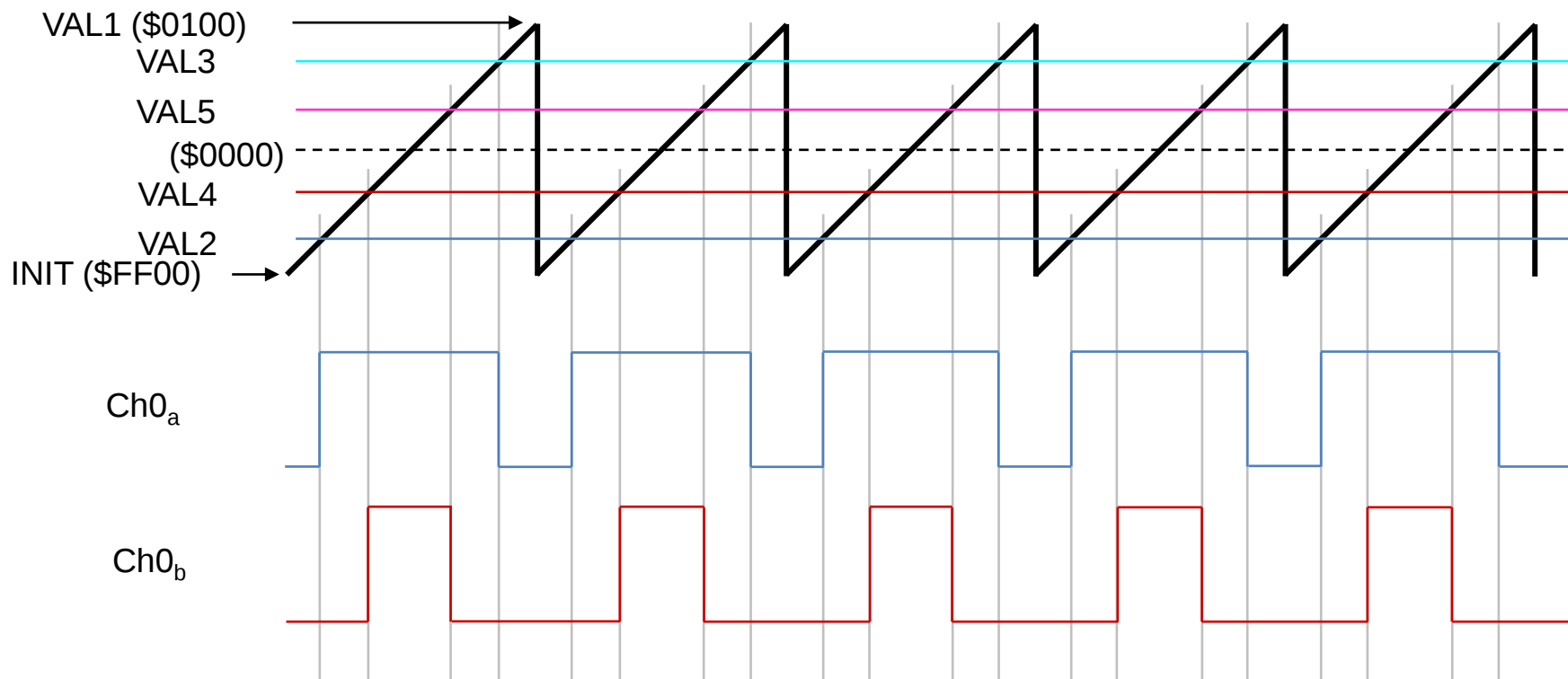


eFlexPWM – Edge Aligned PWM Generation

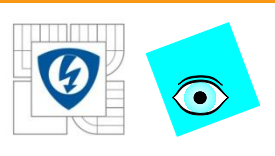


- All PWM-on values are set to the init value, and never changed again. Positive PWM-off values generate pulse widths above 50% duty cycle. Negative PWM-off values generate pulse widths below 50% duty cycle. This works well for bipolar waveform generation.

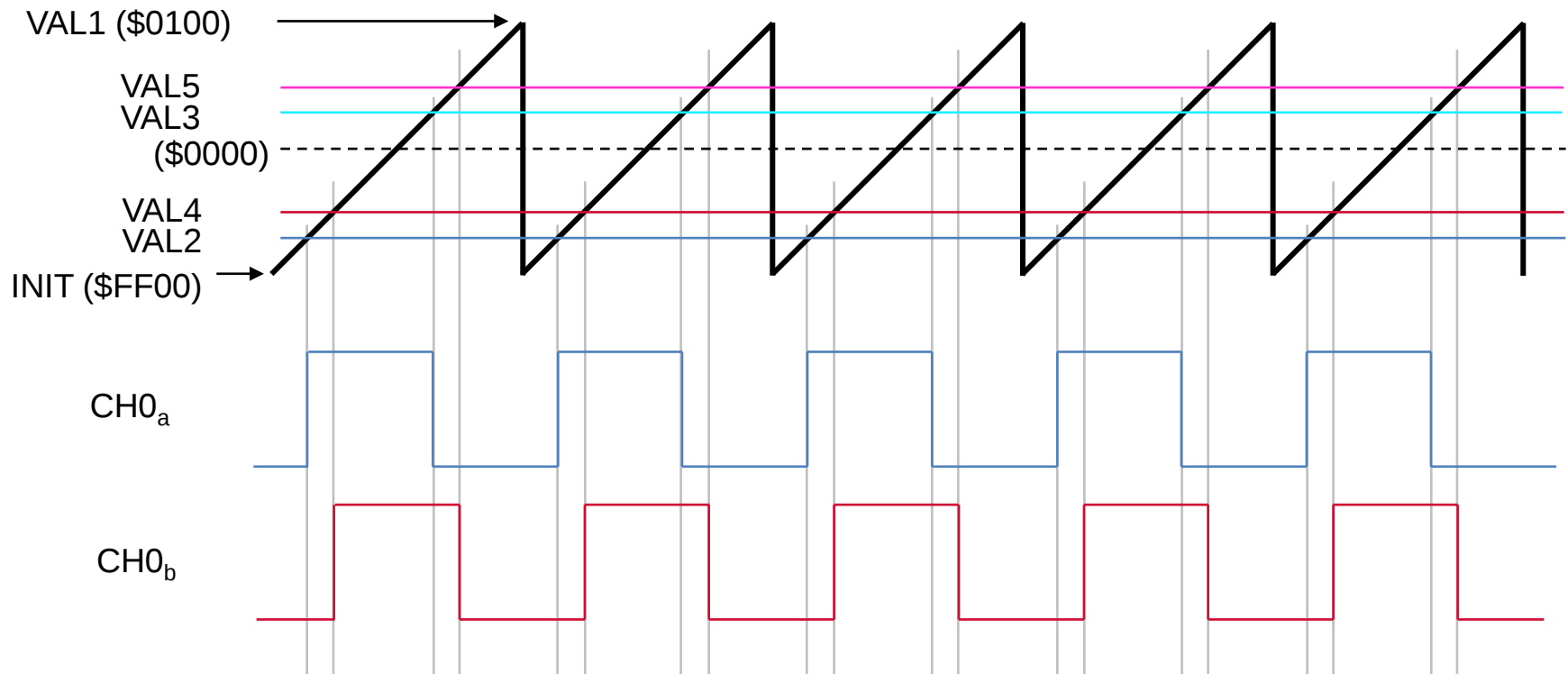
eFlexPWM – Center Aligned PWM Generation



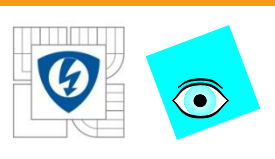
- When the Init value is the signed negative of the Modulus value, the PWM module works in signed mode. Center-aligned operation is achieved when the turn-on and turn-off values are the same number, but just different signs.



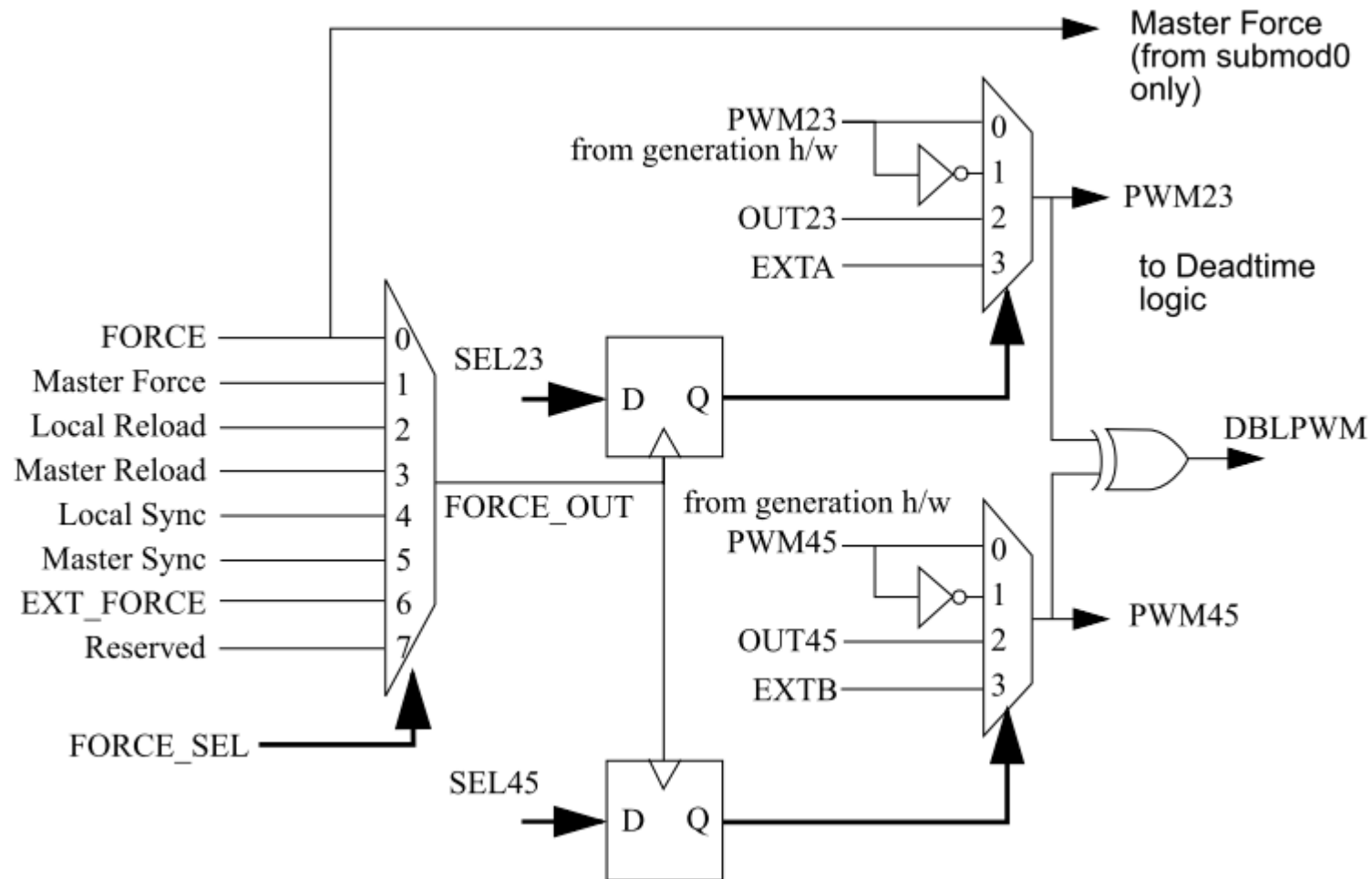
eFlexPWM – Shifted PWM Generation



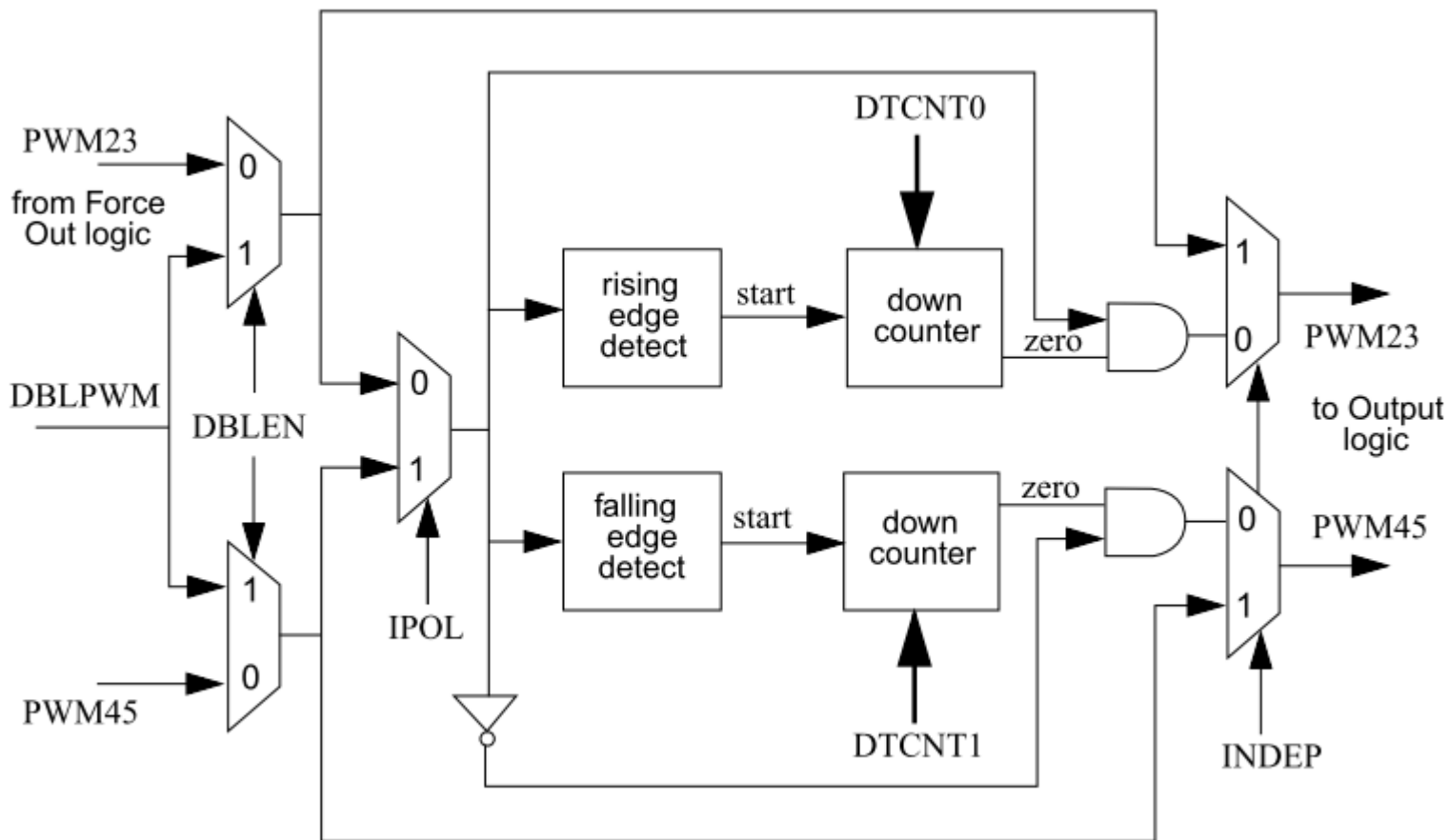
- In this example, both PWMs have the same duty-cycle. However, the edges are shifted relative to each other by simply biasing the compare values of one waveform relative to the other.

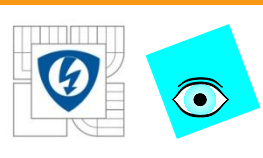


eFlexPWM – Force Output Logic

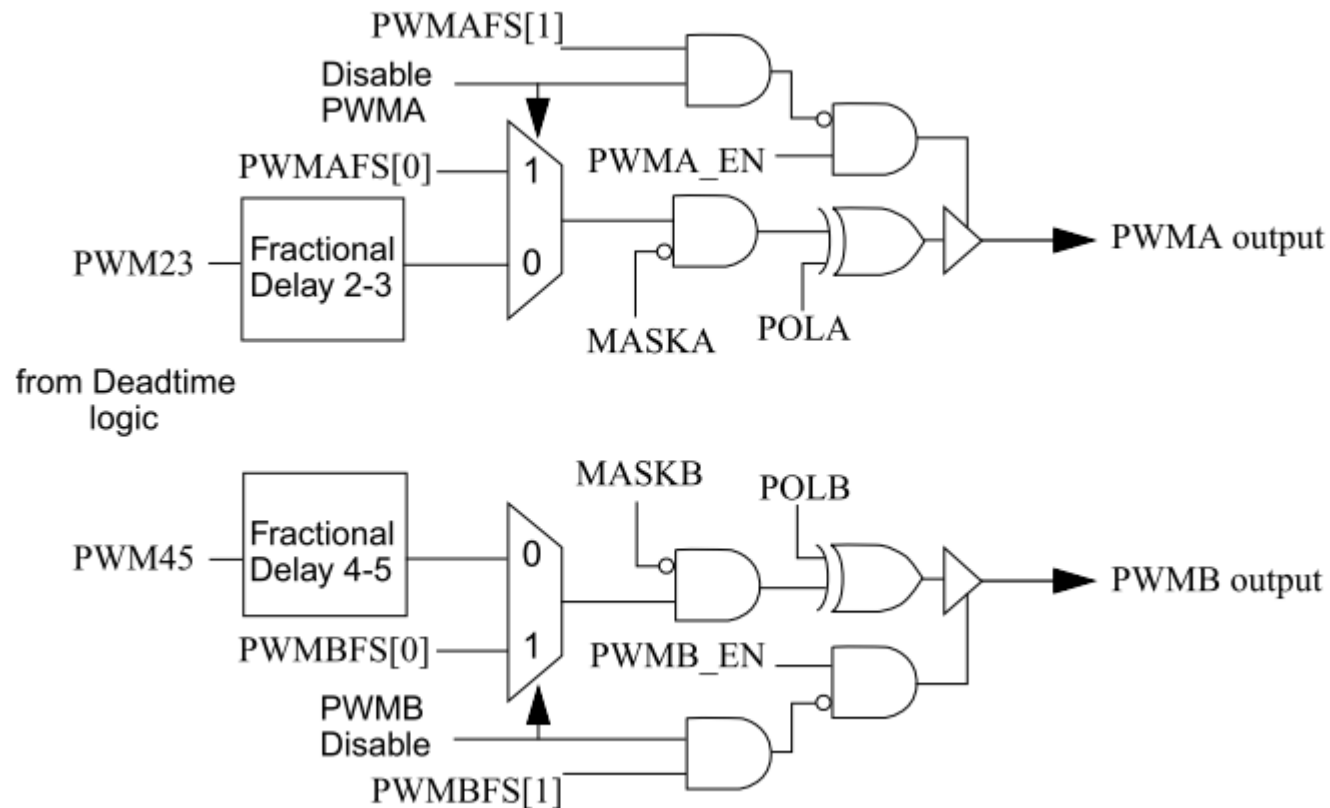


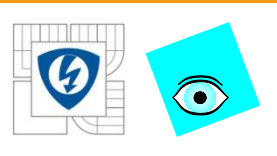
eFlexPWM – Complementary and Deadtime Logic





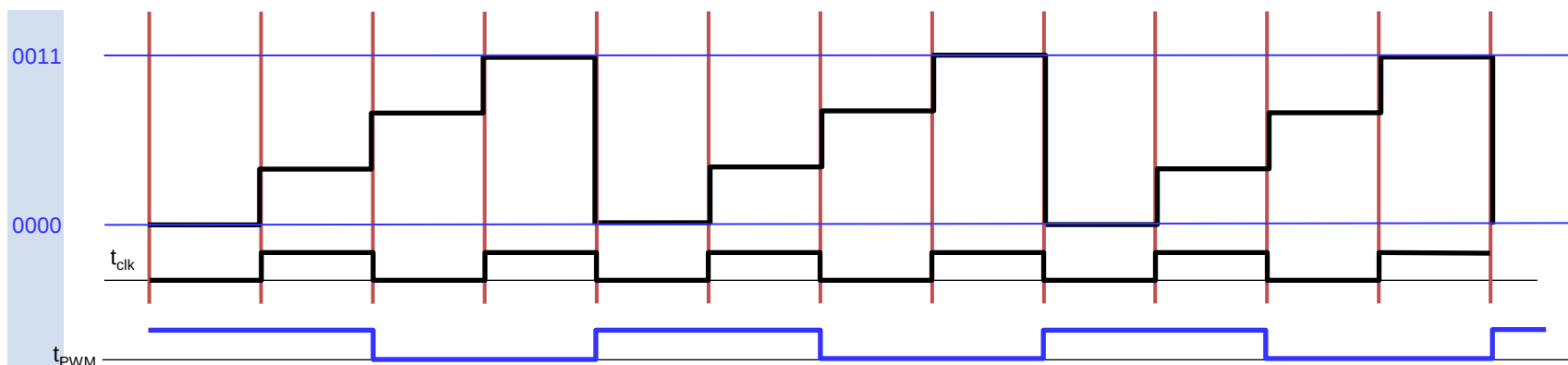
eFlexPWM – Fractional Delay and Output Logic

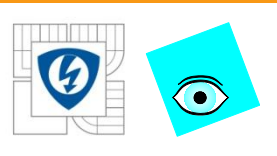




eFlexPWM – High Resolution Duty Cycle Generation

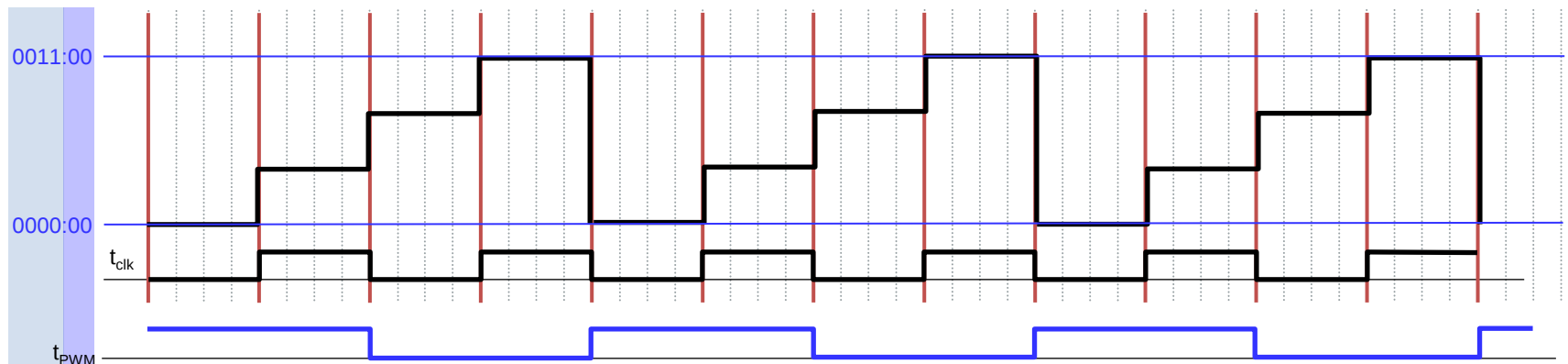
- PWM resolution is given by input clock of PWM module

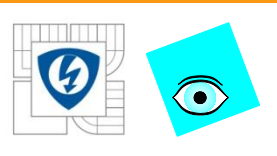




eFlexPWM – High Resolution Duty Cycle Generation

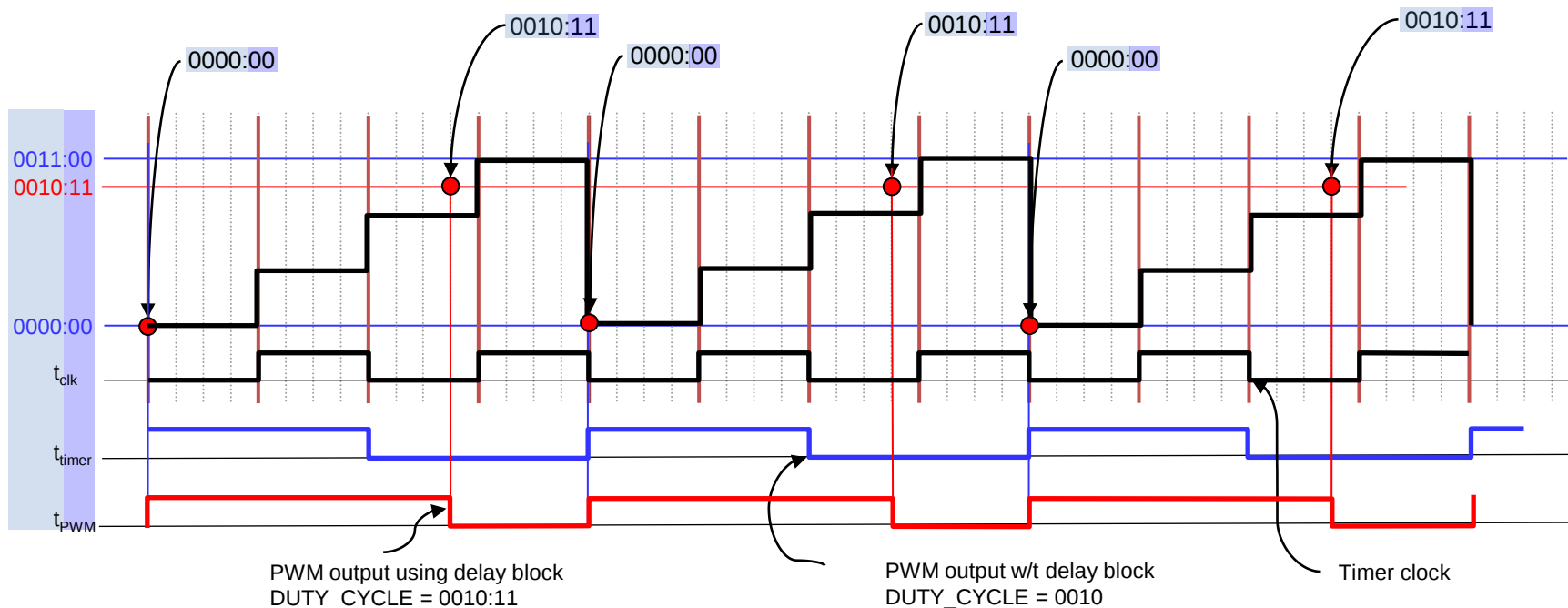
- PWM resolution is given by input clock of PWM module
- The PWM resolution can be enhanced by analog delay circuit, which can place edge between two edges, derived from input clock
- *Example*
 - Consider 2-bit analog delay block
 - Let's generate PWM signal with MODULO=4:0, DUTY_CYCLE=2:3 (68.75 %)





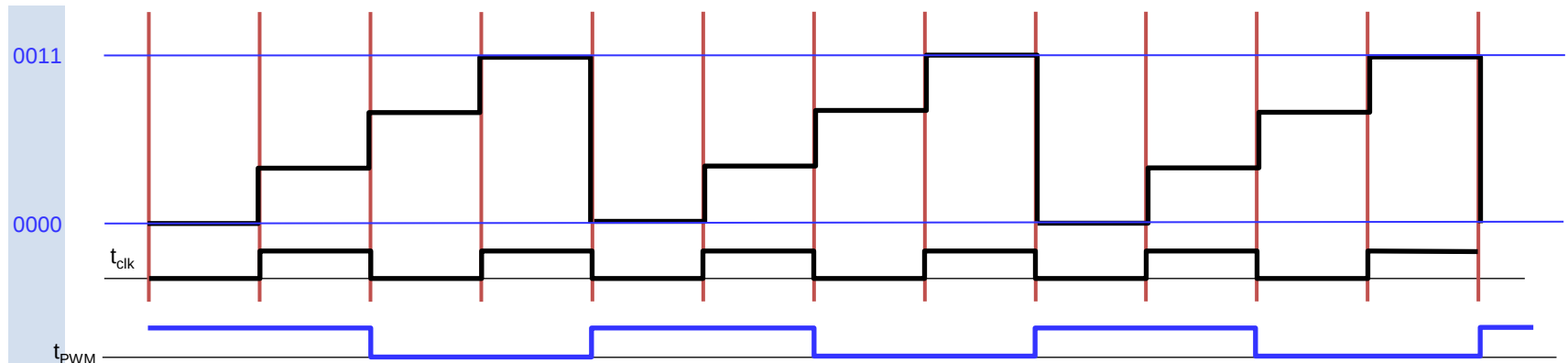
eFlexPWM – High Resolution Duty Cycle Generation

- At high resolution duty cycle generation
 - The leading edge is usually aligned with digital clock
 - The falling edge is generated by delay block
 - The analog delay is constant every PWM period



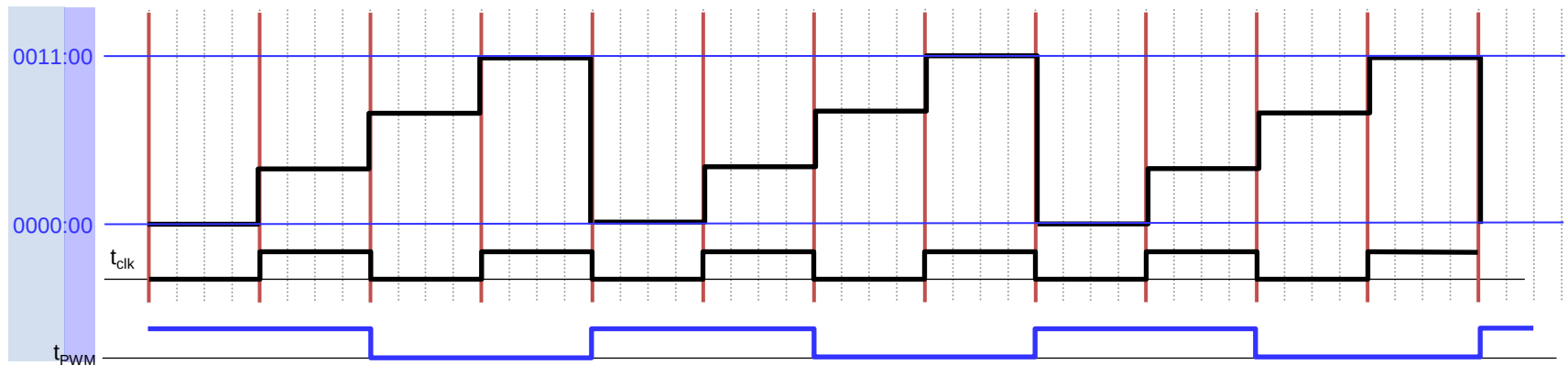
eFlexPWM – High Resolution Frequency Generation

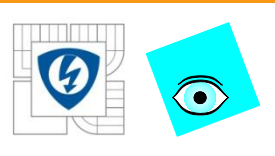
- *Example*
 - Consider 2-bit analog delay block
 - Let's generate PWM signal with $\text{MODULO}=4:2$, $\text{DUTY_CYCLE}=2:1$ (50 %)



eFlexPWM – High Resolution Frequency Generation

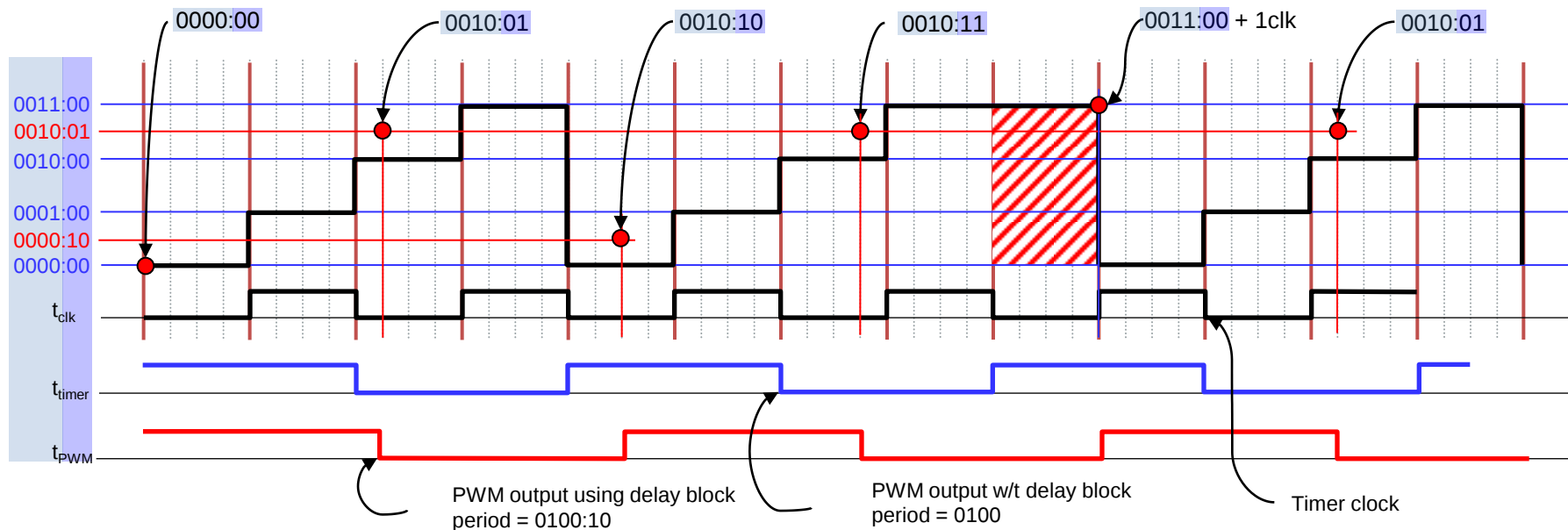
- *Example*
 - Consider 2-bit analog delay block
 - Let's generate PWM signal with MODULO=4:2, DUTY_CYCLE=2:1 (50 %)





eFlexPWM – High Resolution Frequency Generation

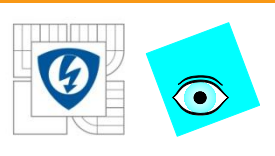
- At high resolution frequency generation
 - Both edges are generated by delay block
 - The analog delay is changing edge by edge every PWM period
 - The analog delay must be calculated every edge or requires some hardware support





-
- The diagram illustrates the NEP calculation logic for PWM period N, divided into three main sections by dashed lines: Ideal timing, Actual timing, and Timer.
- Ideal timing:** A block representing the ideal timing for PWM Period N. It is divided into two parts:
 - Top part: 16 bits at IP Bus timing resolution.
 - Bottom part: 5 bits NanoEdge timing resolution.
 - Actual timing:** A block representing the actual timing for PWM Period N. It is divided into two parts:
 - Top part: 16 bits at IP Bus timing resolution.
 - Bottom part: 5 bits NanoEdge timing resolution.
 - Timer:** A block representing the timer output for PWM Period N. It is divided into two parts:
 - Top part: 16 bits at IP Bus timing resolution.
 - Bottom part: 5 bits NanoEdge timing resolution.
- The logic flow is as follows:
- The **Ideal timing** block and the **PWM Period N-1** input (5 bits from previous NEP calculation) are combined in a **16 bit + 5 bit adder**.
 - The output of the adder is the **Actual timing** block.
 - The **Actual timing** block is then compared with the **Timer** block to determine the final output.

- 109



eFlexPWM – HR Frequency Generation

from User Perspective

- The new edge calculation is seen less from user perspective
- The user sets required 21-bit (16+5 bit) values into corresponding value registers only
- The 5-bit delay block corresponds to 1.92 GHz input clock (for 60MHz PWM module input clock)

16-bit digital value

PWM Value Register

NanoEdge™ placement not used. 16-bit value only.

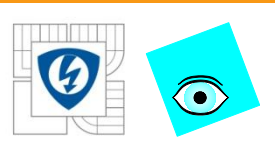
16-bit digital value

5-bit nano-
edge value

PWM Value Register

PWM Fractional Value Register

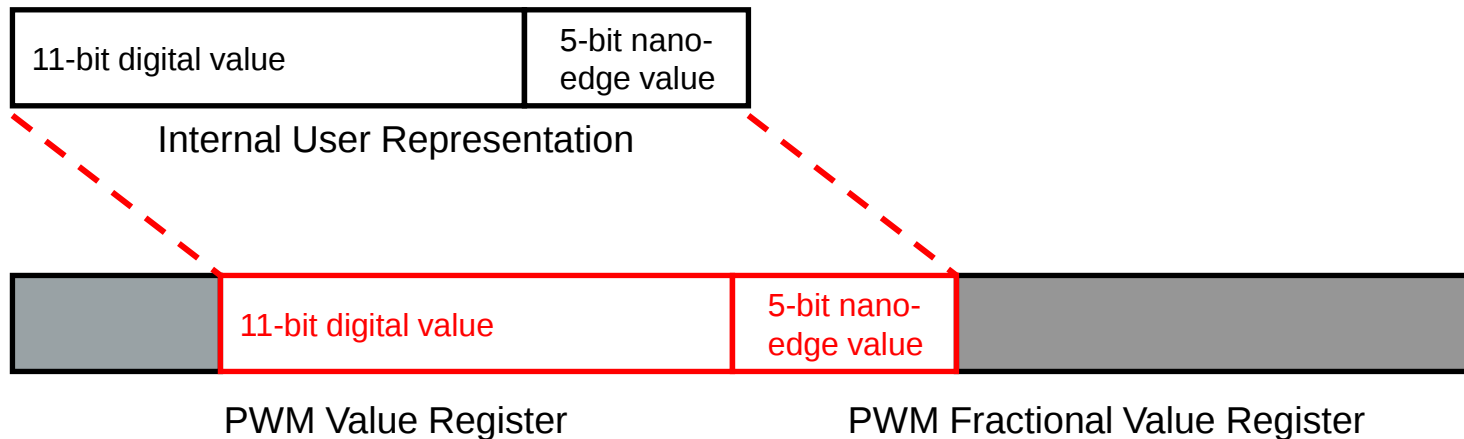
NanoEdge™ placement enabled. 21-bit (32-bit) value.



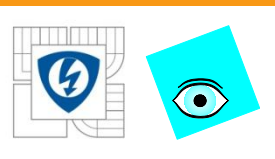
eFlexPWM – HR Frequency Generation

from User Perspective

- Example of high resolution calculation
 - For high frequency the digital value is usually less than 11 bits. For example, 200 kHz edge-aligned PWM has resolution less than 9 bits
 - Therefore we can keep calculation in 16 bits
 - Result of calculation is moved right by 5 bits and written into 32-bit register

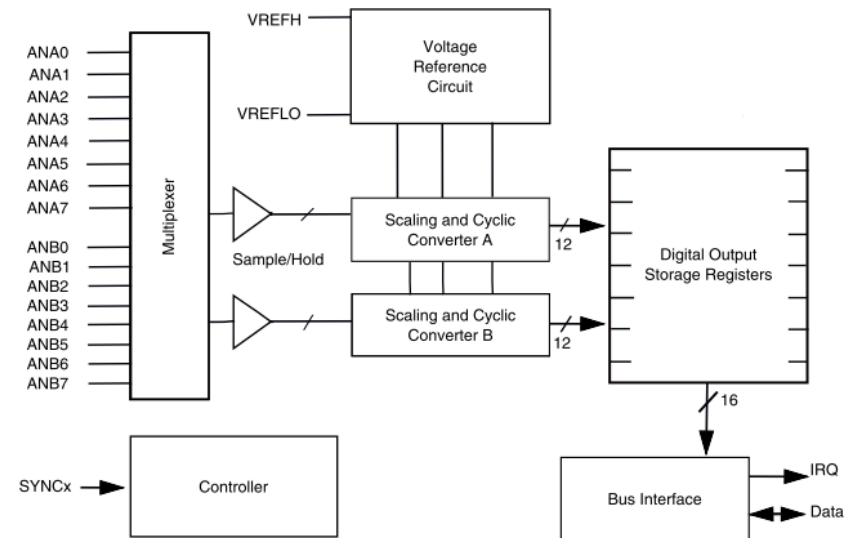


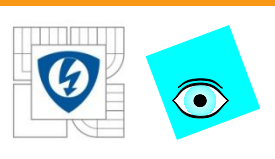
NanoEdge™ placement enabled. 21-bit (32-bit) value.



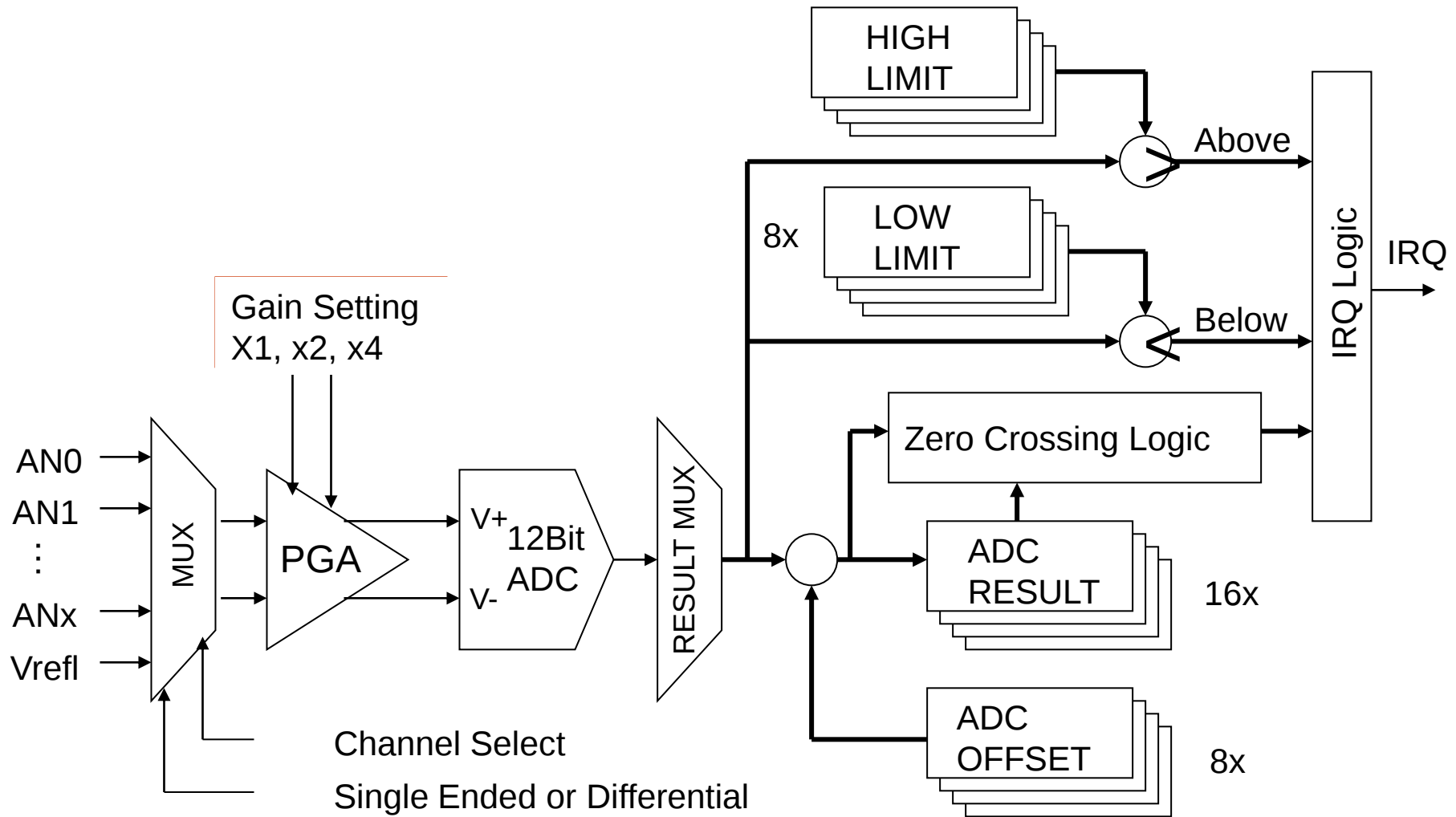
A/D Converter

- 12-bit resolution
- Maximum ADC clock frequency of 20 MHz with 50 ns period
- Sampling rate up to 6.66 million samples per second
- Single conversion time of 8.5 ADC clock cycles ($8.5 \times 50 \text{ ns} = 450 \text{ ns}$)
- Additional conversion time of 6 ADC clock cycles ($6 \times 50 \text{ ns} = 300 \text{ ns}$)
- ADC to PWM synchronization through the SYNC0/1 input signal sequentially scans and stores up to sixteen measurements
- Scans and stores up to eight measurements each on two ADC converters operating simultaneously and in parallel
- Scans and stores up to eight measurements each on two ADC converters operating asynchronously to each other in parallel
- Multi-triggering support
- Gains the input signal by x1, x2, or x4
- Optional interrupts at end of scan if an out-of-range limit is exceeded or there is a zero crossing
- Optional sample correction by subtracting a pre-programmed offset value
- Signed or unsigned result
- Single-ended or differential inputs
- PWM outputs with hysteresis for three of the analog inputs



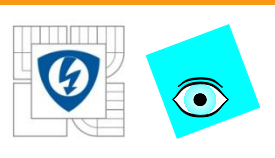


A/D Converter





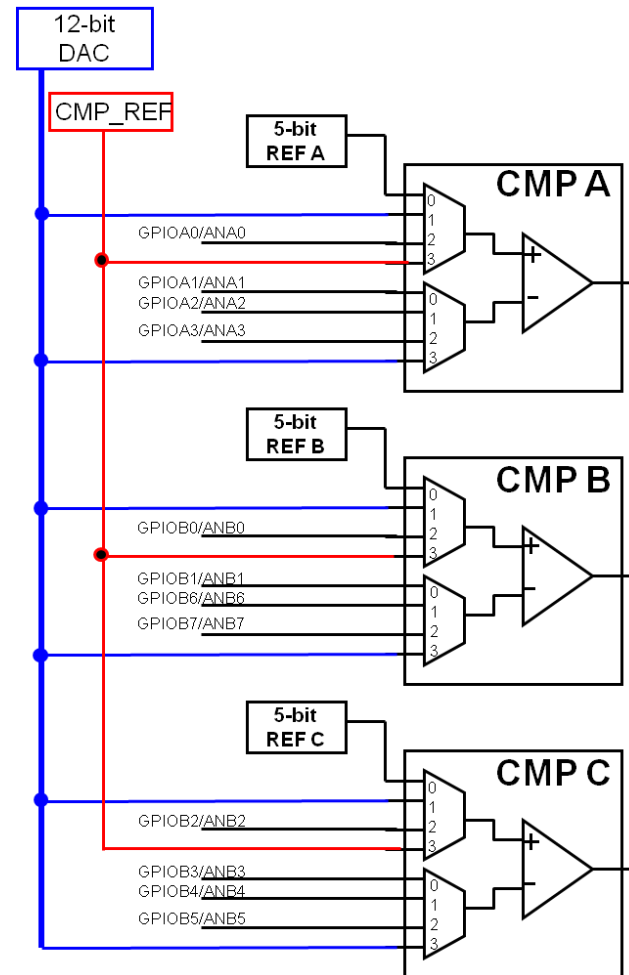
- Digitally filtered
 - Filter can be bypassed
-
- The diagram illustrates the AD_CONVERTER module. It features two 4-bit multiplexers for inputs P1-P4 and M1-M4. The P inputs are summed at the ACO (Analog-to-Digital Converter Output) block. The M inputs are routed to the WINDOW/SAMPLE input of the Window Control block. A Clock Prescaler takes the peripheral clock and FILTER_PER as inputs to produce a divided peripheral clock, which is then used by the Window Control and Filter Block. The Window Control block also receives a SE (Start Enable) signal. The Filter Block can be bypassed, as indicated by the text. The output of the Filter Block is sent to the Interrupt Control block, which generates the IRQ signal. The Filter Block also outputs COUT (to other SoC functions) and COUTA. The COUTA signal is routed through a multiplexer (controlled by COS) to the CMPO to PAD output.

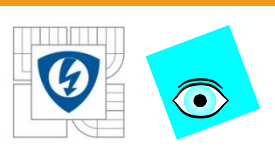


56F82xx Comparators Interconnection

	CMPA	CMPB	CMPC
P0	VREF A	VREF B	VREF C
P1	DACO	DACO	DACO
P2	ANA0	ANB0	ANB2
P3	cmpref	cmpref	cmpref
M0	ANA1	ANB1	ANB3
M1	ANA2	ANB6	ANB4
M2	ANA3	ANB7	ANB5
M3	DACO	DACO	DACO

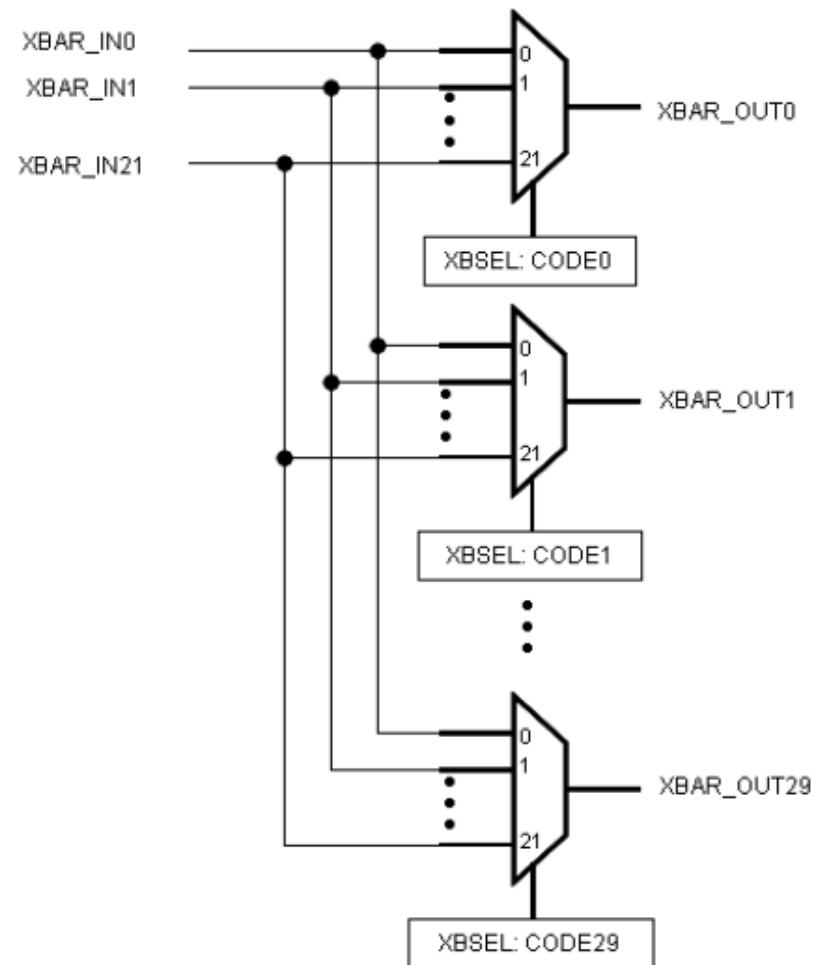
ADC PIN	COMP	COMP PIN
ANA0	CMPA	P2
ANA1	CMPA	M0
ANA2	CMPA	M1
ANA3	CMPA	M2
ANB0	CMPB	P2
ANB1	CMPB	M0
ANB2	CMPC	P2
ANB3	CMPC	M0
ANB4	CMPC	M1
ANB5	CMPC	M1
ANB6	CMPB	M1
ANB7	CMPB	M2



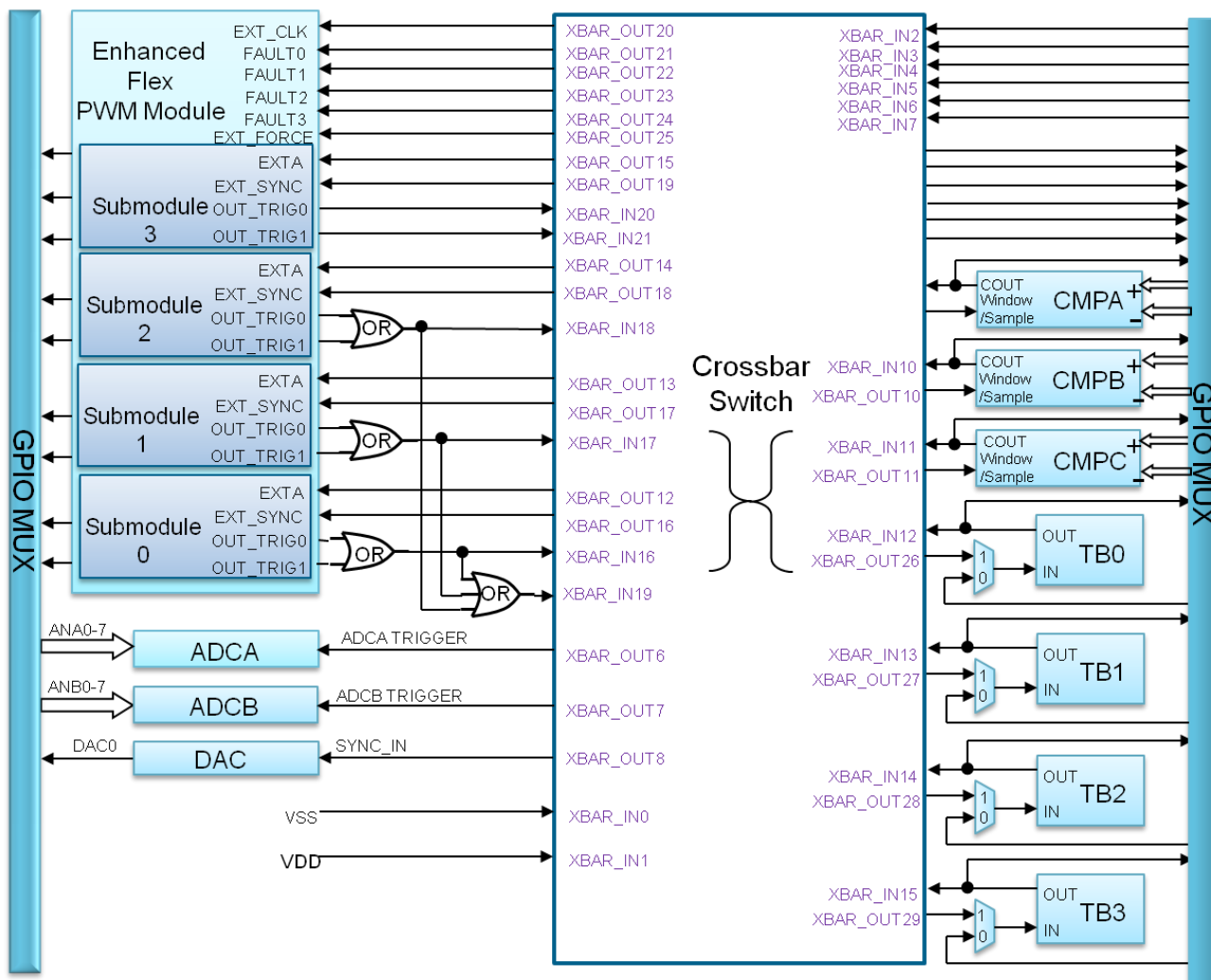


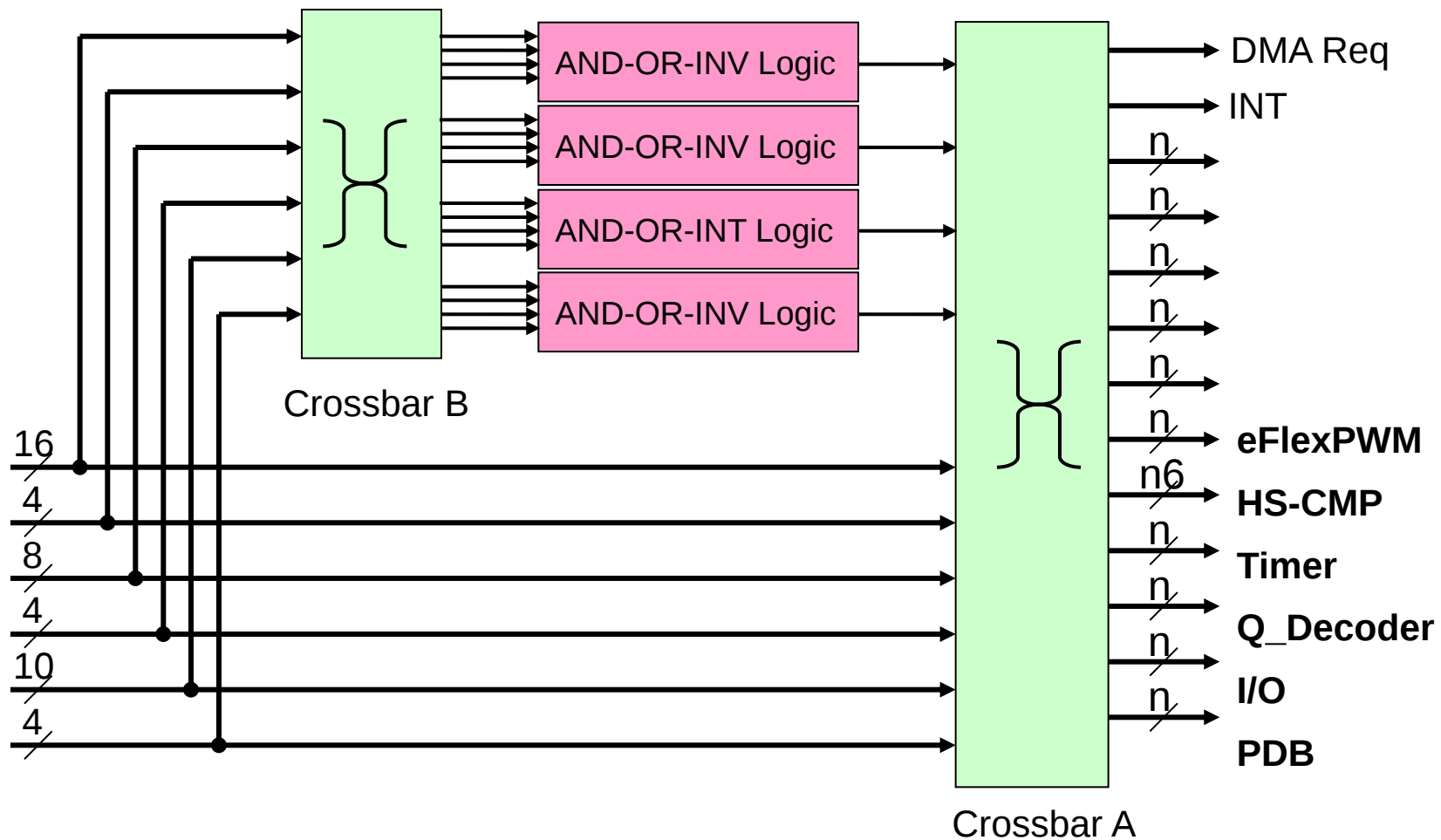
Crossbar Switch - MC56F824x/5x

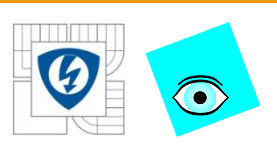
- Flexible signal interconnection among peripherals
- Connects any of 22 signals on left side to the output on right side (multiplexer)
- Total 30 multiplexers
- All multiplexers share the same set of 22 signals
- Increase flexibility of peripheral configuration according to user needs



Crossbar Inter-module Connection - MC56F824x/5x

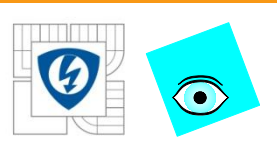






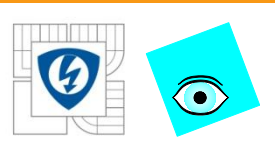
Agenda

- Linear Regulator
- Non-Isolated SMPS
- Isolated SMPS
- Resonant SMPS
- **Digital Control of SMPS**
 - Advantages of Digital Control
 - MCU Requirements
 - Example of suitable MCU's
 - Key MCU Peripherals
 - **Example of SMPS Application**
- Hands on (Step down Converter)



LLC Resonant Converter

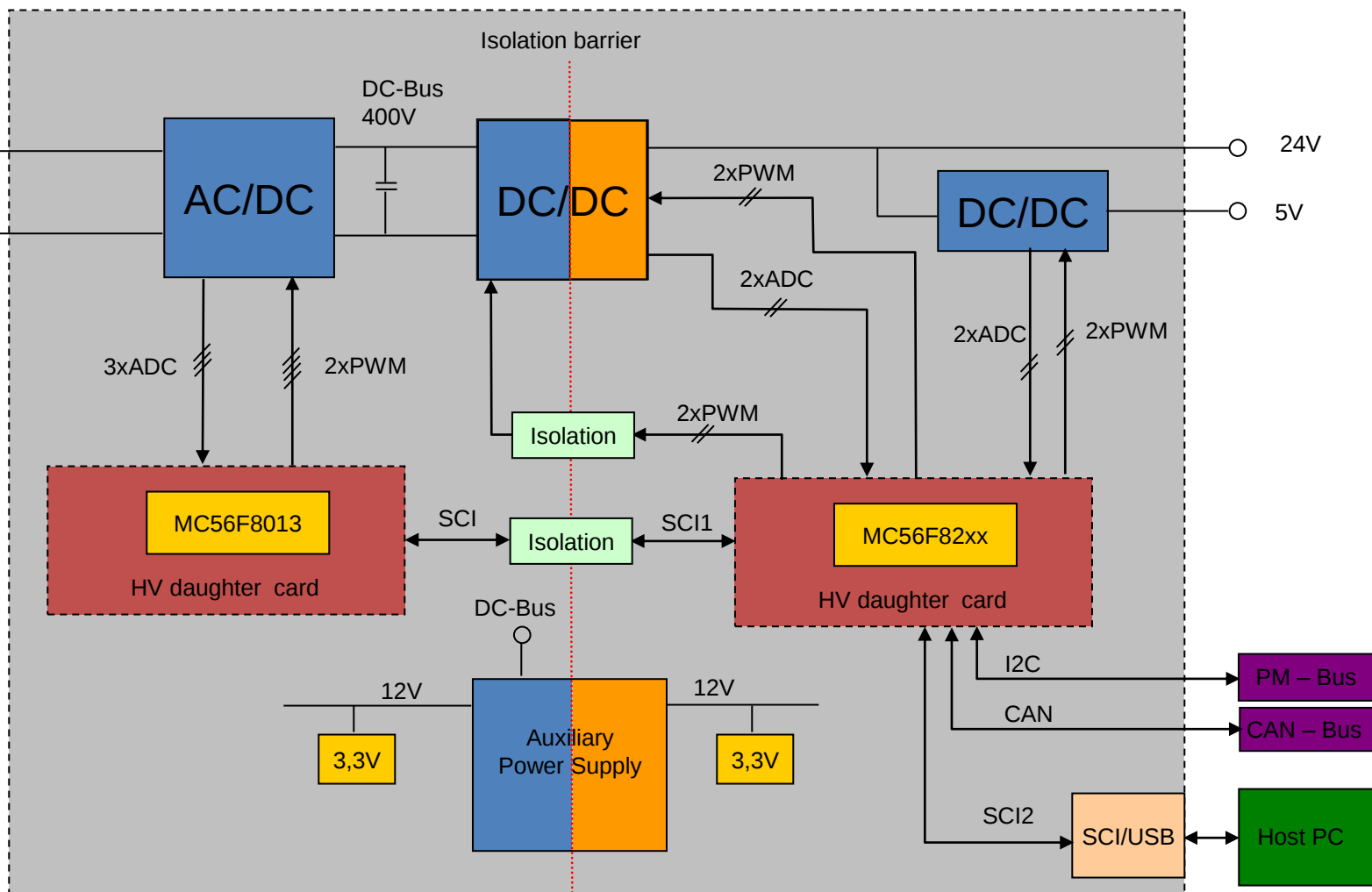
- Used SMPS Topology
 - Primary Side: Two Phase Interleaved PFC (Average Current Control)
 - Secondary Side: Half Bridge LLC Resonant Converter with Synchronous Rectification for 12V output
 - Additional Synchronous Buck Converter for 5V output
- Fully Digital Control by Two DSCs:
 - Primary Side: MC56F8013
 - Secondary Side: MC56F8257

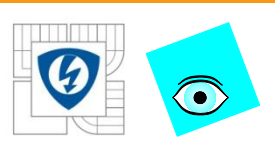


LLC Resonant Converter

- Input voltage
 - 85-265Vac @ 45-65Hz
- Output voltage
 - 24V/ 14 Amps (max.)
 - 5V/25 Amps (max.)
- Output Power
 - 350W shared by both voltage outputs. The power limit can be set individually by SW for each voltage output.
- Communication
 - PM Bus communication (HW ready)
 - CAN Communication (HW ready)
 - Communication with PC using USB
- Full Fault Protection
 - Over-voltage, Over-current, over-temperature on both primary and secondary side. Active controlled cooling

LLC Resonant Converter - Block Diagram

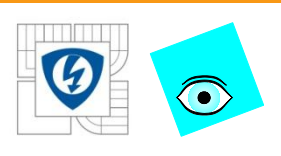




LLC Resonant Converter - Primary Side

- PFC Topology
 - Two Phase Interleaved Boost Converter
- PFC Control Algorithm
 - Fully Digital Average Current Control by DSC MC56F8013
- Measured Quantities
 - Input Rectified Voltage
 - Input Current
 - DC Bus Voltage
 - Heatsing Temperature
- Generated signals
 - 2x PWM signals for MOSFETs transistor (100kHz)
 - 1x PWM signal for cooling fan
 - 1x GPIO input relay control
- Fault Protection
 - HW over-current protection
 - SW over-voltage/under-voltage protection
 - SW over-temperature protection

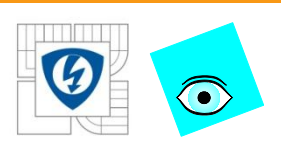




LLC Resonant Converter

- PFC SW Implementation

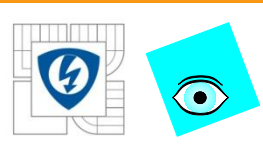
- Inner current loop
 - PI Controller running every 10 μs
- Outer voltage Loop
 - PI Controller with running every 500 μs
 - Optionally output power feedforward (sent from secondary side)
- Other Control Tasks
 - Cooling fan control based on heatsing temperature
 - Input relay control
 - Communication with secondary controller



LLC Resonant Converter

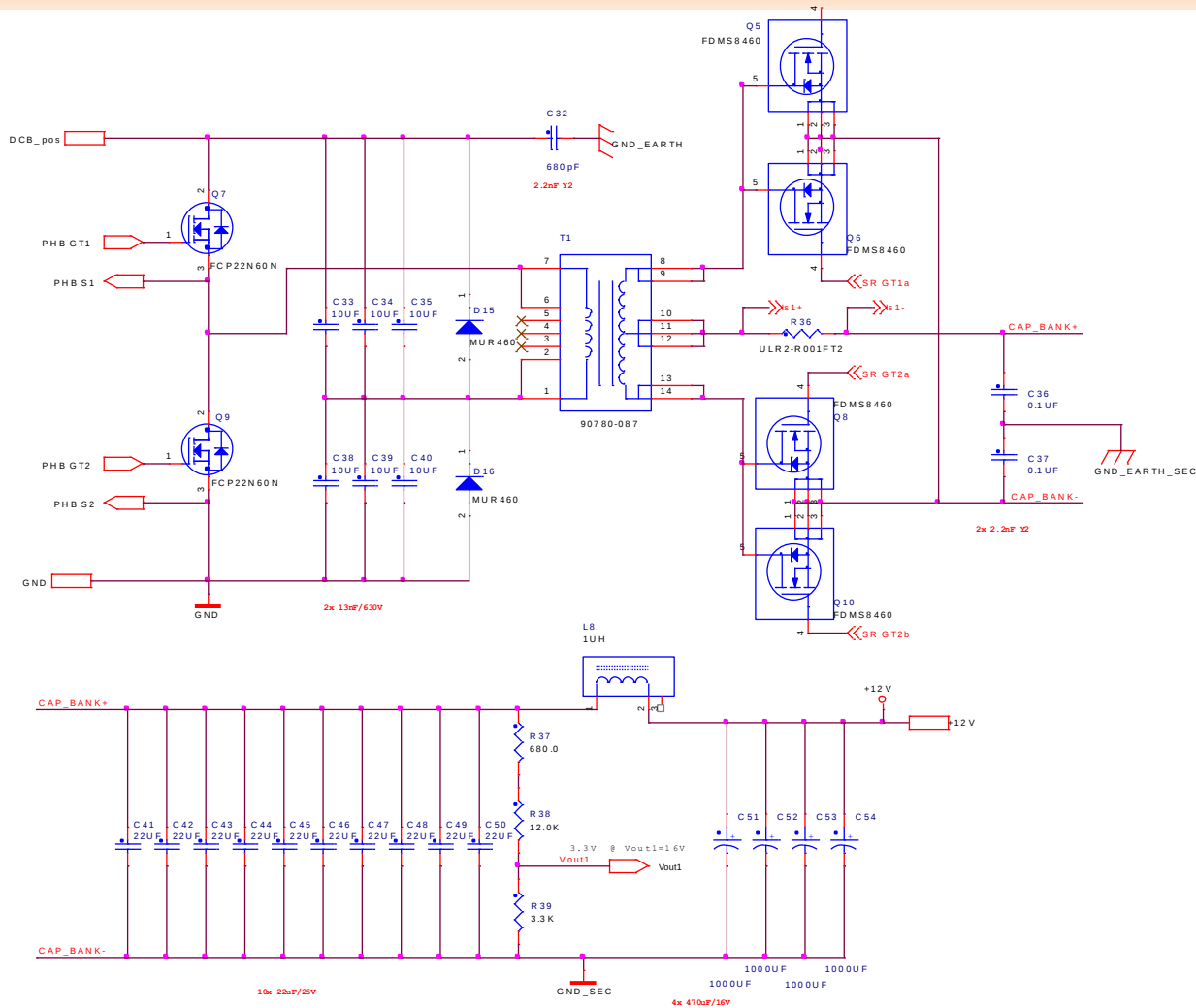
- Secondary Side

- Main Converter Topology (24V Output)
 - Half Bridge LLC Resonant Converter with synchronous rectification
- Secondary Converter Topology (5V Output)
 - Synchronous Buck Converter
- Control Algorithm
 - Fully Digital Voltage Mode Control by DSC MC56F8257 for both converters
- Measured Quantities
 - 2x Output Voltage
 - 2x Output Current
 - Secondary Side PCB Temperature
- Generated Signals
 - 2x PWM signals for half bridge MOSFET transistors (50% duty cycle, 100kHz – 400kHz)
 - 2x PWM signals for synchronous rectification MOSFET transistors (50% duty cycle, 100kHz – 400kHz)
 - 2x PWM signals for secondary buck MOSFET transistors (500 kHz)
- Fault Protection
 - 2x HW over-current protection
 - 2x SW over-voltage protection
 - Over-temperature protection



LLC Resonant Converter

- LLC Converter Schematic

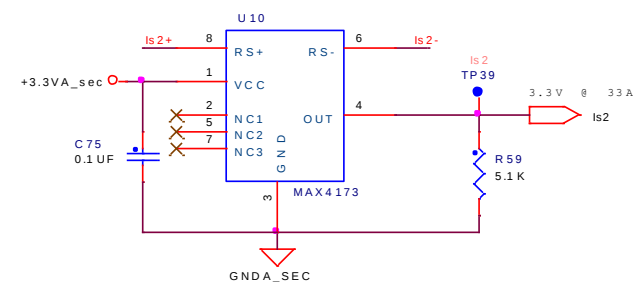
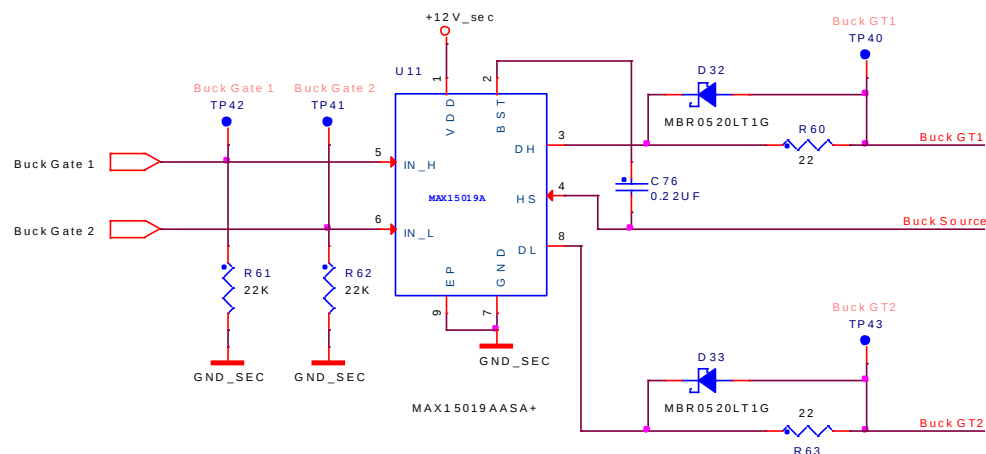
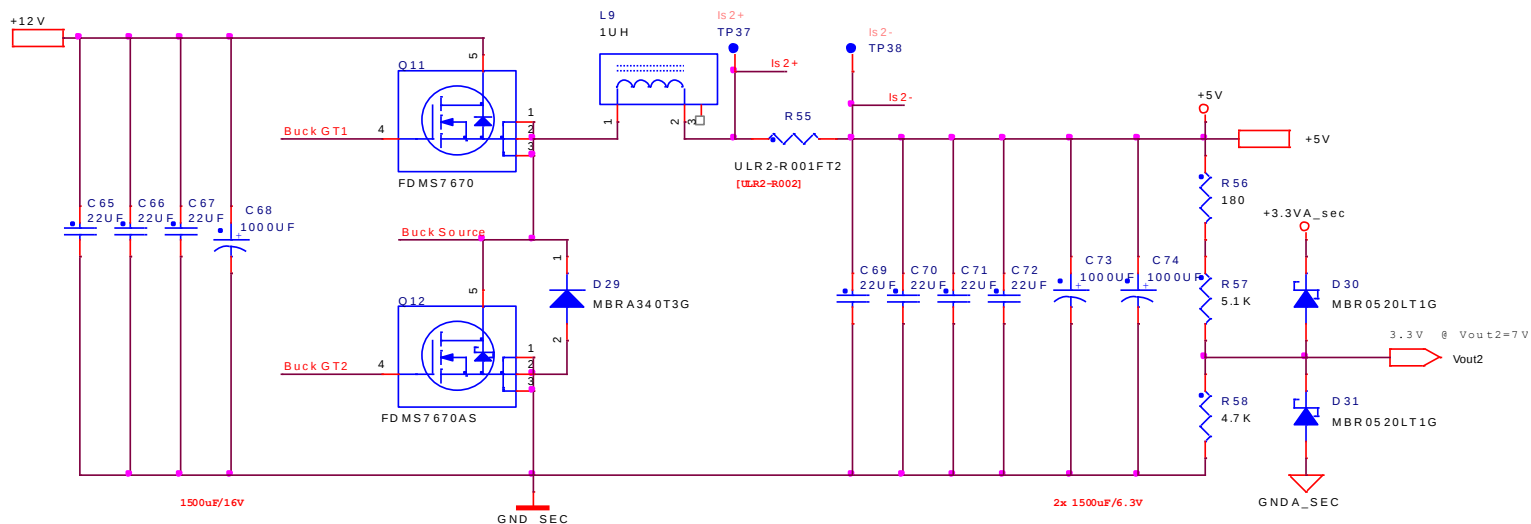


31.5-1. 6. 2012

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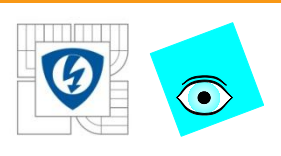
LLC Resonant Converter

- Buck Converter Schematic



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LLC Resonant Converter

- Secondary Side SW Implementation

- LLC Resonant Converter
 - PI Controller running every 10 μ s
- Buck Converter
 - PID Controller running every 10 μ s
- Other task Control
 - Communication with host PC
 - Communication with primary controller
 - Communication via PM Bus (Optional)
 - Communication via CAN (Optional)



LLC Resonant Converter

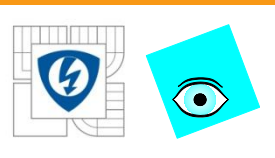
– Picture Gallery



31.5-1. 6. 2012

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LLC Resonant Converter

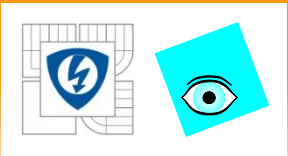
– Picture Gallery



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Thank you

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